Precision Picoampere Input Current Quad Operational Amplifier

OP497

FEATURES

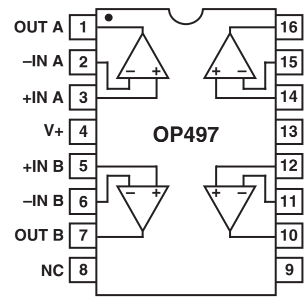
Low Offset Voltage: 50 μV max
Low Offset Voltage Drift: 0.5 μV/°C max
Very Low Bias Current
25°C: 100 pA max
–55°C to +125°C: 450 pA max
Very High Open-Loop Gain: 2000 V/mV min
Low Supply Current (per Amplifier): 625 μA max
Operates from ±2 V to ±20 V Supplies
High Common-Mode Rejection: 120 dB min

APPLICATIONS

Strain Gage and Bridge Amplifiers
High Stability Thermocouple Amplifiers
Instrumentation Amplifiers
Photo-Current Monitors
High Gain Linearity Amplifiers
Long-Term Integrators/Filters
Sample-and-Hold Amplifiers
Peak Detectors
Logarithmic Amplifiers
Battery-Powered Systems

PIN CONNECTIONS

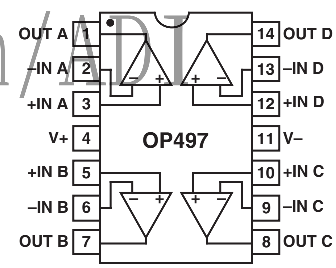
16-Lead Wide Body SOIC (S-Suffix)



NC = NO CONNECT

14-Lead Plastic Dip (P-Suffix)

14-Lead Ceramic Dip (Y-Suffix)



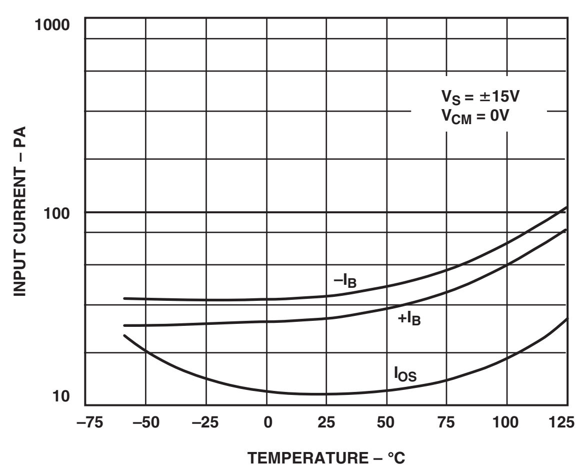
GENERAL DESCRIPTION

The OP497 is a quad op amp with precision performance in the space-saving, industry standard 16-lead SOIC package. Its combination of exceptional precision with low power and extremely low input bias current makes the quad OP497 useful in a wide variety of applications.

Precision performance of the OP497 includes very low offset, under 50 μV, and low drift, below 0.5 μV/°C. Open-loop gain exceeds 2000 V/mV ensuring high linearity in every application. Errors due to common-mode signals are eliminated by the OP497's common-mode rejection of over 120 dB. The OP497's power supply rejection of over 120 dB minimizes offset voltage changes experienced in battery-powered systems. Supply current of the OP497 is under 625 μA per amplifier, and it can operate with supply voltages as low as ±2 V.

The OP497 utilizes a superbeta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP497 is under 100 pA at 25°C and is under 450 pA over the military temperature range.

Combining precision, low power, and low bias current, the OP497 is ideal for a number of applications, including instrumentation amplifiers, log amplifiers, photo-diode preamplifiers, and long-term integrators. For a single device, see the OP97; for a dual device, see the OP297.



Input Bias, Offset Current vs. Temperature

REV. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

OP497–SPECIFICATIONS (@ V_S = 15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Condition	A Min	A Typ	A Max	F Min	F Typ	F Max	C/G Min	C/G Typ	C/G Max	Unit
INPUT CHARACTERISTICS												
Offset Voltage	Vos			20	50		40	75		80	150	µV
		–40°C ≤ +85°C					70	150		120	250	
		–55°C ≤ +125°C		40	100		80	150		140	300	
Average Input Offset Voltage Drift	TCV_{OS}	T_{MIN} – T_{MAX}		0.2	0.5		0.4	1.0		0.6	1.5	µV/°C
Long-Term Input Offset Voltage Stability				0.1			0.1			0.1		µV/Mo
Input Bias Current	I_B	V_{CM} = 0 V		30	100		40	150		60	200	pA
		–40° ≤ T_A ≤ +85°C					60	200		80	300	
		–55° ≤ T_A ≤ +125°C		80	450		110	600		130	600	
Average Input Bias Current Drift	TC_{IB}	–40° ≤ T_A ≤ +85°C					0.3			0.3		
		–55° ≤ T_A ≤ +125°C		0.5			0.7			0.7		pA/°C
Input Offset Current	Ios	V_{CM} = OV		15	100		30	150		50	200	pA
		–40° ≤ T_A ≤ +85°C					50	200		80	300	
		–55° ≤ T_A ≤ +125°C		35	400		60	600		90	600	
Average Input Offset Current Drift	T_CI_{OS}			0.2			0.3			0.4		pA/°C
Input Voltage Range[1]	IVR		+ 13	+14		+13	tl4		+13	+14		V
		T_{MIN} – T_{MAX}	+13	+13.5		+13	+13.5		+13	+13.5		
Common-Mode Rejection	CMR	V_{CM} = ±13 V	120	140		114	135		114	135		dB
		T_{MIN} – T_{MAX}	114	130		108	120		108	120		
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 2 kΩ	2000	6000		1500	4000		1200	4000		V/mV
		–40° ≤ T_A ≤ +85°C				800	2000		800	2000		
		–55° ≤ T_A ≤ +125°C	1200	4000		1000	3000		800	3000		
Input Resistance Differential Mode	R_{IN}			30			30			30		MΩ
Input Resistance Common Mode	R_{INCM}			500			500			500		GΩ
Input Capacitance	C_{IN}			3			3			3		pF
OUTPUT CHARACTERISTICS												
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±13.7		±13	±13.7		±13	±13.7V		
		R_L = 10 kΩ	± 13	±14		±13	±14		±13	±14		
		T_{MIN} – T_{MAX} R_L = 10 kΩ	±13	±13.5		±13	±13.5		±13	±13.5		
Short Circuit	I_{SC}			±25			±25			±25		mA
POWER SUPPLY												
Power Supply Rejection Ratio	PSRR	Vs = ±2 V to ±20 V	120	140		114	135		114	135		dB
		Vs = ±2.5 V to ±20 V T_{MIN} – T_{MAX}	114	130		108	120		108	120		
Supply Current	I_{SY}	No Load		525	625		525	625		525	625	µA
(per Amplifier)		T_{MIN} – T_{MAX}		580	750		580	750	580	750		
Supply Voltage Range	V_S	Operating Range	±2		±20	±2		±20	±2		±20	V
		T_{MIN} – T_{MAX}	±2.5		±20	±2.5		±20	±2.5		±20	
DYNAMIC PERFORMANCE												
Slew Rate	SR		0.05	0.15		0.05	0.15		0.05	0.15		V/µS
Gain Bandwidth Product	GBW			500			500			500		kHz
Channel Separation	CS	V_O = 20 V_{p-p}, fo = 10 Hz		150			150			150		dB
NOISE PERFORMANCE												
Voltage Noise	$e_{n\ p-p}$	0.1 Hz to 10 Hz		0.3			0.3			0.3		µV/p-p
Voltage Noise Density	e_n = 10 Hz			17			17			17		nV/$\sqrt{Hz}$
	e_n = 1 kHz			15			15			15		nV/$\sqrt{Hz}$
Current Noise Density	i_n = 10 Hz			20			20			20		fA/$\sqrt{Hz}$

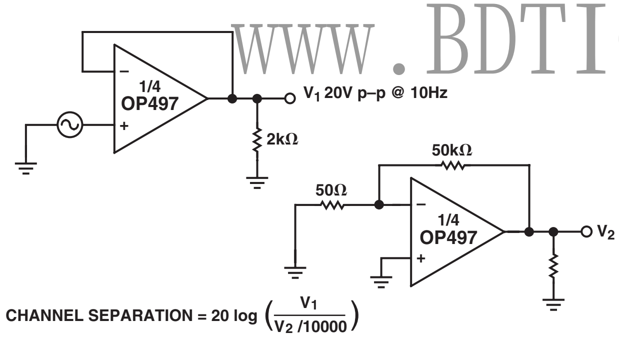
NOTE
[1]Guaranteed by CMR Test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±20 V
Input Voltage[2] . . . . 20 V
Differential Input Voltage[2] . . . . 40 V
Output Short-Circuit Duration . . . . Indefinite
Storage Temperature Range
  Y Package . . . . –65°C to +175°C
  P, S Package . . . . –65°C to +150°C
Operating Temperature Range
  OP497A, C (Y) . . . . –55°C to +125°C
  OP497F, G (Y) . . . . –40°C to +85°C
  OP497F, G (P, S) . . . . –40°C to +85°C
Junction Temperature
  Y Package . . . . –65°C to +175°C
  P, S Package . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . 300°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
14-Pin Cerdip (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	92	23	°C/W

NOTES
[1]Absolute Maximum Ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
[3]HIA is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.



Channel Separation Test Circuit

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP497AY*	–55°C to +125°C	14-Lead Cerdip	Q-14
OP497CY*	–55°C to +125°C	14-Lead Cerdip	Q-14
OP497FP	–40°C to +85°C	14-Lead Plastic DIP	N-14
OP497FS	–40°C to +85°C	16-Lead SOIC	R-16
OP497GP	–40°C to +85°C	14-Lead Plastic DIP	N-14
OP497GS	–40°C to +85°C	16-Lead SOIC	R-16

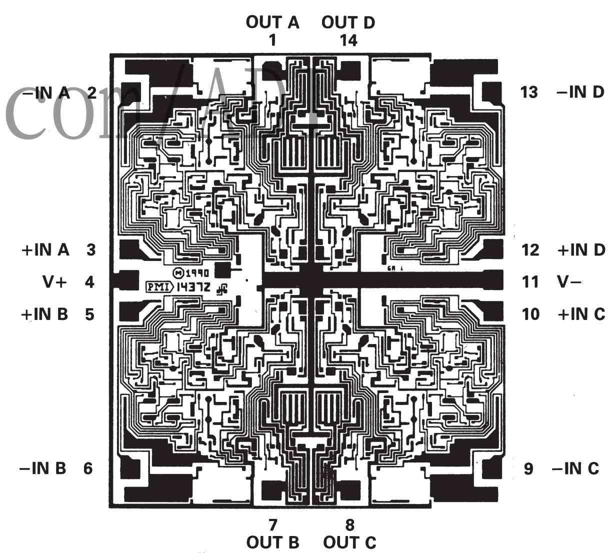
*Not for new design; obsolete April 2002.

For a military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs.milspec./default.asp.

SMD Part Number	ADI Part Number
5962–9452101M2A*	OP497BRC
5962–9452101MCA	OP497BY

*Not for new designs; obsolete April 2002.

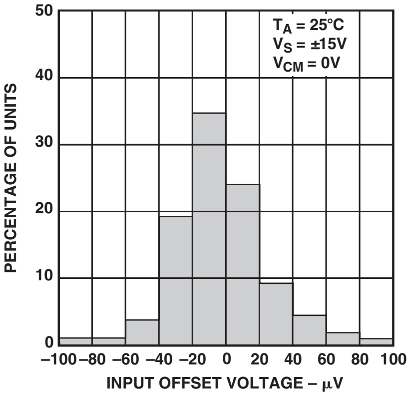
DICE CHARACTERISTICS



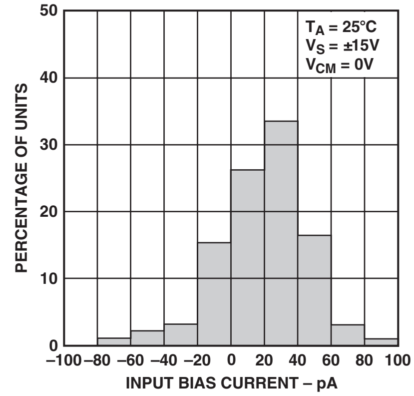
Die Size 0.112 × 0.129 inch, 14,448 sq. mils

CAUTION

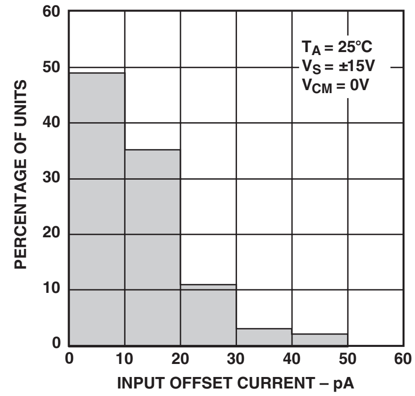
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP497 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



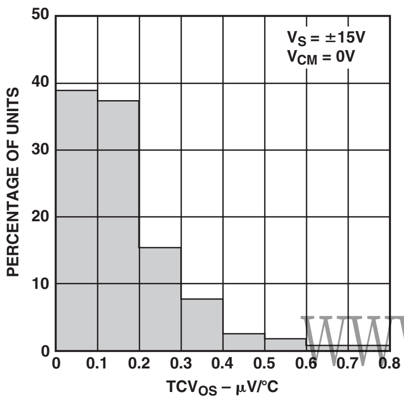
TPC 1. Typical Distribution of Input Offset Voltage



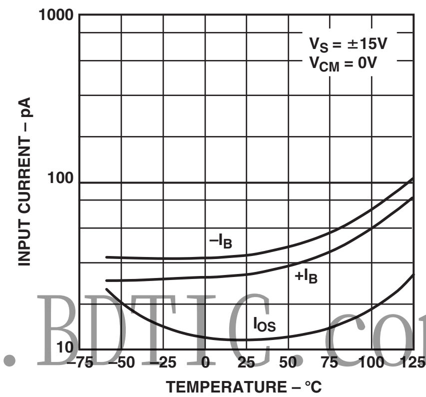
TPC 2. Typical Distribution of Input Bias Current



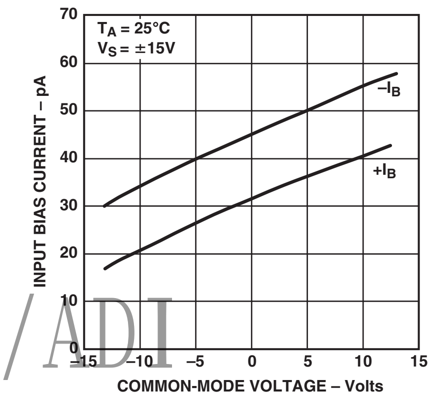
TPC 3. Typical Distribution of Input Offset Current



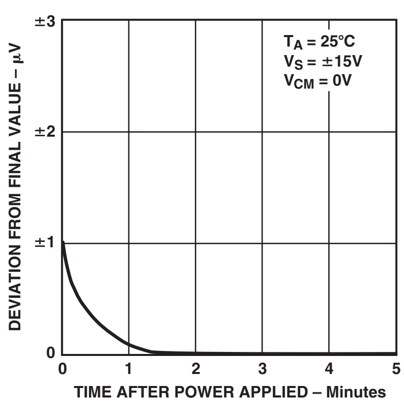
TPC 4. Typical Distribution of TCV_{OS}



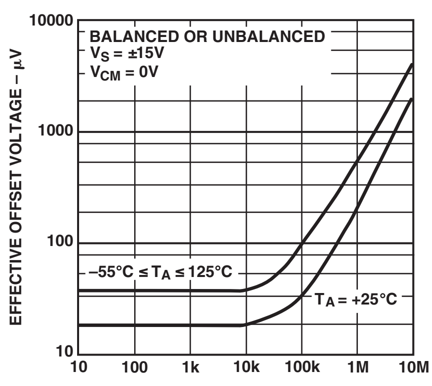
TPC 5. Input Bias, Offset Current vs. Temperature



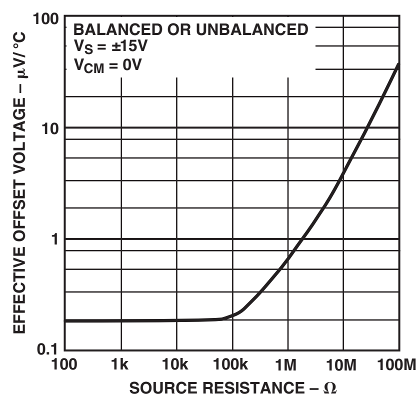
TPC 6. Input Bias Current vs. Common-Mode Voltage



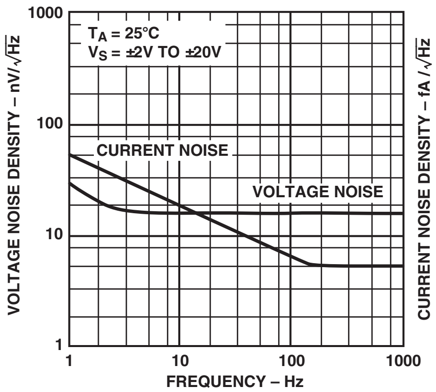
TPC 7. Input Offset Voltage Warm-Up Drift



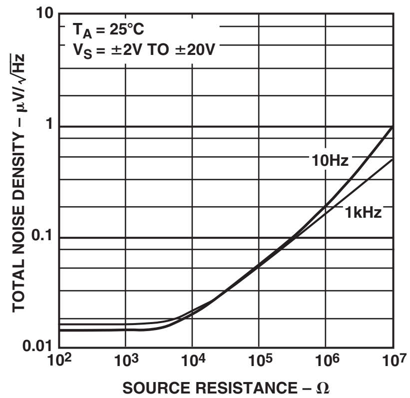
TPC 8. Effective Offset Voltage vs. Source Resistance



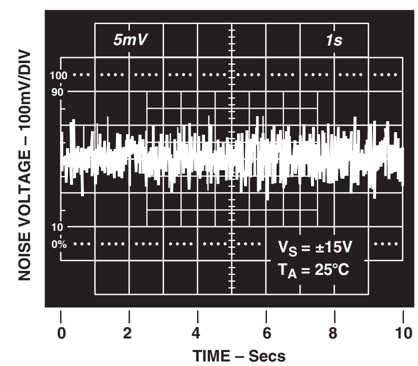
TPC 9. Effective TCV_{OS} vs. Source Resistance



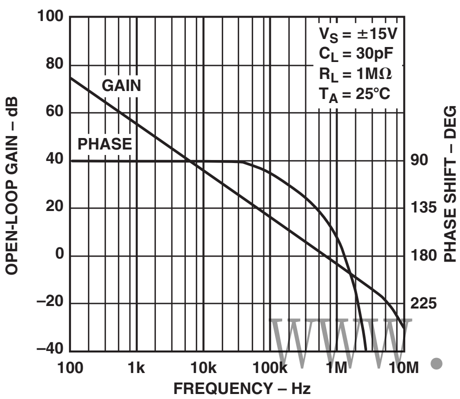
TPC 10. Voltage Noise Density vs. Frequency



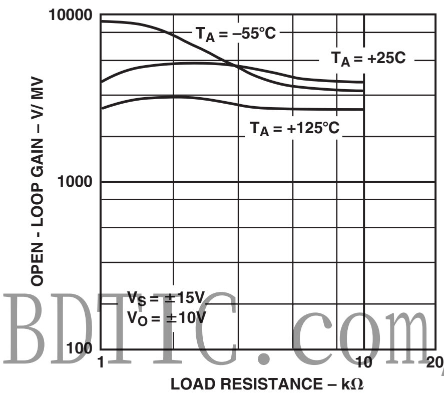
TPC 11. Total Noise Density vs. Source Resistance



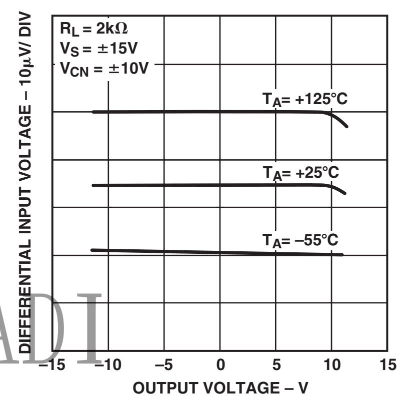
TPC 12. 0.1 Hz to 10 Hz Noise Voltage



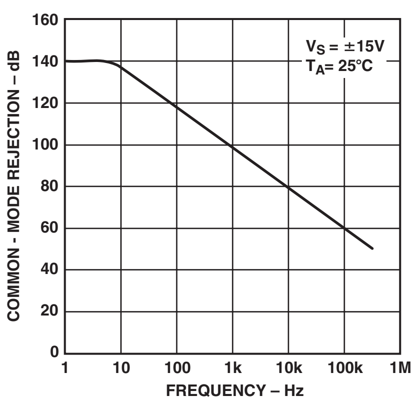
TPC 13. Open-Loop Gain, Phase vs. Frequency



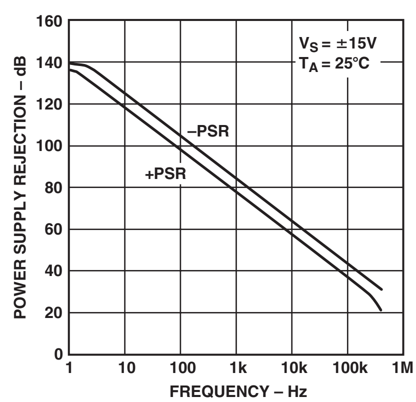
TPC 14. Open-Loop Gain vs. Load Resistance



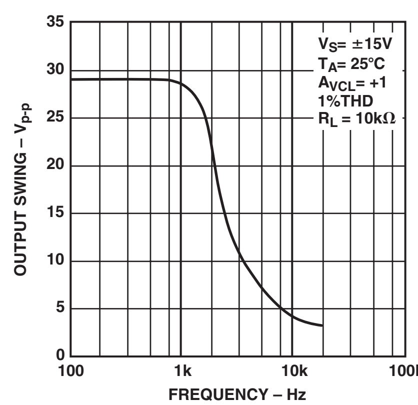
TPC 15. Open-Loop Gain Linearity



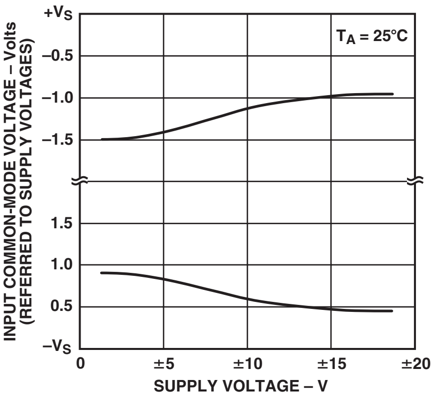
TPC 16. Common-Mode Rejection vs. Frequency



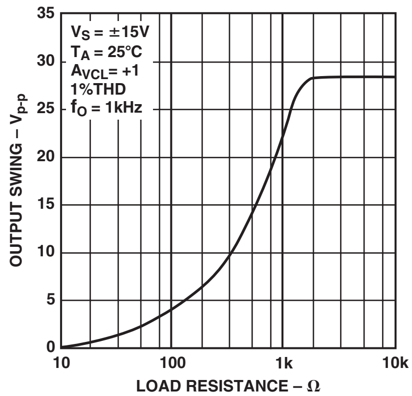
TPC 17. Power Supply Rejection vs. Frequency



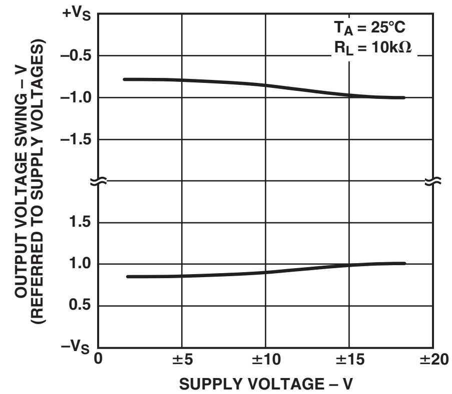
TPC 18. Maximum Output Swing vs. Frequency



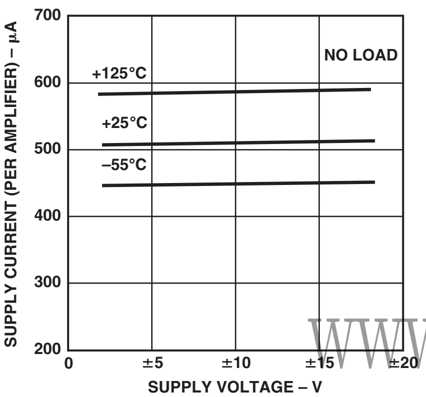
TPC 19. Input Common-Mode Voltage Range vs. Supply Voltage



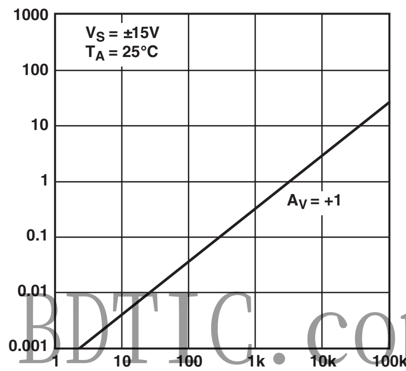
TPC 20. Maximum Output Swing vs. Load Resistance



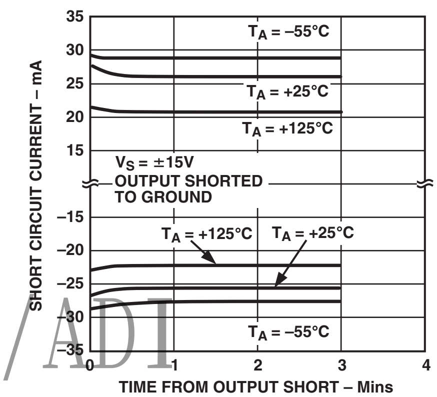
TPC 21. Output Voltage Swing vs. Supply Voltage



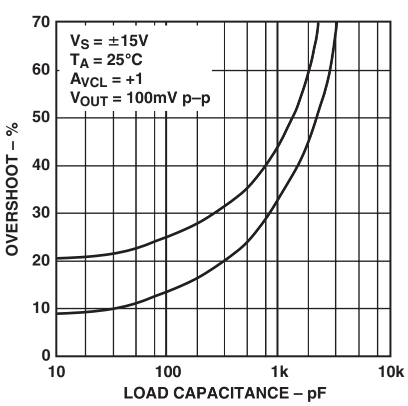
TPC 22. Supply Current (per Amplifier) vs. Supply Voltage



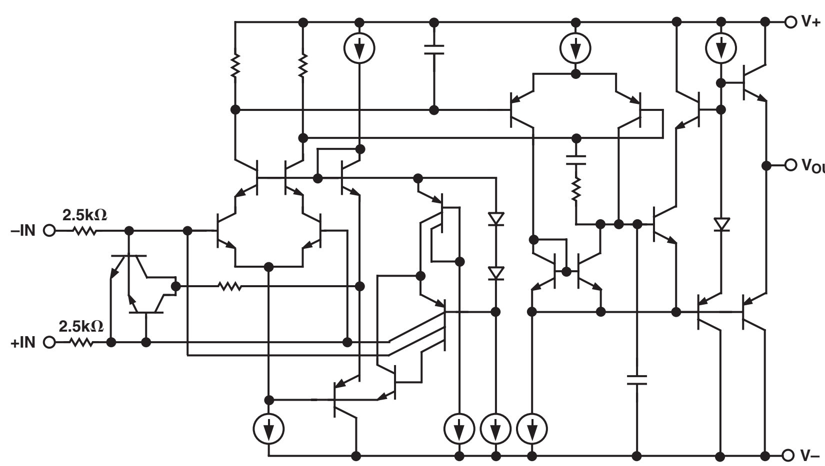
TPC 23. Closed-Loop Output Impedance vs. Frequency



TPC 24. Short-Circuit Current vs. Time Temperature



TPC 25. Small-Signal Overshoot vs. Capacitance Load



TPC 26. Simplified Schematic Showing One Amplifier

APPLICATIONS INFORMATION

Extremely low bias current over the full military temperature range makes the OP497 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the OP497. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the OP497 are protected against large differential voltage by back-to-back diodes and current-limiting resistors. Common-mode voltages at the inputs are not restricted, and may vary over the full range of the supply voltages used.

The OP497 requires very little operating headroom about the supply rails, and is specified for operation with supplies as low as ±2 V. Typically, the common-mode range extends to within 1 V of either rail. The output typically swings to within 1 V of the rails when using a 10 kΩ load.

AC PERFORMANCE

The OP497's ac characteristics are highly stable over its full operating temperature range. Unity-gain small-signal response is shown in Figure 1. Extremely tolerant of capacitive loading on the output, the OP497 displays excellent response even with 1000 pF loads (Figure 2).

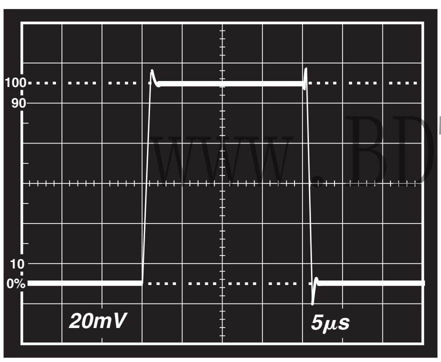


Figure 1. Small-Signal Transient Response (C_{LOAD} = 100 pF, A_{VCL} = 1)

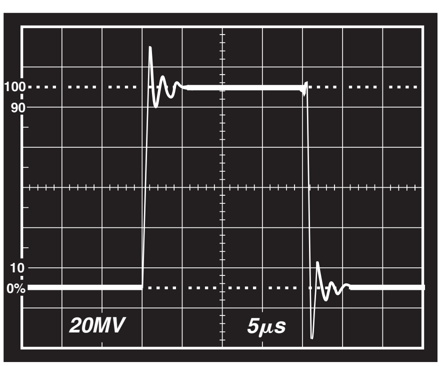


Figure 2. Small-Signal Transient Response (C_{LOAD} = 1000 pF, A_{VCL} = 1)

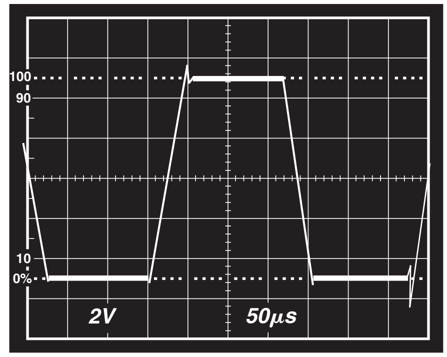


Figure 3. Large-Signal Transient Response (A_{VCL} = 1)

GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP497, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100 pA of leakage currents between adjacent traces, so guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, as shown in Figure 4, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input. In inverting applications, both inputs remain at ground, so the guard trace should be grounded. Guard traces should be on both sides of the circuit board.

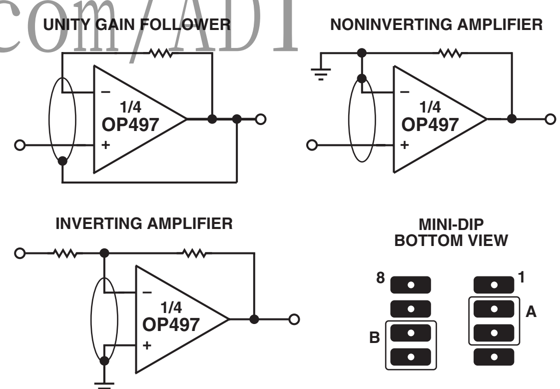


Figure 4. Guard Ring Layout and Connections

OPEN-LOOP GAIN LINEARITY

The OP497 has both an extremely high gain of 2000 V/mv minimum and constant gain linearity. This enhances the precision of the OP497 and provides for very high accuracy in high closed-loop gain applications. Figure 5 illustrates the typical open-loop gain linearity of the OP 497 over the military temperature range.

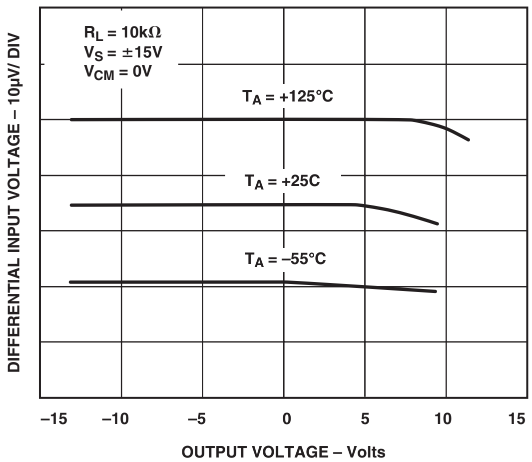


Figure 5. Open-Loop Linearity of the OP497

APPLICATIONS

Precision Absolute Value Amplifier

The circuit of Figure 6 is a precision absolute value amplifier with an input impedance of 30 MΩ. The high gain and low TCV_{OS} of the OP497 ensure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP497 exceeds 120 dB, yielding an error of less than 2 ppm.

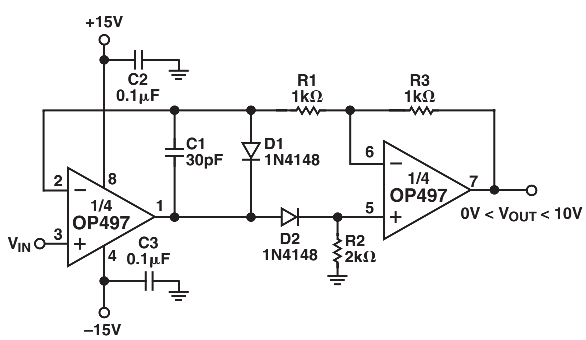


Figure 6. Precision Absolute Value Amplifier

PRECISION CURRENT PUMP

Maximum output current of the precision current pump shown in Figure 7 is ±10 mA. Voltage compliance is ±10 V with ±15 V supplies. Output impedance of the current transmitter exceeds 3 MΩ with linearity better than 16 bits.

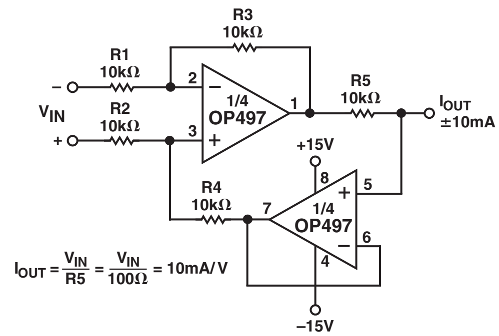


Figure 7. Precision Current Pump

PRECISION POSITIVE PEAK DETECTOR

In Figure 8, the CH must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of CH and the bias current of the OP497.

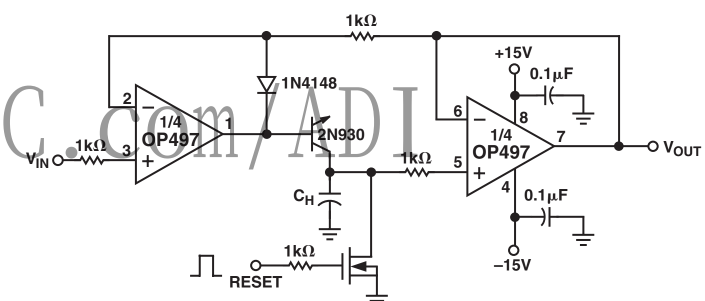


Figure 8. Precision Positive Peak Detector

SIMPLE BRIDGE CONDITIONING AMPLIFIER

Figure 9 shows a simple bridge conditioning amplifier using the OP497. The transfer function is:

$$V_{OUT} = V_{REF}\left(\frac{\Delta R}{R + \Delta R}\right)\frac{R_F}{R}$$

The REF43 provides an accurate and stable reference voltage for the bridge. To maintain the highest circuit accuracy, R_F should be 0.1% or better with a low temperature coefficient.

*Teflon is a registered trademark of the Dupont Company.

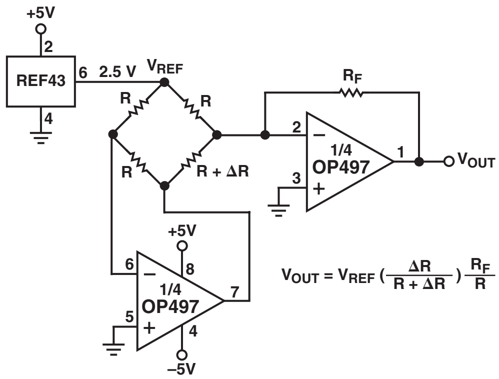


Figure 9. A Simple Bridge Conditioning Amplifier Using the OP497

NONLINEAR CIRCUITS

Due to its low input bias currents, the OP497 is an ideal log amplifier in nonlinear circuits such as the square and square root circuits shown in Figures 10 and 11. Using the squaring circuit of Figure 10 as an example, the analysis begins by writing a voltage-loop equation across transistors Q_1, Q_2, Q_3, and Q_4.

$$V_{T1} In\left(\frac{I_{IN}}{I_{S1}}\right) + V_{T2} In\left(\frac{I_{IN}}{I_{S2}}\right) = V_{T3} In\left(I\frac{I_O}{I_{S3}}\right) + V_{T4} In\left(\frac{I_{REF}}{I_{S4}}\right)$$

All the transistors of the MAT04 are precisely matched and at the same temperature, so the I_S and V_T terms cancel, giving:

$$2InI_{IN} = InI_O + InI_{REF} = In\left(I_O \times I_{REF}\right)$$

Exponentiating both sides of thick equation leads to:

$$I_O = \frac{\left(I_{IN}\right)^2}{I_{REF}}$$

Op amp A_2 forms a current-to-voltage converter which gives $V_{OUT} = R2 \times I_O$. Substituting (V_{IN}/R1) for I_{IN} and the above equation for I_O, yields:

$$V_{OUT} = \left(\frac{R2}{I_{REF}}\right)\left(\frac{V_{IN}}{R1}\right)^2$$

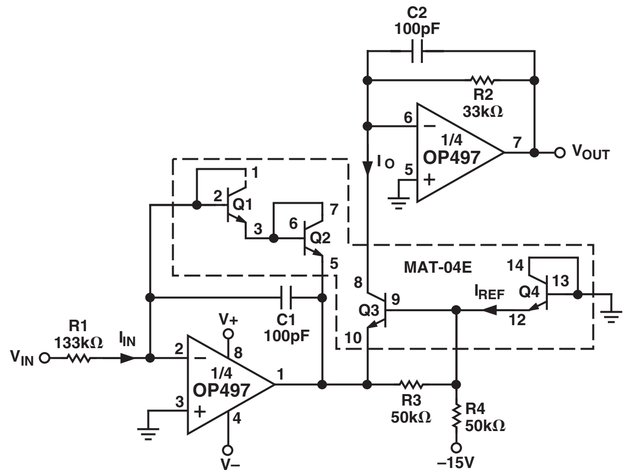


Figure 10. Squaring Amplifier

A similar analysis made for the square-root circuit of Figure 11 leads to its transfer function:

$$V_{OUT} = R2\sqrt{\frac{\left(V_{IN}\right)\left(I_{REF}\right)}{R1}}$$

In these circuits, I_{REF} is a function of the negative power supply. To maintain accuracy, the negative supply should be well regulated. For applications where very high accuracy is required, a voltage reference may be used to set I_{REF}. An important consideration for the squaring circuit is that a sufficiently large input voltage can force the output beyond the operating range of the output op amp. Resistor R4 can be changed to scale I_{REF}, or Rl and R2 can be varied to keep the output voltage within the usable range.

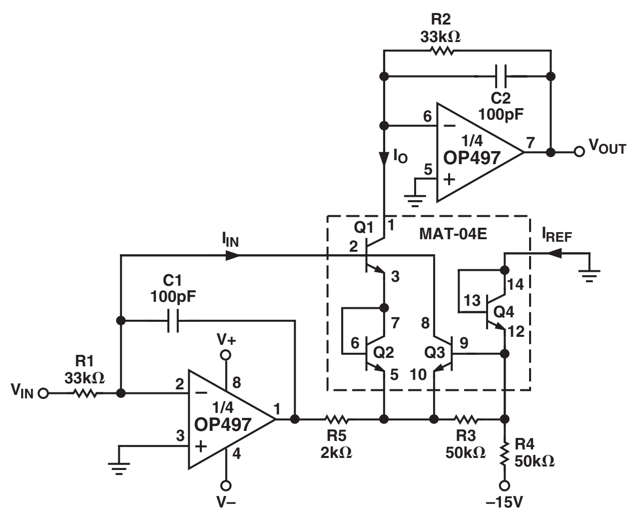


Figure 11. Square-Root Amplifier

Unadjusted accuracy of the square-root circuit is better than 0.1% over an input voltage range of 100 mV to 10 V. For a similar input voltage range, the accuracy of the squaring circuit is better than 0.5%.

OP497 SPICE MACRO-MODEL

Figure 12 and Table I show the node and net list for a SPICE macro-model of the OP497. The model is a simplified version of the actual device and simulates important dc parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O, and I_{SY}. AC parameters such as slew rate, gain and phase response, and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP497. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response of the OP497. In this way, the model presents an accurate ac representation of the actual device. The model assumes an ambient temperature of 25°C.

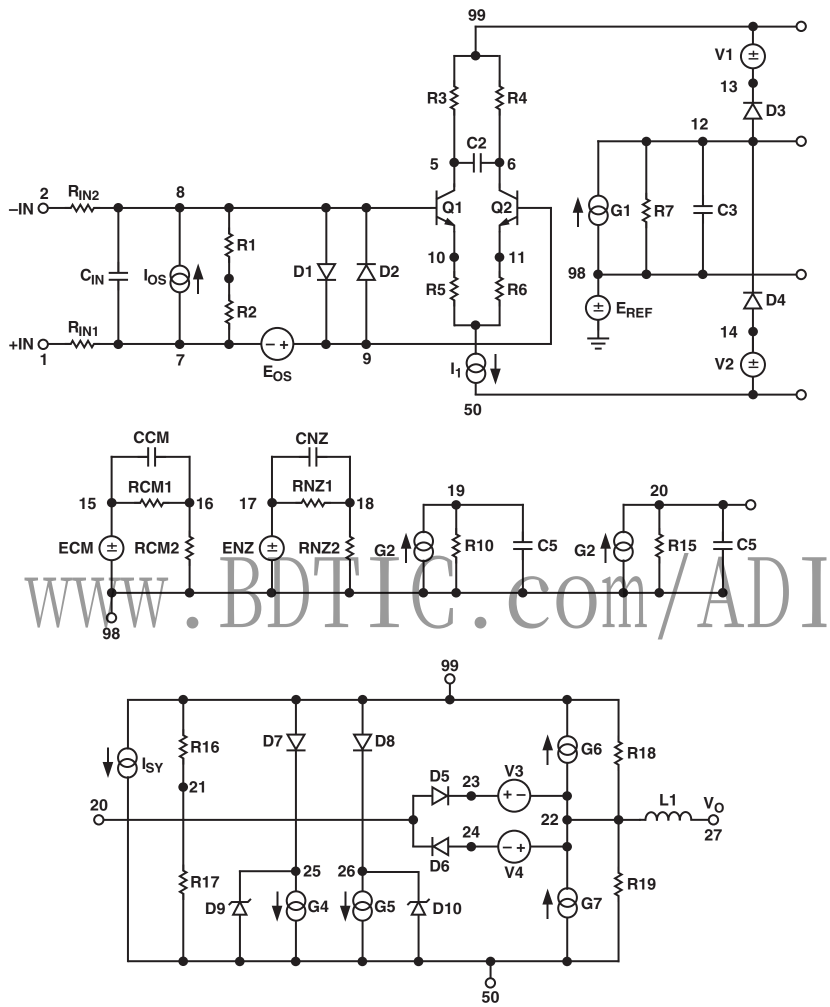


Figure 12. OP497 Macro Model

Table I. OP497 SPICE Net-List

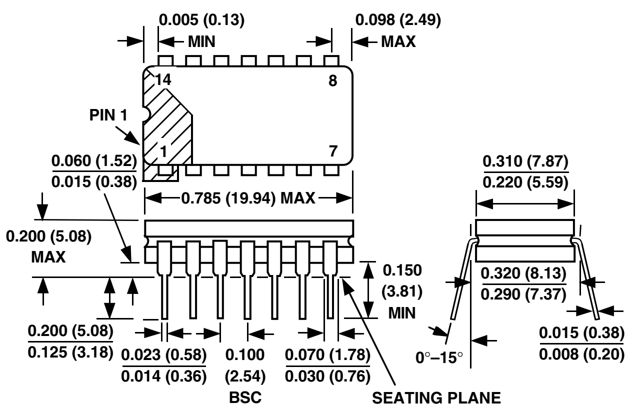
```
* Node assignments
*                         noninverting input
*                               inverting input
*                                       positive supply
*                                               negative supply
*                                                     output
*
*SUBCKT OP497   1     2     99     50    27
*
* INPUT STAGE AND POLE  AT 6 MHz
*
RIN1 1      7      2500
RIN2 2      8      2500
R1   8      3      6.782E8
R2   7      3      6.782E8
R3   5      99     542.57
R4   6      99     542.57
CIN  7      8      3E-12
C2   5      6      24.445E-12
I1   4      50     0.1E-3
IOS  7      8      15E-12
EOS  9      7      POLY(1)  16    21   40E-6        1
Q1   5      8      10   QX
Q2   6      9      11   QX
R5   10     4      25.374
R6   11     4      25.374
D1   8      9      DX
D2   9      8      DX
*
EREF 98     0      21   0     1
*
*GAIN STAGE AND DOMINANT POLE AT 0.11 Hz
*
R7   1      98     2.1703E9
C3   2      98     666.67E-12
G1   98     12     5
V1   99     13     1.275
V2   11     9      1.275
D3   12     13     DX
D4   14     12     DX
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 50 MHz
*
RCM1   15   16     1E6
CCM    15   16     3.18E-9
RCM2   16   98     1
ECM    15   98     3    21    177.83E-3
```

```
* NEGATIVE ZERO AT 1.8 MHz
*
E1     17   98    12   21    1E6
R8     17   18    1E6
C4     17   18    –88.419E-15
R9     18   98    1
*
* POLE AT 6 MHz
*
G2     98   19    18   21    1E-6
R15    20   98    1E6
C8     20   98    26.526E-15
*
* POLE AT 1.8 MHz
*
G6     98   20    19   21    1E-6
R20    20   98    1E6
C10    20   98    88.419E-15
*
* OUTPUT STAGE
*
R16    99   21    160 k
R17    21   50    160 k
ISY    99   50    331E-6
V3     23   22    1.9
D5     20   23    DX
V4     22   24    1.9
D6     24   20    DX
D7     99   25    DX
G4     25   50    20   22    5E-3
D9     50   25    DY
D8     99   26    DX
G5     26   50    22   20    5E-3
D10    50   26    DY
G6     22   99    99   20    5E-3
R18    99   22    200
G7     50   22    20   50    5E-3
R19    22   50    200
L1     22   27    0.1E-6
*
* MODELS USED
*
.MODEL QX NPN (BF = 1.25E6)
.MODEL DX (IS = 1E-15)
.MODEL DZ D(IS = 1E-15 BV = 50)
.ENDS OP497
```

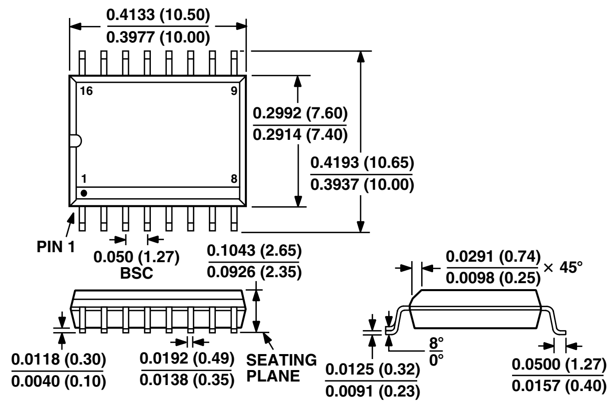
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

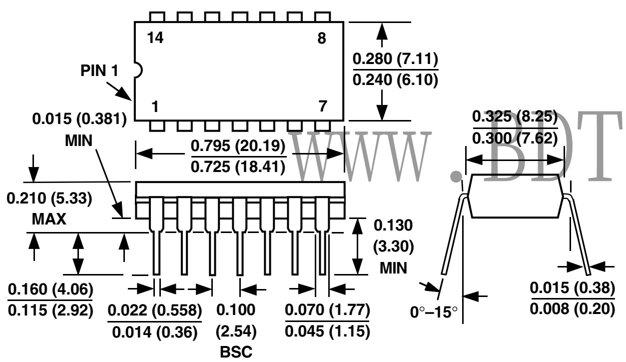
14-Lead Ceramic DIP (Y-Suffix)



16-Lead Wide-Body SOIC (S-Suffix)



14-Lead Epoxy DIP (P-Suffix)



C00309–0–2/02(D)

Revision History

Location	Page
11/01—Data Sheet changed from REV. C to REV. D.	
Edits to PIN CONNECTIONS headings	1
Deleted WAFER TEST LIMITS	3
Edits to ORDERING GUIDE	3
Edits to ABSOLUTE MAXIMUM RATINGS	3
Edits to OUTLINE DIMENSIONS	12

PRINTED IN U.S.A.