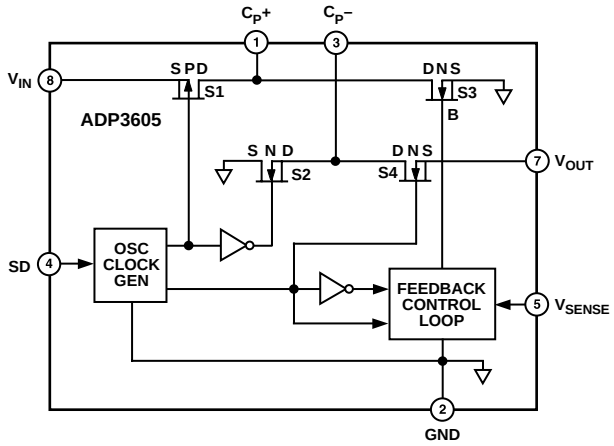
120 mA Switched Capacitor Voltage Inverter with Regulated Output

ADP3605

FEATURES
Fully Regulated Output Voltage (–3 V and Adjustable)
High Output Current: 120 mA
Output Accuracy: ±3%
250 kHz Switching Frequency
Low Shutdown Current: 2 μA Typical
Input Voltage Range from 3 V to 6 V
SO-8 and RU-14 Packages
–40°C to +85°C Ambient Temperature Range

APPLICATIONS
Voltage Inverters
Voltage Regulators
Computer Peripherals and Add-On Cards
Portable Instruments
Battery Powered Devices
Pagers and Radio Control Receivers
Disk Drives
Mobile Phones

FUNCTIONAL BLOCK DIAGRAM

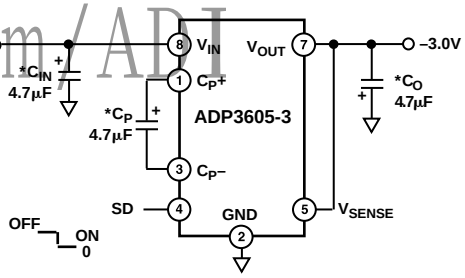


GENERAL DESCRIPTION

The ADP3605 is a 120 mA regulated output switched capacitor voltage inverter. It provides a regulated output voltage with minimum voltage loss and requires a minimum number of external components. In addition, the ADP3605 does not require the use of an inductor.

Pin-for-pin and functionally compatible with the ADP3604, the internal oscillator of the ADP3605 runs at 500 kHz nominal frequency which produces an output switching frequency of 250 kHz. This allows for the use of smaller charge pump and filter capacitors.

The ADP3605 provides an accuracy of ±3% with a typical shutdown current of 2 μA. It can also operate from a single positive input voltage as low as 3 V. The ADP3605 is offered with the regulation fixed at –3 V or adjustable via external resistors over a –3 V to –6 V range.



*FOR BEST PERFORMANCE, 10μF IS RECOMMENDED
C_P : SPRAGUE, 293D475X0010B2W
C_{IN}, C_O: TOKIN, 1E475ZY5UC205F

Figure 1. Typical Application Circuit

REV. A

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ADP3605–SPECIFICATIONS[1, 2, 3] (V_{IN} = 5.0 V @ T_A = +25°C, C_P = C_O = 4.7 µF unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OPERATING SUPPLY RANGE	V_S		3	5	6	V
SUPPLY CURRENT	I_S	–40°C < T_A < +85°C		3	6	mA
Shutdown Mode		V_{SD} = V_{IN} –40°C < T_A < +85°C		2	15	µA
OUTPUT VOLTAGE[4]	V_O	I_O = 60 mA	–3.09	–3.0	–2.91	V
		I_O = 10 mA–120 mA, –40°C ≤ T_A ≤ +85°C 4.75 V ≤ V_S ≤ 6.0 V	–3.15	–3	–2.85	V
LOAD REGULATION	$\Delta V_O/I_O$	I_O = 10 mA–60 mA		0.3		mV/mA
		I_O = 10 mA–120 mA		0.25		mV/mA
OUTPUT RESISTANCE						
Open Loop	R_O			9		Ω
OUTPUT RIPPLE VOLTAGE	V_{RIPPLE}	C_{IN} = C_O = 4.7 µF,				
		I_{LOAD} = 60 mA		38		mV
		I_{LOAD} = 120 mA		75		mV
SWITCHING FREQUENCY	F_S	V_{IN} = 5 V –40°C < T_A < +85°C	212	250	288	kHz
SHUTDOWN						
Logic Input High	V_{IH}		2.4			V
Input Current	I_{IH}			1		µA
Logic Input Low	V_{IL}				0.4	V
Input Current	I_{IL}			1		µA

NOTES
[1]Capacitors C_{IN}, C_O and C_P in the test circuit are 4.7 µF with 0.1 Ω ESR.
[2]See Figure 1 Conditions.
[3]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[4]For the adjustable device, a 1% resistor should be used to maintain output voltage tolerance. For both device types, tolerances can be improved by >1% using larger value and lower ESR capacitors for C_O and C_P.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

Input Voltage (V+ to GND, GND to OUT) . . . . . +7.5 V
Input Voltage (V+ to OUT) . . . . . +11 V
Output Short Circuit Protection . . . . . 1 sec
Power Dissipation, SO-8 . . . . . 660 mW
θ_{JA}[2] . . . . . 150°C/W
Power Dissipation, RU-14 . . . . . 600 mW
θ_{JA}[2] . . . . . 165°C/W
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES
[1]This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.
[2]θ_{JA} is specified for worst case conditions with device soldered on a circuit board.

ORDERING GUIDE

Model	Output Voltage	Package Description	Package Options*
ADP3605AR-3	–3 V	Small Outline	SO-8
ADP3605AR	ADJ	Small Outline	SO-8
ADP3605ARU-3	–3 V	Thin Shrink Small Outline Package (TSSOP)	RU-14

*Contact the factory for the availability of other output voltage options.

Table I. Other Members of ADP36xx Family[1]

Model	Output Current	Package Option[2]	Comments
ADP3603AR	50 mA	SO-8	Nom.–3 ± 3% Inverter
ADP3604AR	120 mA	SO-8	Nom.–3 ± 3% Inverter
ADP3610ARU	320 mA	TSSOP-16	Nom. 3.3 V_{IN} Doubler

NOTES
[1]See individual data sheets for detailed ordering information.
[2]SO = Small Outline; TSSOP = Thin Shrink Small Outline Package.

Table II. Alternative Capacitor Technologies

Type	Life	High Freq	Temp	Size	Cost
Aluminum Electrolytic Capacitor	Fair	Fair	Fair	Small	Low
Multilayer Ceramic Capacitor	Long	Good	Poor	Fair[1]	High
Solid Tantalum Capacitor	Above Avg	Avg	Avg	Avg	Avg
OS-CON Capacitor	Above Avg	Good	Good	Good	Avg

NOTE
[1]Refer to capacitor manufacturer's data sheet for operation below 0°C.

Table III. Recommended Capacitor Manufacturers

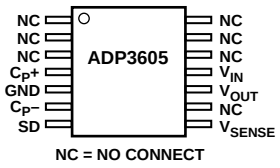
Manufacturer	Capacitor	Capacitor Type
Sprague	672D, 673D, 674D, 678D	Aluminum Electrolytic
Sprague	675D, 173D, 199D	Tantalum
Nichicon	PF and PL	Aluminum Electrolytic
Mallory	TDC and TDL	Tantalum
TOKIN	MLCC	Multilayer Ceramic
MuRata	GRM	Multilayer Ceramic

PIN FUNCTION DESCRIPTIONS

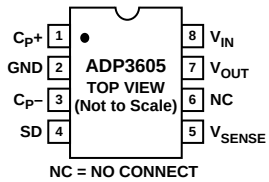
Pin SO-8	Pin TSSOP	Name	Function
1	4	C_P+	Positive Terminal for the Pump Capacitor.
2	5	GND	Device Ground.
3	6	C_P–	Negative Terminal for the Pump Capacitor.
4	7	SD	Logic Level Shutdown Pin. Apply a logic high or connect to V_{IN} to shutdown the device. In shutdown mode, the charge pump is turned off and quiescent current is reduced to 2 µA (typical). Apply a logic low or connect to ground for normal operation.
5	8	V_{SENSE}	Output Voltage Sense Line. This is used to improve load regulation by eliminating IR drop on the high current carrying output traces. For normal operation, connect V_{SENSE} to V_{OUT}. See Application section for more detail.
6	1, 2, 3, 9, 12, 13, 14	NC	No Connection.
7	10	V_{OUT}	Regulated Negative Output Voltage. Connect a low ESR, 4.7 µF or larger capacitor between this pin and device GND.
8	11	V_{IN}	Positive Supply Input Voltage. Connect a low ESR bypass capacitor between this pin and device ground to minimize supply transients.

PIN CONFIGURATIONS

RU-14



SO-8



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3605 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges larger than 600 V HBM. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADP3605–Typical Performance Characteristics

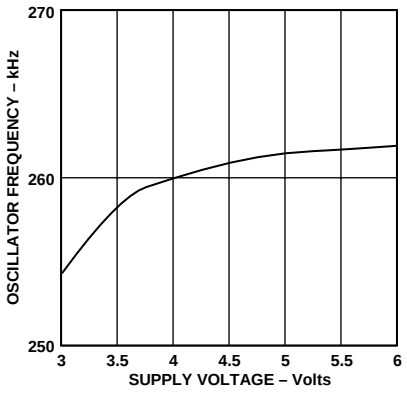


Figure 2. Oscillator Frequency vs. Supply Voltage

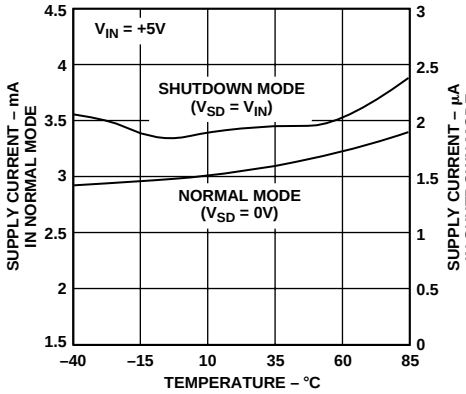


Figure 3. Supply Current vs. Temperature

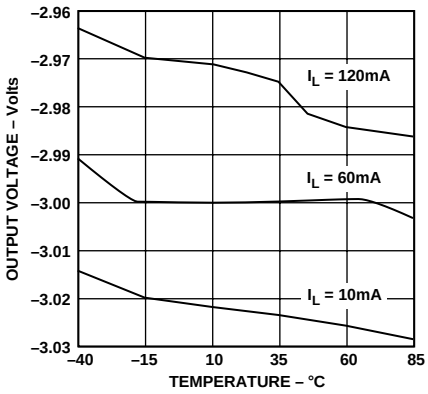


Figure 4. Output Voltage vs. Temperature

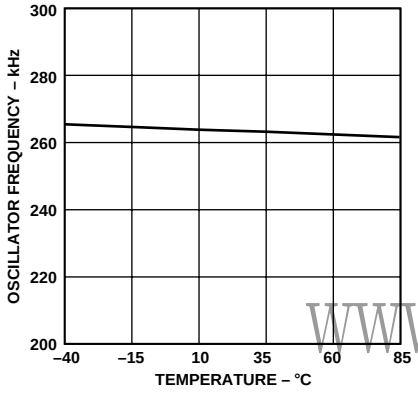


Figure 5. Oscillator Frequency vs. Temperature

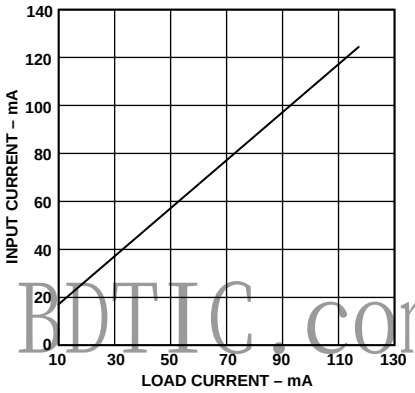


Figure 6. Average Input Current vs. Output Current

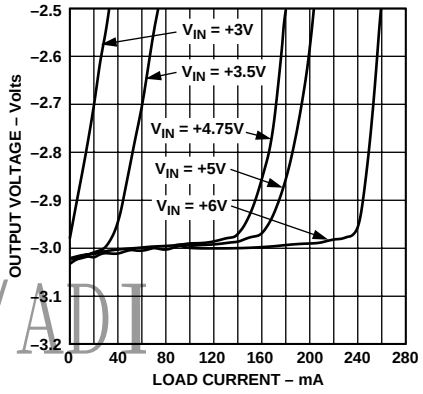


Figure 7. Output Voltage vs. Load Current

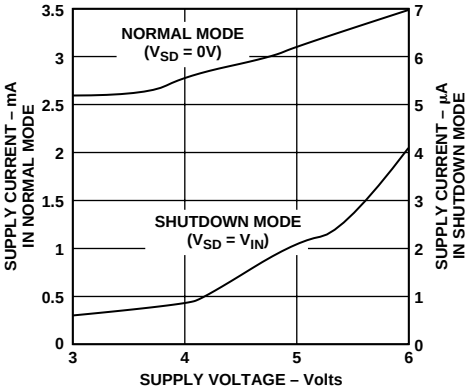


Figure 8. Supply Current vs. Supply Voltage

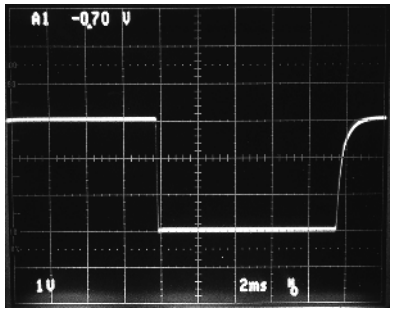


Figure 9 . Start-Up Under Full Load

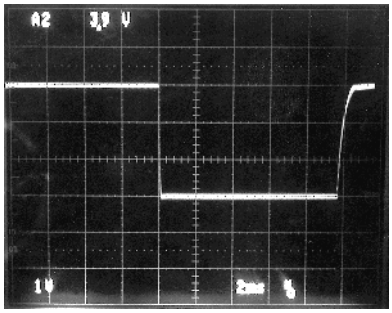


Figure 10. Enable/Disable Time Under Full Load

THEORY OF OPERATION

The ADP3605 uses a switched capacitor principle to generate a negative voltage from a positive input voltage. An onboard oscillator generates a two phase clock to control a switching network that transfers charge between the storage capacitors. The switches turn on and off at a 250 kHz rate, which is generated from an internal 500 kHz oscillator. The basic principle behind the voltage inversion scheme is illustrated in Figures 11 and 12.

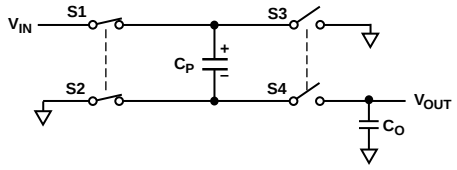


Figure 11. ADP3605 Switch Configuration Charging the Pump Capacitor

During phase one, S1 and S2 are ON, charging the pump capacitor to the input voltage. Before the next phase begins, S1 and S2 are turned OFF as well as S3 and S4 to prevent any overlap. S3 and S4 are turned ON during the second phase (see Figure 12) and charge stored in the pump capacitor is transferred to the output capacitor.

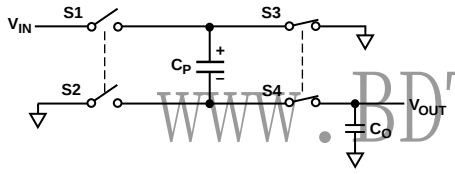


Figure 12. ADP3605 Switch Configuration Charging the Output Capacitor

During the second phase, the positive terminal of the pump capacitor is connected to ground through variable resistance switch, S3, and the negative terminal is connected to the output, resulting in a voltage inversion at the output terminal. The ADP3605 block diagram is shown on the front page.

APPLICATION INFORMATION

Capacitor Selection

The ADP3605's high internal oscillator frequency permits the use of small capacitors for both the pump and the output capacitors. For a given load current, factors affecting the output voltage performance are:

- Pump (C_P) and output (C_O) capacitance.
- ESR of the C_P and C_O.

When selecting the capacitors, keep in mind that not all manufacturers guarantee capacitor ESR in the range required by the circuit. In general, the capacitor's ESR is inversely proportional to its physical size, so larger capacitance values and higher voltage ratings tend to reduce ESR. Since the ESR is also a function of the operating frequency, when selecting a capacitor, make sure its value is rated at the circuit's operating frequency.

Temperature is another factor affecting capacitor performance. Figure 13 illustrates the temperature effect on various capacitors. If the circuit has to operate at temperatures significantly different from 25°C, the capacitance and ESR values must be carefully selected to adequately compensate for the change. Various capacitor technologies offer improved performance over temperature; for example, certain tantalum capacitors provide good low-temperature ESR but at a higher cost. Table II provides the ratings for different types of capacitor technologies to help the designer select the right capacitors for the application. The exact values of C_{IN} and C_O are not critical. However, low ESR capacitors such as solid tantalum and multilayer ceramic capacitors are recommended to minimize voltage loss at high currents. Table III shows a partial list of the recommended low ESR capacitor manufacturers.

Input Capacitor

A small 1 µF input bypass capacitor, preferably with low ESR, such as tantalum or multilayer ceramic, is recommended to reduce noise and supply transients and supply part of the peak input current drawn by the ADP3605. A large capacitor is recommended if the input supply is connected to the ADP3605 through long leads, or if the pulse current drawn by the device might affect other circuitry through supply coupling.

Output Capacitor

The output capacitor (C_O) is alternately charged to the C_P voltage when C_P is switched in parallel with C_O. The ESR of C_O introduces steps in the V_{OUT} waveform whenever the charge pump charges C_O, which contributes to V_{OUT} ripple. Thus, ceramic or tantalum capacitors are recommended for C_O to minimize ripple on the output. Figure 14 illustrates the output ripple voltage effect for various capacitance and ESR values. Note that as the capacitor value increases beyond the point where the dominant contribution to the output ripple is due to the ESR, no significant reduction in V_{OUT} ripple is achieved by added capacitance. Since output current is supplied solely by the output capacitor, C_O, during one-half of the charge-pump cycle, peak-to-peak output ripple voltage is calculated by using the following formula.

$$V_{RIPPLE} = \frac{I_L}{2 \times F_S \times C_O} + 2 \times I_L \times ESR_{CO}$$

where: I_L = Load Current

F_S = 250 kHz nominal switching frequency

C_O = 10 µF with an ESR of 0.15 Ω

$$V_{RIPPLE} = \frac{120\ mA}{2 \times 250\ kHz \times 10\ \mu F} + 2 \times 120\ mA \times 0.15 = 60\ mV$$

Multiple smaller capacitors can be connected in parallel to yield lower ESR and lower cost. For lighter loads, proportionally smaller capacitors are required. To reduce high frequency noise, bypass the output with a 0.1 µF ceramic capacitor in parallel with the output capacitor.

Pump Capacitor

The ADP3605 alternately charges C_P to the input voltage when C_P is switched in parallel with the input supply, and then transfers charge to C_O when C_P is switched in parallel with C_O.

During the time C_P is charging, the peak current is approximately two times the output current.

During the time C_P is delivering charge to C_O, the supply current drops down to about 3 mA.

A low ESR capacitor has much greater impact on performance for C_P than C_O since current through C_P is twice the C_O current. Therefore, the voltage drop due to C_P is about four times the ESR of C_P times the load current. While the ESR of C_O affects the output ripple voltage, the voltage drop generated by the ESR of C_P, combined with the voltage drop due to the output source resistance, determines the maximum available V_{OUT}.

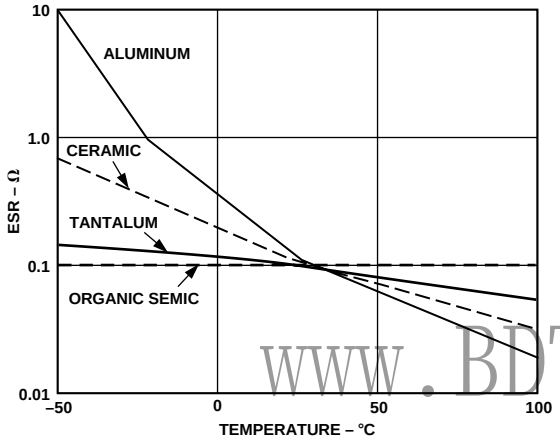


Figure 13. ESR vs. Temperature

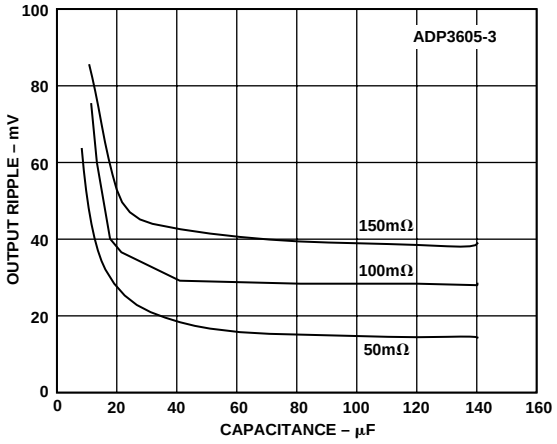


Figure 14. Output Ripple Voltage (mV) vs. Capacitance and ESR

Improved Load Regulation

In most applications, the IR drop from printed circuit board traces is not critical. V_{SENSE} should be connected to the output at a convenient PCB location close to the load. However, if a reduction in IR drop or improvement in load regulation is desired, the sense line can be used to monitor the output voltage at the load. To avoid excessive noise pickup, keep the V_{SENSE} line as short as possible and away from any noisy line.

Shutdown Mode

The ADP3605's output can be disabled by pulling the SD pin (Pin 4) high to a TTL/CMOS logic compatible level which will stop the internal oscillator. In shutdown mode, the quiescent current is reduced to 2 µA (typical). Applying a digital low level or tying the SD Pin to ground will turn on the output. If the shutdown feature is not used, Pin 4 should be tied to the ground pin.

Power Dissipation

The power dissipation of the ADP3605 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature rating. Total power dissipation is calculated as follows:

$$P = (V_{IN} - |V_{OUT}|)\, I_{OUT} + (V_{IN})\, I_S$$

Where I_{OUT} and I_S are output current and supply current, V_{IN} and V_{OUT} are input and output voltages respectively.

For example: assuming worst case conditions, V_{IN} = 6 V, V_{OUT} = –2.9 V, I_{OUT} = 120 mA and I_S = 5 mA. Calculated device power dissipation is:

$$P \approx (6\ V - |-2.9\ V|)(0.12) + (6\ V)(0.005\ A) = 402\ mW$$

This is far below the 660 mW power dissipation capability of the ADP3605 in SO-8 or 600 mW in RU-14

General Board Layout Guidelines

Since the ADP3605's internal switches turn on and off very fast, good PC board layout practices are critical to ensure optimal operation of the device. Improper layouts will result in poor load regulation, especially under heavy loads. Following these simple layout guidelines will improve output performance.

1. Use adequate ground and power traces or planes.
2. Use single point ground for device ground and input and output capacitor grounds.
3. Keep external components as close to the device as possible.
4. Use short traces from the input and output capacitors to the input and output pins respectively.

Maximum Output Voltage

Maximum unregulated output voltage can be obtained on the ADP3605-3 by connecting the V_{SENSE} pin to ground instead of to the V_{OUT} pin. Under this condition, the magnitude of the unregulated output voltage depends on the load current. V_{OUT} is inversely proportional to the load current as illustrated in Figure 15.

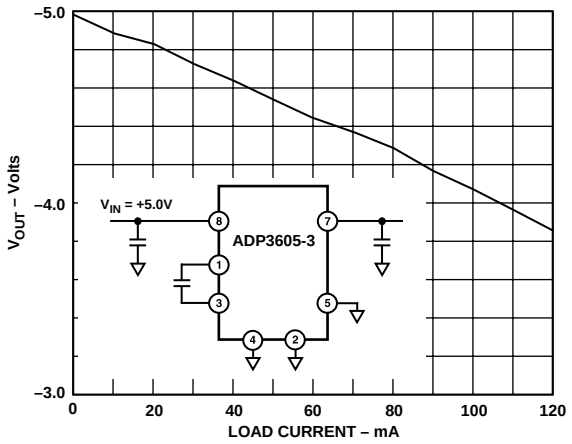


Figure 15. Maximum Unregulated Output Voltage

Regulated Adjustable Output Voltage

For the adjustable version of the ADP3605, the regulated output voltage is programmed by a resistor which is inserted between the V_{SENSE} and V_{OUT} pins, as illustrated in Figure 16. The inherent limit of the output voltage of a single inverting charge pump stage is –1 times the input voltage. The inverse (i.e., negative) scaling factor of 1.00 is reduced somewhat due to losses that increase with output current. To increase the scaling factor to attain a more negative output voltage, an external pump stage can be added with just passive components as shown in Figure 17. That single stage increases the inverse scaling factor to a limit of two, although the diode drops will limit the ability to attain that exact 2.00 scaling factor noticeably. Even further increases can be achieved with more external pump stages.

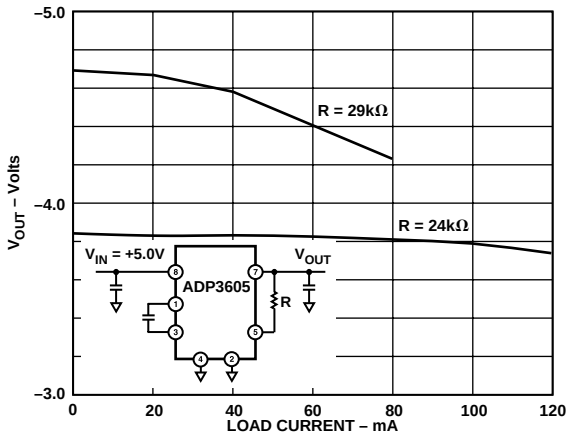


Figure 16. Adjustable Regulated Output Voltage

High accuracy on the adjustable output voltage is achieved with the use of precision trimmed internal resistors, which eliminates the need to trim the external resistor or add a second resistor to form a divider. The adjustable output voltage is set using the following formula:

$$V_{OUT} = -\frac{1.5}{9.5\,k\Omega}R$$

where V_{OUT} is in volts and R is in kΩ.

Regulated Dual Supply System

The circuit in Figure 18 provides regulated positive and negative voltages for systems that require dual supplies from a single battery or power supply.

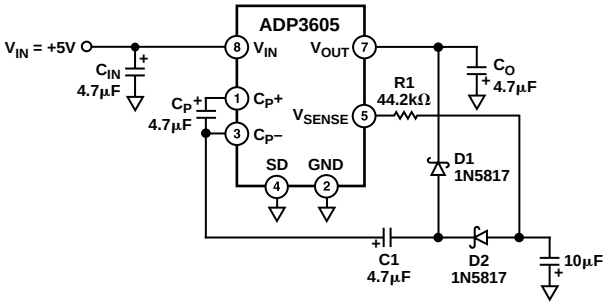


Figure 17. Regulated –7 V from a 5 V Input

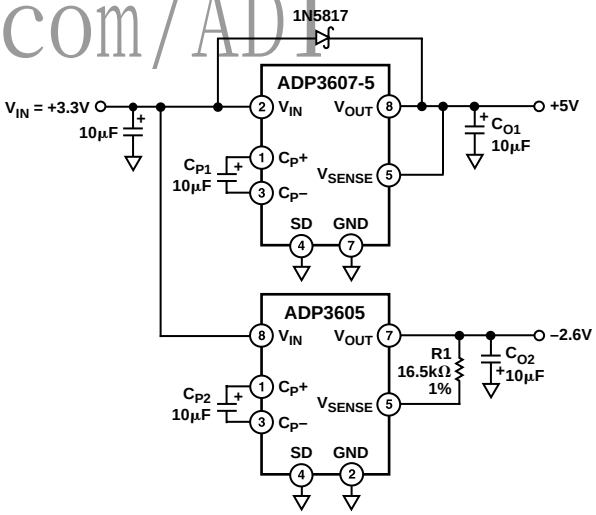
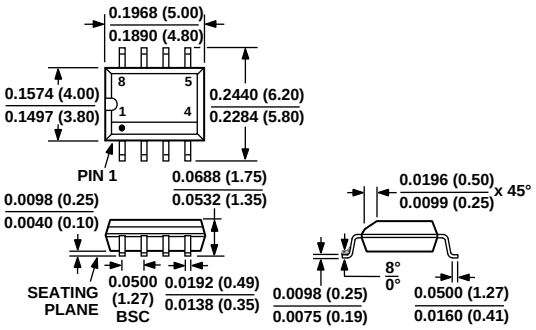


Figure 18. Dual Supply System

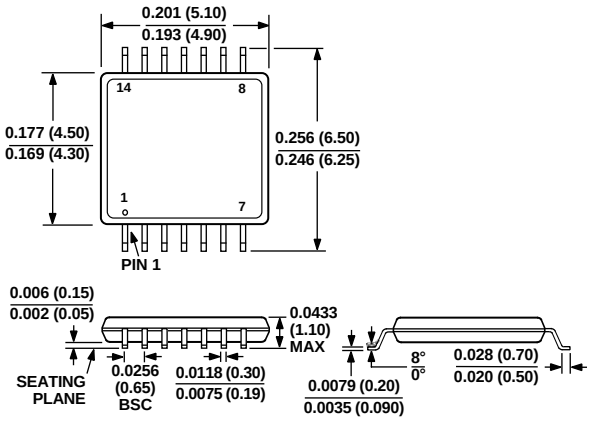
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Small Outline IC (SO-8)



14-Lead Thin Shrink Small Outline Package (TSSOP) (RU-14)



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