

### FEATURES

- ±15 kV ESD protection on receiver input pins
- 400 Mbps (200 MHz) switching rates
- Flow-through pin configuration simplifies PCB layout
- 150 ps channel-to-channel skew (typical)
- 100 ps differential skew (typical)
- 2.7 ns maximum propagation delay
- 3.3 V power supply
- High impedance outputs on power-down
- Low power design (3 mW quiescent typical)
- Interoperable with existing 5 V LVDS drivers
- Accepts small swing (310 mV typical) differential input signal levels
- Supports open, short, and terminated input fail-safe
- 0 V to -100 mV threshold region
- Conforms to TIA/EIA-644 LVDS standard
- Industrial operating temperature range of -40°C to +85°C
- Available in 16-lead surface-mount SOIC and 16-lead low profile TSSOP package

### APPLICATIONS

- Point-to-point data transmission
- Multidrop buses
- Clock distribution networks
- Backplane receivers

### GENERAL DESCRIPTION

The ADN4668 is a quad-channel CMOS, low voltage differential signaling (LVDS) line receiver offering data rates of over 400 Mbps (200 MHz) and ultralow power consumption. It features a flow-through pin configuration for easy PCB layout and separation of input and output signals.

The device accepts low voltage (310 mV typical) differential input signals and converts them to a single-ended, 3 V TTL/CMOS logic level.

### FUNCTIONAL BLOCK DIAGRAM

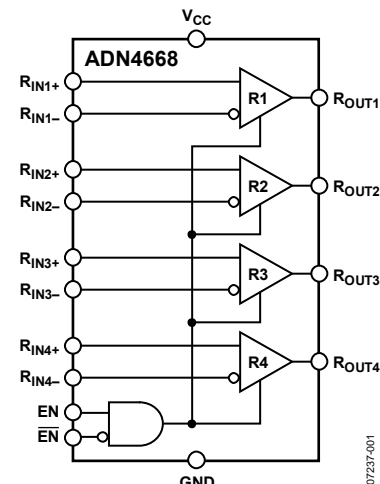


Figure 1.

The ADN4668 also offers active-high and active-low enable/disable inputs (EN and  $\overline{\text{EN}}$ ) that control all four receivers. They disable the receivers and switch the outputs to a high impedance state.

This high impedance state allows the outputs of one or more ADN4668s to be multiplexed together and reduces the quiescent power consumption to 3 mW typical.

The ADN4668 and its companion driver, the ADN4667, offer a new solution to high speed, point-to-point data transmission and a low power alternative to emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL).

#### Rev. A

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REVISION HISTORY

7/08—Rev. 0 to Rev. A	
Added 16-Lead SOIC_N.....	Universal
Changes to Table 1.....	3
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

3/08—Revision 0: Initial Version

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## SPECIFICATIONS

$V_{DD} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $C_L = 15\text{ pF}$  to GND, all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1, 2</sup>

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
LVDS INPUTS ( $R_{INX+}$ , $R_{INX-}$ )					
Differential Input High Threshold, $V_{TH}$ at $R_{INX+}$ , $R_{INX-}$ <sup>3</sup>		−35	0	mV	$V_{CM} = 1.2\text{ V}$ , 0.05 V, 2.95 V
Differential Input Low Threshold, $V_{TL}$ at $R_{INX+}$ , $R_{INX-}$ <sup>3</sup>	−100	−35		mV	$V_{CM} = 1.2\text{ V}$ , 0.05 V, 2.95 V
Common-Mode Voltage Range, $V_{CMR}$ at $R_{INX+}$ , $R_{INX-}$ <sup>4</sup>	0.1		2.3	V	$V_{ID} = 200\text{ mV p-p}$
Input Current, $I_{IN}$ at $R_{INX+}$ , $R_{INX-}$	−10	±5	+10	μA	$V_{IN} = 2.8\text{ V}$ , $V_{CC} = 3.6\text{ V}$ or 0 V
	−10	±1	+10	μA	$V_{IN} = 0\text{ V}$ , $V_{CC} = 3.6\text{ V}$ or 0 V
	−20	±1	+20	μA	$V_{IN} = 3.6\text{ V}$ , $V_{CC} = 0\text{ V}$
LOGIC INPUTS					
Input High Voltage, $V_{IH}$	2.0		$V_{CC}$	V	
Input Low Voltage, $V_{IL}$	GND		0.8	V	
Input Current, $I_{IN}$	−10	±5	+10	μA	$V_{IN} = 0\text{ V}$ or $V_{CC}$ , other input = $V_{CC}$ or GND
Input Clamp Voltage, $V_{CL}$	−1.5	−0.8		V	$I_{CL} = -18\text{ mA}$
OUTPUTS ( $R_{OUTx}$ )					
Output High Voltage, $V_{OH}$	2.7	3.3		V	$I_{OH} = -0.4\text{ mA}$ , $V_{ID} = 200\text{ mV}$
	2.7	3.3		V	$I_{OH} = -0.4\text{ mA}$ , input terminated
	2.7	3.3		V	$I_{OH} = -0.4\text{ mA}$ , input shorted
Output Low Voltage, $V_{OL}$		0.05	0.25	V	$I_{OL} = 2\text{ mA}$ , $V_{ID} = -200\text{ mV}$
Output Short-Circuit Current, $I_{OS}$ <sup>5</sup>	−15	−47	−100	V	Enabled, $V_{OUT} = 0\text{ V}$
Output Off State Current, $I_{OZ}$	−10	±1	+10	μA	Disabled, $V_{OUT} = 0\text{ V}$ or $V_{CC}$
POWER SUPPLY					
No Load Supply, Current Receivers Enabled, $I_{CC}$		12	15	mA	EN = $V_{CC}$ , inputs open
No Load Supply, Current Receivers Disabled, $I_{CCZ}$	—	—	1—	—	5—
ESD PROTECTION					
$R_{INX+}$ , $R_{INX-}$ Pins		±15		kV	Human body model
All Pins Except $R_{INX+}$ , $R_{INX-}$		±3.5		kV	Human body model

<sup>1</sup> Current-into-device pins are defined as positive. Current-out-of-device pins are defined as negative. All voltages are referenced to ground, unless otherwise specified.

<sup>2</sup> All typicals are given for  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>3</sup>  $V_{CC}$  is always higher than the  $R_{INX+}$  and  $R_{INX-}$  voltage.  $R_{INX-}$  and  $R_{INX+}$  have a voltage range of  $-0.2\text{ V}$  to  $V_{CC} - V_{ID}/2$ . However, to be compliant with ac specifications, the common voltage range is 0.1 V to 2.3 V.

<sup>4</sup>  $V_{CMR}$  is reduced for larger  $V_{ID}$ . For example, if  $V_{ID} = 400\text{ mV}$ ,  $V_{CMR}$  is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0 V to 2.4 V but is supported only with inputs shorted and no external common-mode voltage applied.  $V_{ID}$  up to  $V_{CC} - 0\text{ V}$  can be applied to the  $R_{INX+}/R_{INX-}$  inputs with the common-mode voltage set to  $V_{CC}/2$ . Propagation delay and differential pulse skew decrease when  $V_{ID}$  is increased from 200 mV to 400 mV. Skew specifications apply for  $200\text{ mV} \leq V_{ID} \leq 800\text{ mV}$  over the common-mode range.

<sup>5</sup> Output short-circuit current ( $I_{OS}$ ) is specified as magnitude only; a minus sign indicates direction only. Only one output should be shorted at a time; do not exceed the maximum junction temperature specification.

## AC CHARACTERISTICS

$V_{DD} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $C_L = 15 \text{ pF to GND}$ , all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1, 2, 3, 4</sup>

Table 2.

Parameter <sup>5</sup>	Min	Typ	Max	Unit	Conditions/Comments <sup>6</sup>
Differential Propagation Delay, High-to-Low, $t_{PHLD}$	1.2	2.0	2.7	ns	$C_L = 15 \text{ pF}$ , <sup>7</sup> $V_{ID} = 200 \text{ mV}$ , see Figure 2 and Figure 3
Differential Propagation Delay, Low-to-High, $t_{PLHD}$	1.2	1.9	2.7	ns	$C_L = 15 \text{ pF}$ , <sup>7</sup> $V_{ID} = 200 \text{ mV}$ , see Figure 2 and Figure 3
Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $ , $t_{SKD1}$ <sup>8</sup>	0	0.1	0.4	ns	$C_L = 15 \text{ pF}$ , <sup>7</sup> $V_{ID} = 200 \text{ mV}$ , see Figure 2 and Figure 3
Differential Channel-to-Channel Skew, Same Device, $t_{SKD2}$ <sup>3</sup>	0	0.15	0.5	ns	$C_L = 15 \text{ pF}$ , <sup>7</sup> $V_{ID} = 200 \text{ mV}$ , see Figure 2 and Figure 3
Differential Part-to-Part Skew, $t_{SKD3}$ <sup>4</sup>			1.0	ns	$C_L = 15 \text{ pF}$ , <sup>7</sup> $V_{ID} = 200 \text{ mV}$ , see Figure 2 and Figure 3
Differential Part-to-Part Skew, $t_{SKD4}$ <sup>9</sup>			1.5	ns	$C_L = 15 \text{ pF}$ , <sup>7</sup> $V_{ID} = 200 \text{ mV}$ , see Figure 2 and Figure 3
Rise Time, $t_{TLH}$		0.5	1.0	ns	$C_L = 15 \text{ pF}$ , <sup>7</sup> $V_{ID} = 200 \text{ mV}$ , see Figure 2 and Figure 3
Fall Time, $t_{THL}$		0.35	1.0	ns	$C_L = 15 \text{ pF}$ , <sup>7</sup> $V_{ID} = 200 \text{ mV}$ , see Figure 2 and Figure 3
Disable Time, High-to-Z, $t_{PHZ}$		8	14	ns	$R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , <sup>7</sup> see Figure 4 and Figure 5
Disable Time, Low-to-Z, $t_{PLZ}$		8	14	ns	$R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , <sup>7</sup> see Figure 4 and Figure 5
Enable Time, Z-to-High, $t_{PZH}$		9	14	ns	$R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , <sup>7</sup> see Figure 4 and Figure 5
Enable Time, Z-to-Low, $t_{PZL}$		9	14	ns	$R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , <sup>7</sup> see Figure 4 and Figure 5
Maximum Operating Frequency, $f_{MAX}$ <sup>10</sup>	200	250		MHz	All channels switching

<sup>1</sup> All typicals are given for  $V_{CC} = 3.3 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

<sup>2</sup> Generator waveform for all tests, unless otherwise specified:  $f = 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , and  $t_R$  and  $t_F$  (0% to 100%)  $\leq 3 \text{ ns}$  for  $R_{INx+}/R_{INx-}$ .

<sup>3</sup> Channel-to-channel skew,  $t_{SKD2}$ , is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.

<sup>4</sup> Part-to-part skew,  $t_{SKD3}$ , is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same  $V_{CC}$  and within  $5^\circ\text{C}$  of each other within the operating temperature range.

<sup>5</sup> AC parameters are guaranteed by design and characterization.

<sup>6</sup> Current-into-device pins are defined as positive. Current-out-of-device pins are defined as negative. All voltages are referenced to ground, unless otherwise specified.

<sup>7</sup>  $C_L$  includes probe and jig capacitance.

<sup>8</sup>  $t_{SKD1}$  is the magnitude difference in the differential propagation delay time between the positive-going edge and the negative-going edge of the same channel.

<sup>9</sup> Part-to-part skew,  $t_{SKD4}$ , is the differential channel-to-channel skew of any event between devices. This specification applies to devices over the recommended operating temperature and voltage ranges and across process distribution.  $t_{SKD4}$  is defined as  $|\text{maximum} - \text{minimum}|$  differential propagation delay.

<sup>10</sup>  $f_{MAX}$  generator input conditions:  $f = 200 \text{ MHz}$ ,  $t_R = t_F < 1 \text{ ns}$  (0% to 100%), 50% duty cycle, differential (1.05 V p-p to 1.35 V p-p). Output criteria: 60%/40% duty cycle,  $V_{OL}$  (maximum = 0.4 V),  $V_{OH}$  (minimum = 2.7 V),  $C_L = 15 \text{ pF}$  (stray plus probes).

## TEST CIRCUITS AND WAVEFORMS

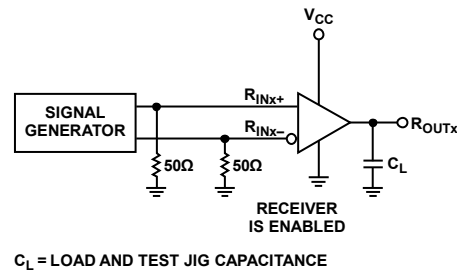


Figure 2. Test Circuit for Receiver Propagation Delay and Transition Time

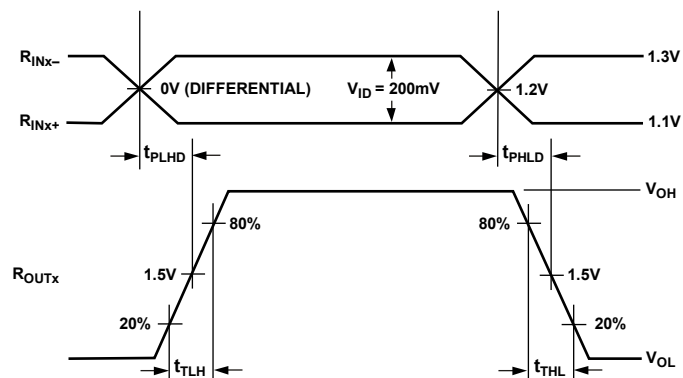
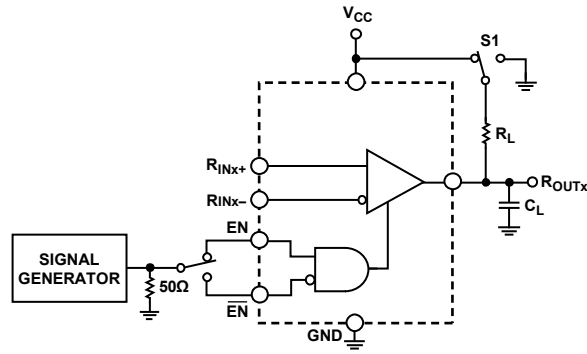


Figure 3. Receiver Propagation Delay and Transition Time Waveforms



NOTES

1.  $C_L$  INCLUDES LOAD AND TEST JIG CAPACITANCE.
2. S1 CONNECTED TO  $V_{CC}$  FOR  $t_{PZL}$  AND  $t_{PLZ}$  MEASUREMENTS.
3. S1 CONNECTED TO GND FOR  $t_{PZH}$  AND  $t_{PHZ}$  MEASUREMENTS.

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Figure 4. Test Circuit for Receiver Enable/Disable Delay

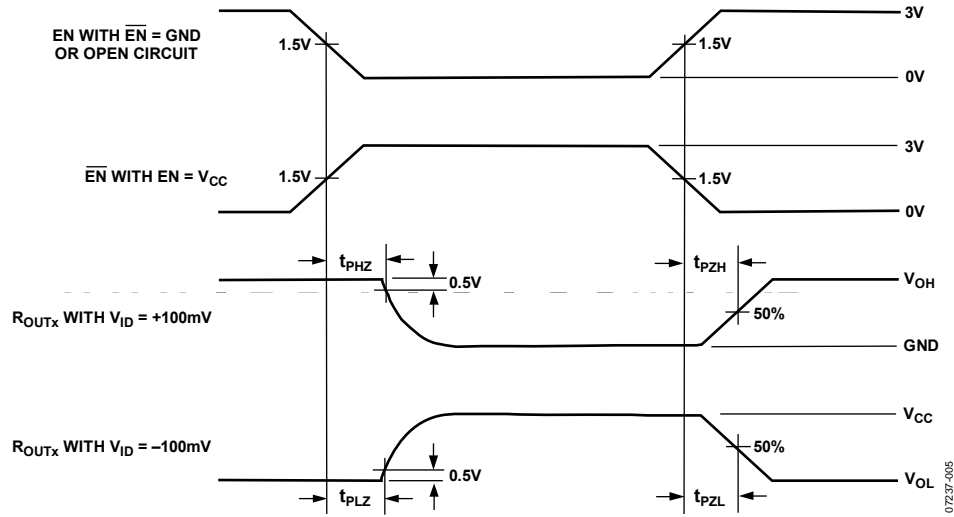


Figure 5. Receiver Enable/Disable Delay Waveforms

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## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{CC}$ to GND	$-0.3\text{ V to }+4\text{ V}$
Input Voltage ( $R_{INX+}$ , $R_{INX-}$ ) to GND	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Enable Input Voltage ( $EN$ , $\overline{EN}$ ) to GND	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Output Voltage ( $R_{OUTx}$ ) to GND	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Operating Temperature Range	
Industrial	$-40^\circ\text{C to }+85^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature ( $T_{J\text{MAX}}$ )	$150^\circ\text{C}$
Power Dissipation	$(T_{J\text{MAX}} - T_A)/\theta_{JA}$
Thermal Impedance, $\theta_{JA}$	
TSSOP Package	$150.4^\circ\text{C/W}$
SOIC Package	$125^\circ\text{C/W} \pm 5^\circ\text{C}$
Reflow Soldering Peak Temperature	
Pb-Free	$260^\circ\text{C} \pm 5^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

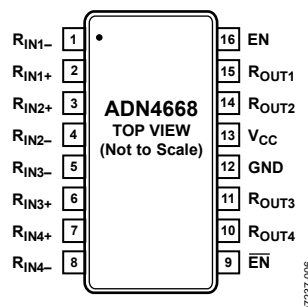


Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R <sub>IN1-</sub>	Receiver Channel 1 Inverting Input. When this input is more negative than R <sub>IN1+</sub> , R <sub>OUT1</sub> is high. When this input is more positive than R <sub>IN1+</sub> , R <sub>OUT1</sub> is low.
2	R <sub>IN1+</sub>	Receiver Channel 1 Noninverting Input. When this input is more positive than R <sub>IN1-</sub> , R <sub>OUT1</sub> is high. When this input is more negative than R <sub>IN1-</sub> , R <sub>OUT1</sub> is low.
3	R <sub>IN2+</sub>	Receiver Channel 2 Noninverting Input. When this input is more positive than R <sub>IN2-</sub> , R <sub>OUT2</sub> is high. When this input is more negative than R <sub>IN2-</sub> , R <sub>OUT2</sub> is low.
4	R <sub>IN2-</sub>	Receiver Channel 2 Inverting Input. When this input is more negative than R <sub>IN2+</sub> , R <sub>OUT2</sub> is high. When this input is more positive than R <sub>IN2+</sub> , R <sub>OUT2</sub> is low.
5	R <sub>IN3-</sub>	Receiver Channel 3 Inverting Input. When this input is more negative than R <sub>IN3+</sub> , R <sub>OUT3</sub> is high. When this input is more positive than R <sub>IN3+</sub> , R <sub>OUT3</sub> is low.
6	R <sub>IN3+</sub>	Receiver Channel 3 Noninverting Input. When this input is more positive than R <sub>IN3-</sub> , R <sub>OUT3</sub> is high. When this input is more negative than R <sub>IN3-</sub> , R <sub>OUT3</sub> is low.
7	R <sub>IN4+</sub>	Receiver Channel 4 Noninverting Input. When this input is more positive than R <sub>IN4-</sub> , R <sub>OUT4</sub> is high. When this input is more negative than R <sub>IN4-</sub> , R <sub>OUT4</sub> is low.
8	R <sub>IN4-</sub>	Receiver Channel 4 Inverting Input. When this input is more negative than R <sub>IN4+</sub> , R <sub>OUT4</sub> is high. When this input is more positive than R <sub>IN4+</sub> , R <sub>OUT4</sub> is low.
9	$\overline{\text{EN}}$	Active-Low Enable and Power-Down Input with Pull-Down (3 V TTL/CMOS). When $\overline{\text{EN}}$ is held high, $\overline{\text{EN}}$ enables the receiver outputs when $\overline{\text{EN}}$ is low or open circuit and puts the receiver outputs into a high impedance state and powers down the device when $\overline{\text{EN}}$ is high.
10	R <sub>OUT4</sub>	Receiver Channel 4 Output (3 V TTL/CMOS). If the differential input voltage between R <sub>IN4+</sub> and R <sub>IN4-</sub> is positive, this output is high. If the differential input voltage is negative, this output is low.
11	R <sub>OUT3</sub>	Receiver Channel 3 Output (3 V TTL/CMOS). If the differential input voltage between R <sub>IN3+</sub> and R <sub>IN3-</sub> is positive, this output is high. If the differential input voltage is negative, this output is low.
12	GND	Ground Reference Point for All Circuitry on the Part.
13	V <sub>CC</sub>	Power Supply Input. These parts can be operated from 3.0 V to 3.6 V.
14	R <sub>OUT2</sub>	Receiver Channel 2 Output (3 V TTL/CMOS). If the differential input voltage between R <sub>IN2+</sub> and R <sub>IN2-</sub> is positive, this output is high. If the differential input voltage is negative, this output is low.
15	R <sub>OUT1</sub>	Receiver Channel 1 Output (3 V TTL/CMOS). If the differential input voltage between R <sub>IN1+</sub> and R <sub>IN1-</sub> is positive, this output is high. If the differential input voltage is negative, this output is low.
16	EN	Active-High Enable and Power-Down Input (3 V TTL/CMOS). When $\overline{\text{EN}}$ is held low or open circuit, EN enables the receiver outputs when EN is high and puts the receiver outputs into a high impedance state and powers down the device when EN is low.

## TYPICAL PERFORMANCE CHARACTERISTICS

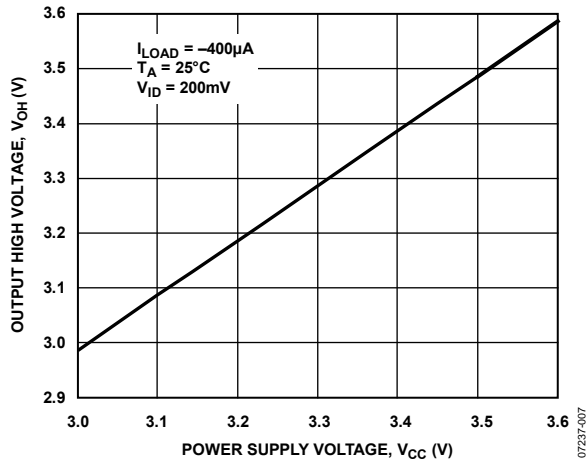


Figure 7. Output High Voltage,  $V_{OH}$  vs. Power Supply Voltage,  $V_{CC}$

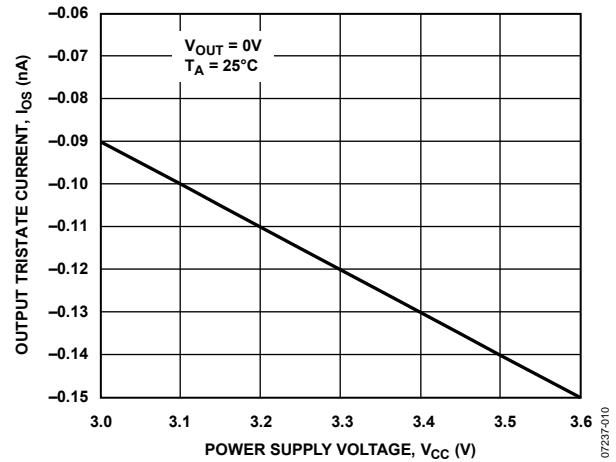


Figure 10. Output Tristate Current,  $I_{OS}$  vs. Power Supply Voltage,  $V_{CC}$

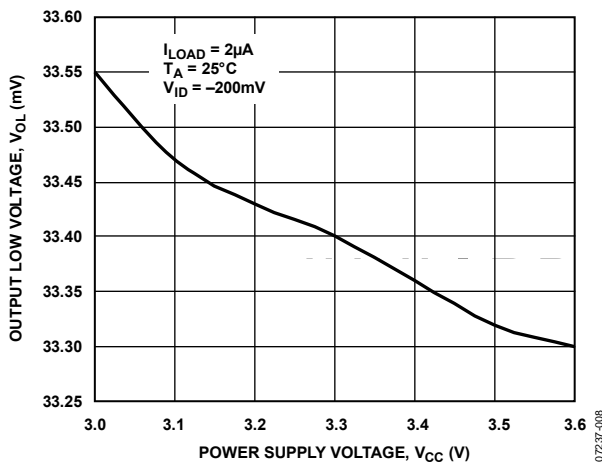


Figure 8. Output Low Voltage,  $V_{OL}$  vs. Power Supply Voltage,  $V_{CC}$

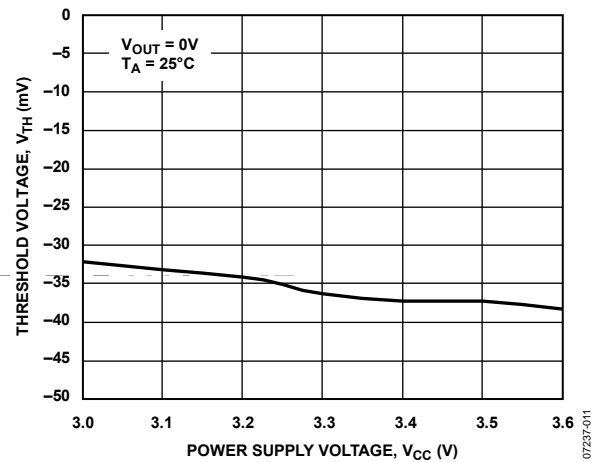


Figure 11. Threshold Voltage,  $V_{TH}$  vs. Power Supply Voltage,  $V_{CC}$

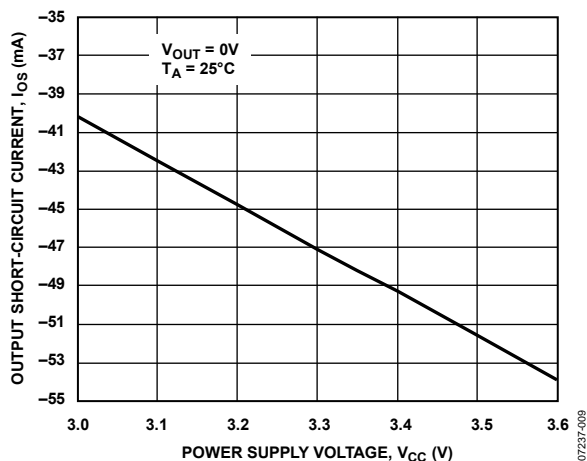


Figure 9. Output Short-Circuit Current,  $I_{OS}$  vs. Power Supply Voltage,  $V_{CC}$

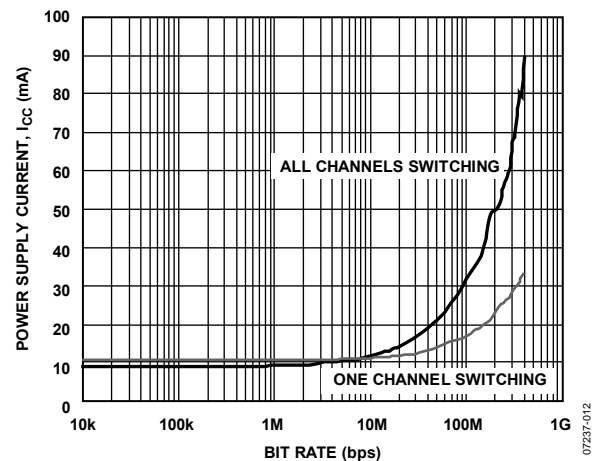
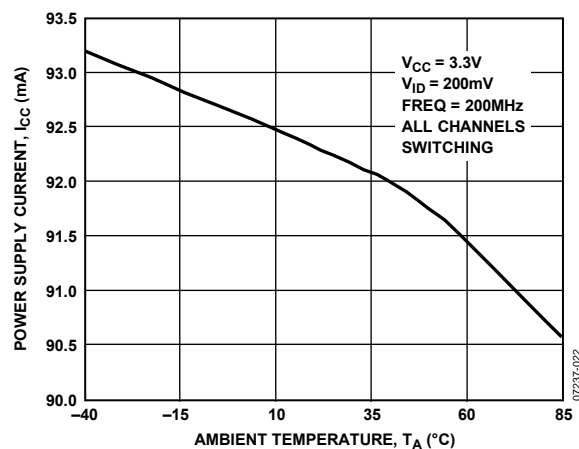
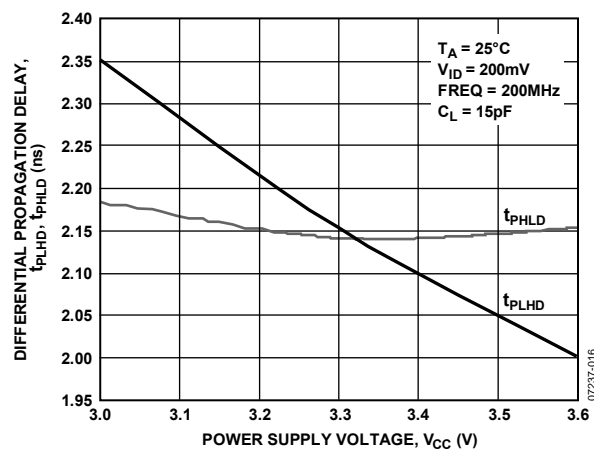
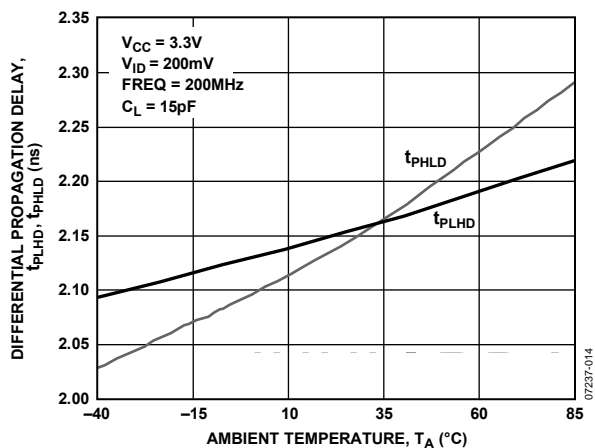
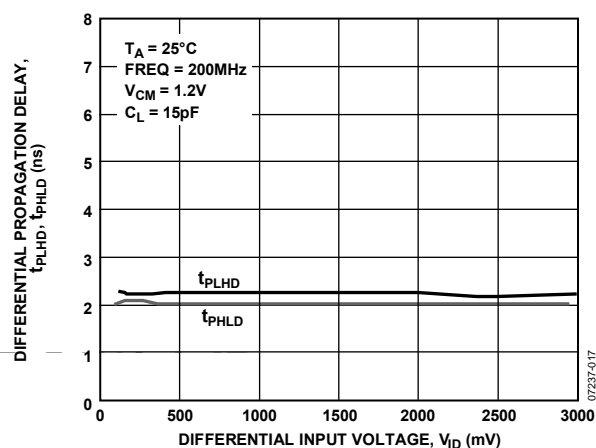
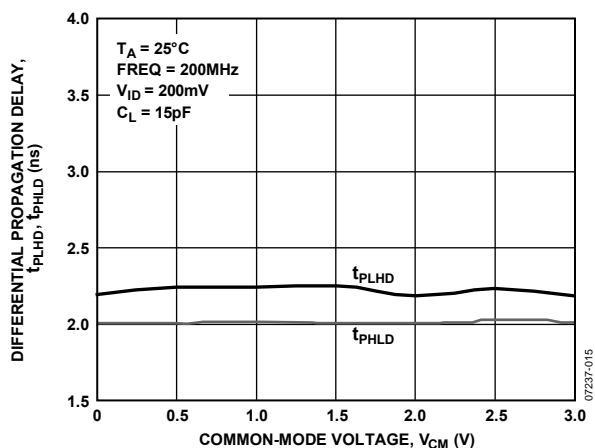
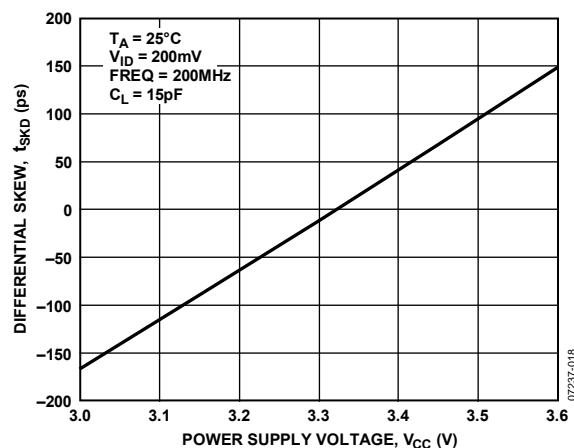


Figure 12. Power Supply Current,  $I_{CC}$  vs. Bit Rate

Figure 13. Power Supply Current,  $I_{CC}$  vs. Ambient Temperature,  $T_A$ Figure 16. Differential Propagation Delay,  $t_{PLHD}, t_{PHLD}$  vs. Power Supply Voltage,  $V_{CC}$ Figure 14. Differential Propagation Delay,  $t_{PLHD}, t_{PHLD}$  vs. Ambient Temperature,  $T_A$ Figure 17. Differential Propagation Delay,  $t_{PLHD}, t_{PHLD}$  vs. Differential Input Voltage,  $V_{ID}$ Figure 15. Differential Propagation Delay,  $t_{PLHD}, t_{PHLD}$  vs. Common-Mode Voltage,  $V_{CM}$ Figure 18. Differential Skew,  $t_{SKD}$  vs. Power Supply Voltage,  $V_{CC}$

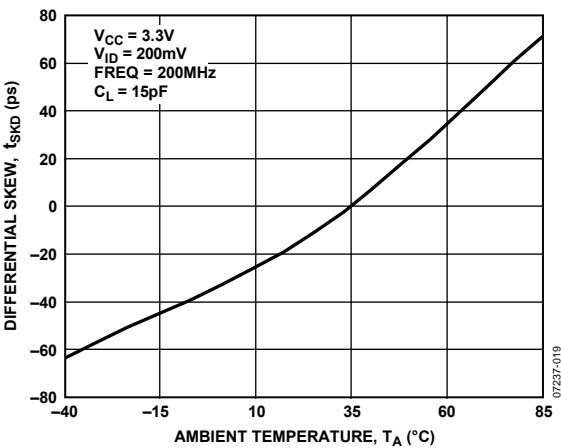


Figure 19. Differential Skew,  $t_{SKD}$  vs. Ambient Temperature,  $T_A$

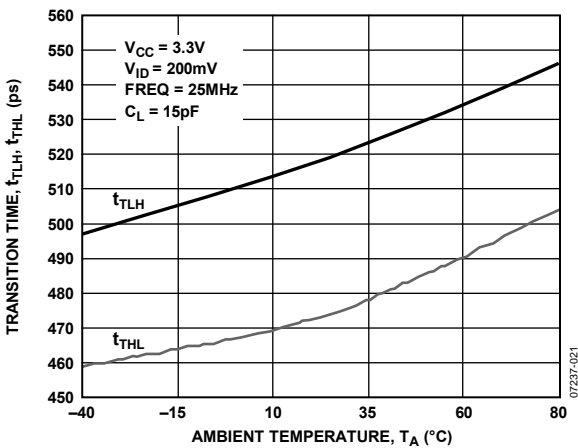


Figure 21. Transition Time,  $t_{TLH}$ ,  $t_{THL}$  vs. Ambient Temperature,  $T_A$

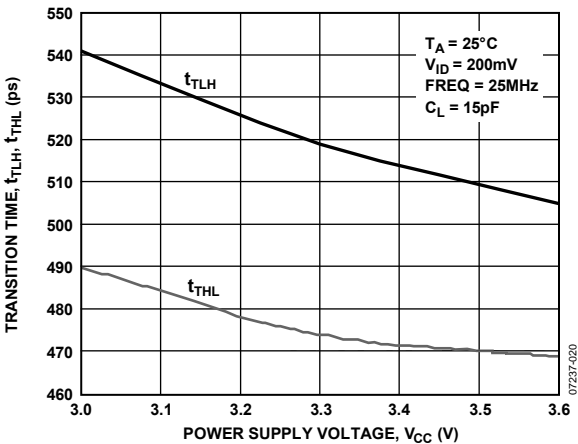


Figure 20. Transition Time,  $t_{TLH}$ ,  $t_{THL}$  vs. Power Supply Voltage,  $V_{CC}$

THEORY OF OPERATION

The ADN4668 is a quad-channel line receiver for low voltage differential signaling. It takes a differential input signal of 310 mV typical and converts it into a single-ended 3 V TTL/CMOS logic signal.

A differential current input signal, received via a transmission medium such as a twisted pair cable, develops a voltage across a terminating resistor,  $R_T$ . This resistor is chosen to match the characteristic impedance of the medium, typically around 100  $\Omega$ . The differential voltage is detected by the receiver and converted back into a single-ended logic signal.

When the noninverting receiver input,  $R_{INx+}$ , is positive with respect to the inverting input,  $R_{INx-}$  (current flows through  $R_T$  from  $R_{INx+}$  to  $R_{INx-}$ ),  $R_{OUTx}$  is high. When the noninverting receiver input,  $R_{INx+}$ , is negative with respect to the inverting input,  $R_{INx-}$  (current flows through  $R_T$  from  $R_{INx-}$  to  $R_{INx+}$ ),  $R_{OUTx}$  is low.

Using the ADN4667 as a driver, the received differential current is between  $\pm 2.5$  mA and  $\pm 4.5$  mA ( $\pm 3.1$  mA typical), developing between  $\pm 250$  mV and  $\pm 450$  mV across a 100  $\Omega$  termination resistor. The received voltage is centered on the receiver offset of 1.2 V. The noninverting receiver input is typically  $(1.2\text{ V} + [310\text{ mV}/2]) = 1.355\text{ V}$ , and the inverting receiver input is  $(1.2\text{ V} - [310\text{ mV}/2]) = 1.045\text{ V}$  for Logic 1. For Logic 0, the inverting and noninverting input voltages are reversed. Note that because the differential voltage reverses polarity, the peak-to-peak voltage swing across  $R_T$  is twice the differential voltage.

Current-mode signaling offers considerable advantages over voltage-mode signaling, such as the RS-422. The operating current remains fairly constant with increased switching frequency, whereas the operating current of voltage-mode drivers increases exponentially in most cases. This increase is caused by the overlap as internal gates switch between high and low, causing currents to flow from  $V_{CC}$  to ground. A current-mode device reverses a constant current between its two outputs, with no significant overlap currents.

This is similar to emitter-coupled logic (ECL) and positive emitter-coupled logic (PECL), but without the high quiescent current of ECL and PECL.

ENABLE INPUTS

The ADN4668 has active-high and active-low enable inputs that put all the logic outputs into a high impedance state when disabled, reducing device current consumption from 9 mA typical to 1 mA typical. See Table 5 for a truth table of the enable inputs.

Table 5. Enable Inputs Truth Table

EN	$\overline{\text{EN}}$	$R_{INx+}$	$R_{INx-}$	$R_{OUTx}$
High	Low or Open	1.045 V	1.355 V	0
High	Low or Open	1.355 V	1.045 V	1
Any other combination of EN and $\overline{\text{EN}}$		X	X	High-Z

APPLICATIONS INFORMATION

Figure 22 shows a typical application for point-to-point data transmission using the ADN4667 as the driver and the ADN4668 as the receiver.

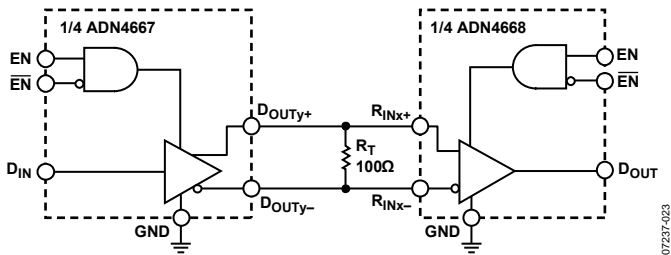
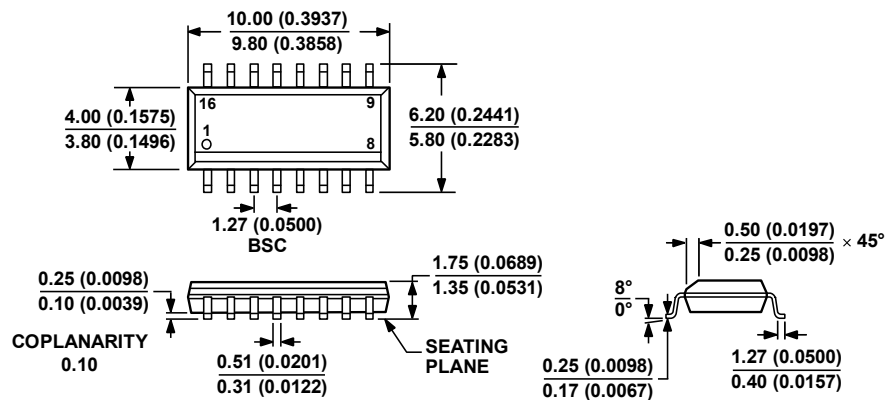


Figure 22. Typical Application Circuit

## OUTLINE DIMENSIONS

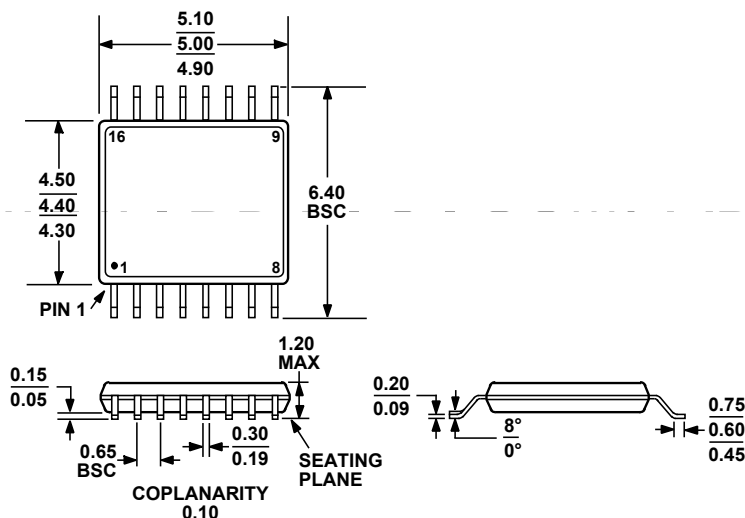


COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 16-Lead Standard Small Outline Package [SOIC\_N]  
(R-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 24. 16-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-16)

Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN4668ARZ <sup>1</sup>	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADN4668ARZ-REEL <sup>1</sup>	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADN4668ARUZ <sup>1</sup>	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADN4668ARUZ-REEL <sup>1</sup>	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

<sup>1</sup> Z = RoHS Compliant Part.