Charge Pump Regulator for Color TFT Panels

ADM8839

FEATURES

- 3 voltages (+5 V, +15 V, −15 V) from a single 3 V supply
- Power efficiency optimized for use with TFT in mobile phones
- Low quiescent current
- Low shutdown current (<5 µA)
- Shutdown function
- Option to use external LDO

APPLICATIONS

- Hand-held instruments
- TFT LCD panels
- Cellular phones

FUNCTIONAL BLOCK DIAGRAM

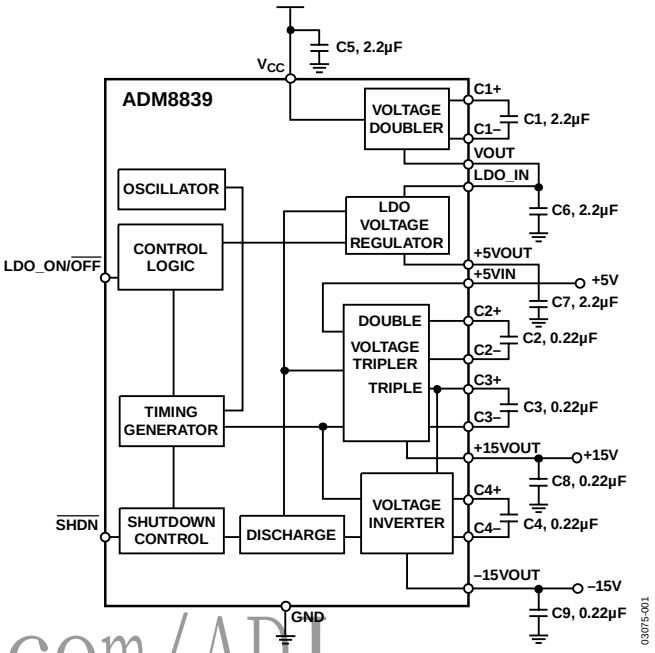

Figure 1.

GENERAL DESCRIPTION

The ADM8839 is a charge pump regulator used for color thin film transistor (TFT) liquid crystal displays (LCDs). Using charge pump technology, the device can be used to generate three voltages (+5 V ± 2%, +15 V, −15 V) from a single 3 V supply. These voltages are then used to provide supplies for the LCD controller (5 V) and the gate drives for the transistors in the panel (+15 V and −15 V). Only a few external capacitors are needed for the charge pumps. An efficient low dropout (LDO) voltage regulator ensures that the power efficiency is high, and provides a low ripple 5 V output. This LDO can be shut down and an external LDO can be used to regulate the 5 V doubler output and drive the input to the charge pump section that generates the +15 V and −15 V outputs, if required by the user.

The ADM8839 has a power save shutdown feature. The 5 V output consumes the most power, so power efficiency is also maximized on this output with an oscillator-enabling scheme (Green Idle™). This effectively senses the load current that is flowing and turns on the charge pump only when charge needs to be delivered to the 5 V pump doubler output.

The ADM8839 is fabricated using CMOS technology for minimal power consumption. The part is packaged in a 20-lead LFCSP (lead frame chip scale package).

Rev. C

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SPECIFICATIONS

V_{CC} = 3 V (+40%/−10%); T_A = −40°C to +85°C; C1, C5, C6, C7 = 2.2 µF; C2, C3, C4, C8, C9 = 0.22 µF; unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE, V_{CC}		2.7		4.2	V
SUPPLY CURRENT, I_{CC}	Unloaded		250	500	µA
	Shutdown mode, T_A = 25°C			5	µA
+5 V OUTPUT					
Output Voltage	I_L = 10 µA to 20 mA	4.9	5.0	5.1	V
Output Current			5	20	mA
Output Ripple	8 mA load		10		mV p-p
Transient Response	I_L stepped from 10 µA to 8 mA		5		µs
+15 V OUTPUT					
Output Voltage	I_L = 1 µA to 150 µA	14.0	15.0	16.0	V
Output Current			1	150	µA
Output Ripple	I_L = 100 µA		50		mV p-p
−15 V OUTPUT					
Output Voltage	I_L = −1 µA to −150 µA	−16.0	−15.0	−14.0	V
Output Current		−150	−1		µA
Output Ripple	I_L = −100 µA		50		mV p-p
POWER EFFICIENCY	R5 V_{OUT} load = 5 mA, ±15 V load = ±150 µA, V_{CC} = 3.0 V		82		%
CHARGE PUMP FREQUENCY		60	100	140	kHz
CONTROL PINS, $\overline{SHDN}$					
Input Voltage, $V_{\overline{SHDN}}$	$\overline{SHDN}$ low = shutdown mode			0.3 × V_{CC}	V
	$\overline{SHDN}$ high = normal mode	0.7 × V_{CC}			V
Digital Input Current				±1	µA
Digital Input Capacitance[1]				10	pF
LDO_ON/OFF					
Input Voltage	Low = External LDO			0.3 × V_{CC}	V
	High = Internal LDO	0.7 × V_{CC}			V
Digital Input Current				±1	µA
Digital Input Capacitance[1]				10	pF

[1] Guaranteed by design. Not 100% production tested.

TIMING SPECIFICATIONS

V_{CC} = 3 V, T_A = 25°C; C1, C5, C6, C7 = 2.2 µF; C2, C3, C4, C8, C9 = 0.22 µF.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-UP SEQUENCE					
+5 V Rise Time, t_{R5V}	10% to 90%, see Figure 14		250		µs
+15 V Rise Time, t_{R15V}	10% to 90%, see Figure 14		3		ms
−15 V Fall Time, t_{FM15V}	90% to 10%, see Figure 14		3		ms
Delay Between −15 V Fall and +15 V, t_{DELAY}	See Figure 14		600		µs
POWER-DOWN SEQUENCE					
+5 V Fall Time, t_{F5V}	90% to 10%, see Figure 14		35		ms
+15 V Fall Time, t_{F15V}	90% to 10%, see Figure 14		10		ms
−15 V Rise Time, t_{RM15V}	10% to 90%, see Figure 14		20		ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	−0.3 V to +6.0 V
Input Voltage on Digital Inputs	−0.3 V to +6.0 V
Output Short-Circuit Duration to GND	10 sec
Output Voltage	
+5 V Output	0 V to 7.0 V
−15 V Output	−17 V to +0.3 V
+15 V Output	−0.3 V to +17 V
Operating Temperature Range	−40°C to +85°C
Power Dissipation	50 mW
Storage Temperature Range	−65°C to +150°C
ESD	Class I

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
20-Lead LFCSP_VQ	31°C	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

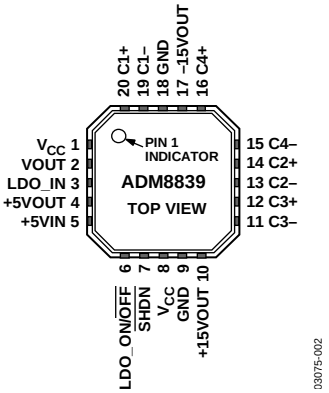


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CC}	Positive Supply Voltage Input. Connect this pin to the 3 V supply with a 2.2 µF decoupling capacitor. Must be electrically tied together with Pin 8 by a PCB trace.
2	VOUT	Voltage Doubler Output. This is derived by doubling the 3 V supply. A 2.2 µF capacitor to ground is required on this pin.
3	LDO_IN	Voltage Regulator Input. The user can bypass this circuit by using the LDO_ON/$\overline{OFF}$ pin.
4	+5VOUT	5 V Output. This is derived by doubling and regulating the 3 V supply. A 2.2 µF capacitor to ground is required on this pin to stabilize the regulator.
5	+5VIN	5 V Input. This is the input to the voltage tripler and inverter charge pump circuits.
6	LDO_ON/$\overline{OFF}$	Control Logic Input. 3 V CMOS logic. A logic high selects the internal LDO for regulation of the 5 V voltage doubler output. A logic low isolates the internal LDO from the rest of the charge pump circuits. This allows the use of an external LDO to regulate the 5 V voltage doubler output. The output of this LDO is then fed back into the voltage tripler and inverter circuits of the ADM8839.
7	$\overline{SHDN}$	Digital Input. 3 V CMOS logic. Active low shutdown control. This shuts down the timing generator and enables the discharge circuit to dissipate the charge on the voltage outputs, thus driving them to 0 V.
8	V_{CC}	Connect this pin to V_{CC}. Must be electrically tied with Pin 1 by a PCB trace.
9	GND	Connect this pin to GND. Must be electrically tied with Pin 18 by a PCB trace.
10	+15VOUT	15 V Output. This is derived by tripling the 5 V regulated output. A 0.22 µF capacitor is required on this pin.
11, 12	C3–, C3+	External Capacitor C3 is connected between these pins. A 0.22 µF capacitor is recommended.
13, 14	C2–, C2+	External Capacitor C2 is connected between these pins. A 0.22 µF capacitor is recommended.
15, 16	C4–, C4+	External Capacitor C4 is connected between these pins. A 0.22 µF capacitor is recommended.
17	−15VOUT	−15 V Output. This is derived by tripling and inverting the 5 V regulated output. A 0.22 µF capacitor is required on this pin.
18	GND	Device Ground. Must be electrically tied with Pin 9 by a PCB trace.
19, 20	C1−, C1+	External Capacitor C1 is connected between these pins. A 2.2 µF capacitor is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

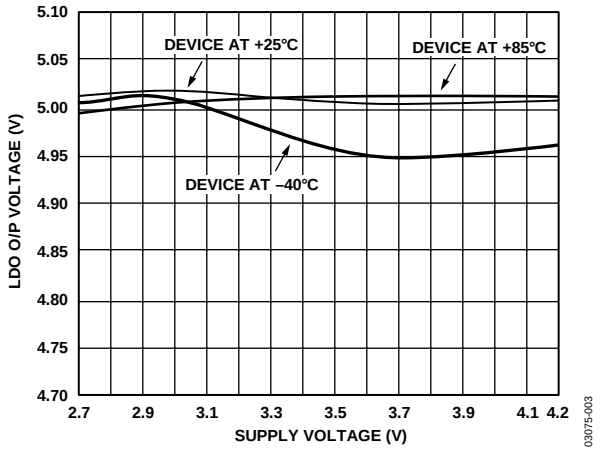


Figure 3. LDO O/P Voltage Variation over Temperature and Supply

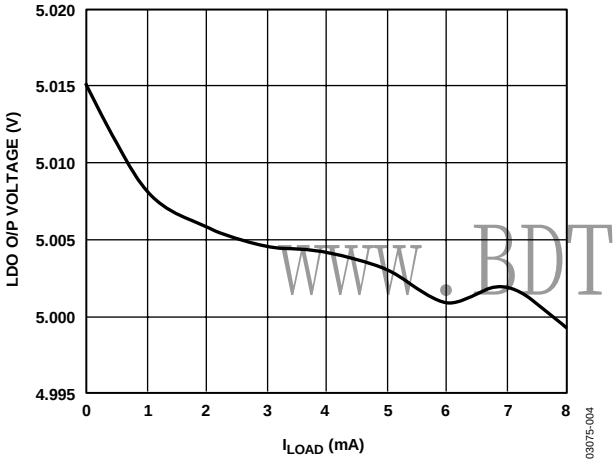


Figure 4. LDO O/P Voltage vs. Load Current

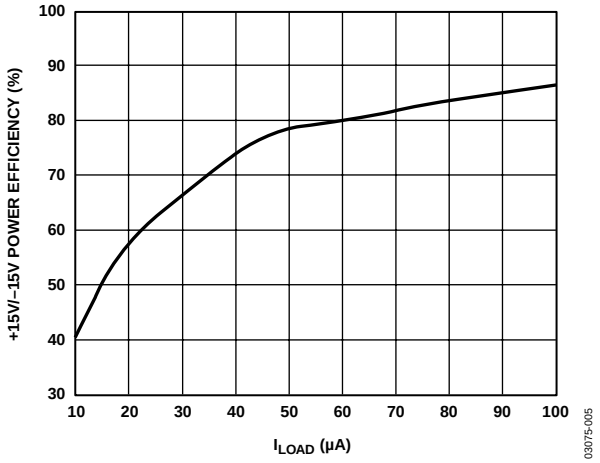


Figure 5. +15 V/−15 V Power Efficiency vs. Load Current

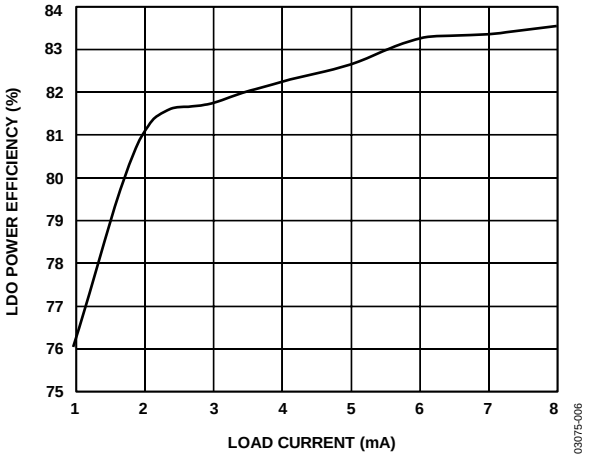


Figure 6. LDO Power Efficiency vs. Load Current, V_{CC} = 3 V

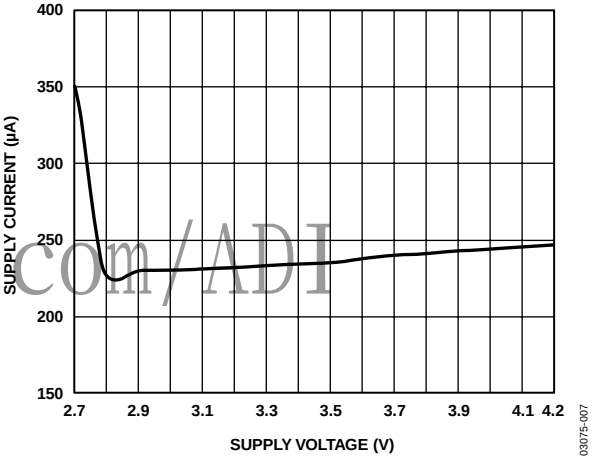


Figure 7. Supply Current vs. Supply Voltage

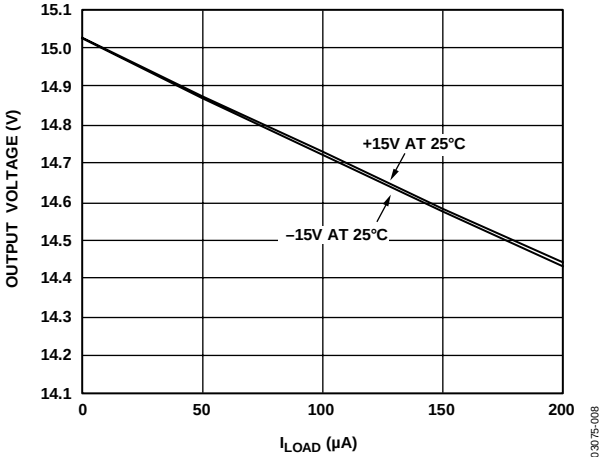


Figure 8. +15 V/−15 V Output Voltage vs. Load Current, Typical Configuration

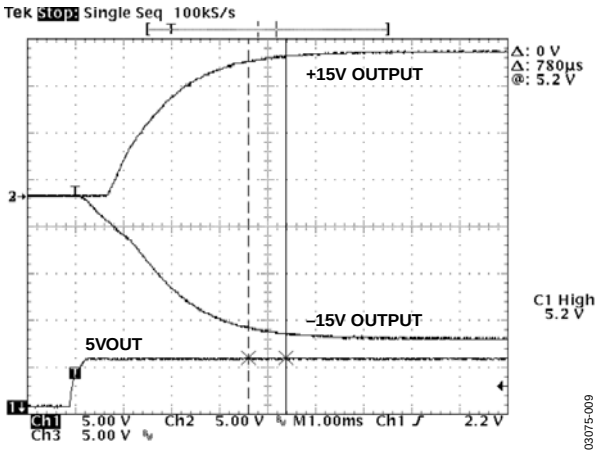


Figure 9. +15 V and −15 V Outputs at Power-Up

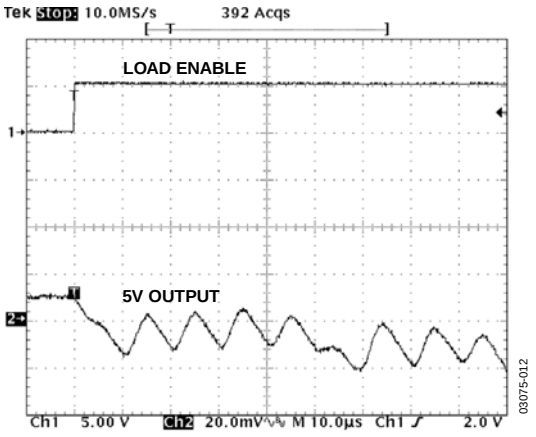


Figure 12. Output Transient Response for Maximum Load Current

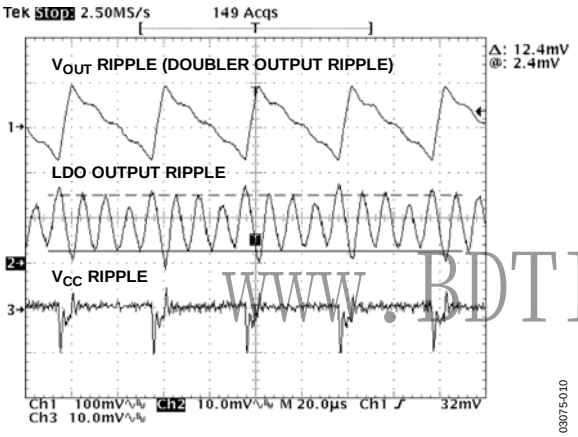


Figure 10. Output Ripple on LDO (5 V Output)

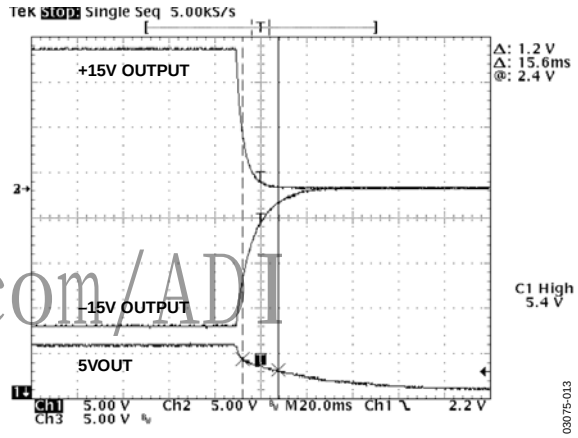


Figure 13. +15 V and −15 V Outputs at Power-Down

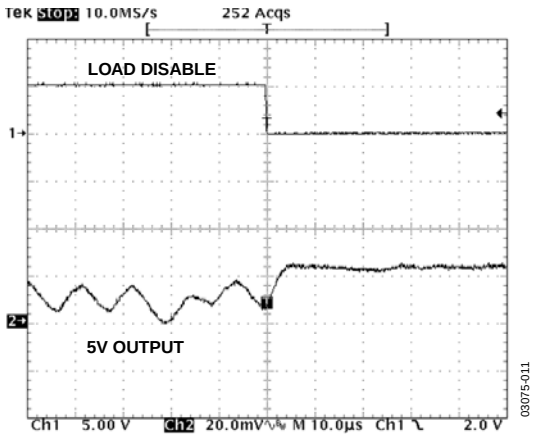


Figure 11. 5 V Output Transient Response, Load Disconnected

THEORY OF OPERATION

POWER SEQUENCING

For the TFT panel to power up correctly, the gate drive supplies must be sequenced such that the −15 V supply is up before the +15 V supply. The ADM8839 controls this sequence. When the device is turned on (a logic high on $\overline{SHDN}$), the ADM8839 allows the −15 V output to ramp immediately but holds off the +15 V output. It continues to do this until the negative output has reached −3 V. At this point, the positive output is enabled and allowed to ramp to +15 V. This sequence is highlighted in Figure 14.

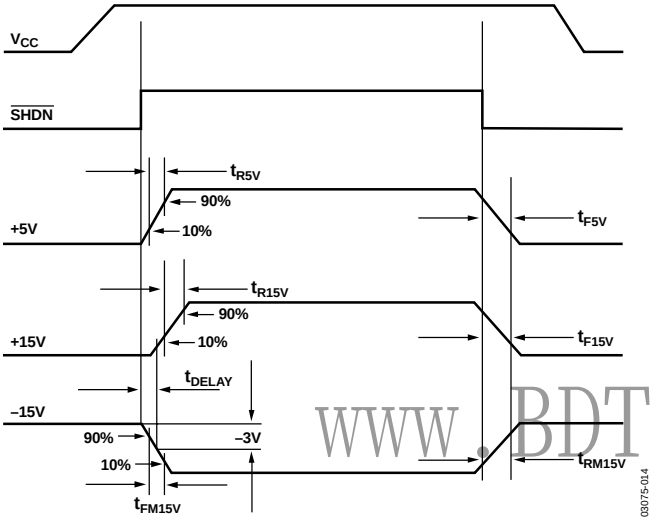


Figure 14. Power Sequence

TRANSIENT RESPONSE

The ADM8839 features extremely fast transient response, making it very suitable for fast image updates on TFT LCD panels. This means that even under changing load conditions, there is still very effective regulation of the 5 V output. Figure 11 and Figure 12 show how the 5 V output responds when a maximum load is dynamically connected and disconnected. Note that the output settles within 5 µs to less than 1% of the output level.

BOOSTING THE CURRENT DRIVE OF THE ±15 V SUPPLY

The ADM8839 ±15 V output can deliver 150 µA of current in the typical configuration, as shown in Figure 15. It is also possible to draw 100 µA from the +15 V output and 200 µA from the −15 V output, or vice versa. It is possible to draw a maximum of only 300 µA combined from the +15 V and the −15 V outputs at any time (see Figure 16). In this configuration, +5VOUT (Pin 4) is connected to +5VIN (Pin 5), as shown in the functional block diagram (see Figure 1).

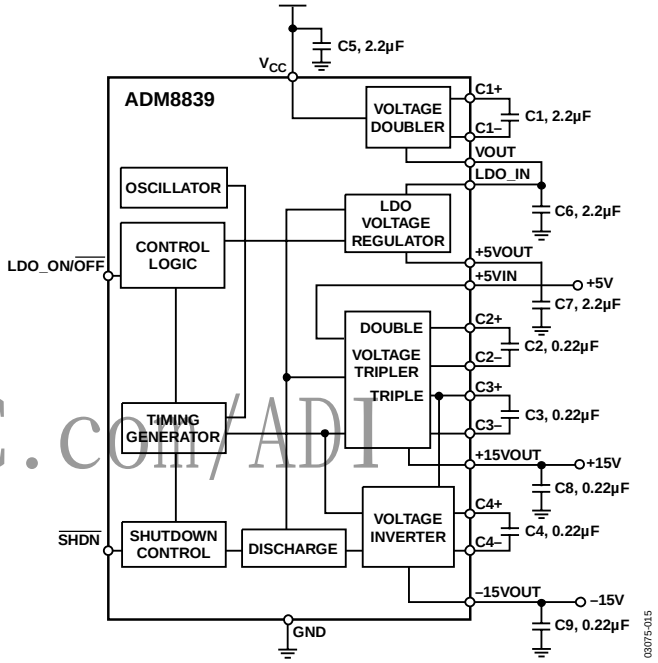


Figure 15. Typical Configuration

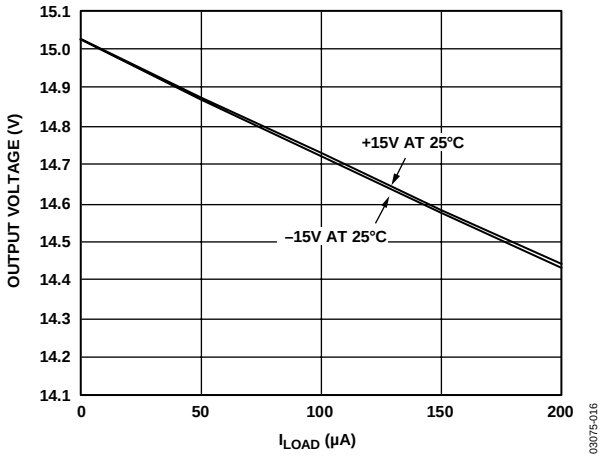


Figure 16. +15 V/−15 V Output Voltage vs. Load Current, Typical Configuration

It is possible to configure the ADM8839 to supply up to 400 µA on the ±15 V outputs by changing its configuration slightly, as shown in Figure 17.

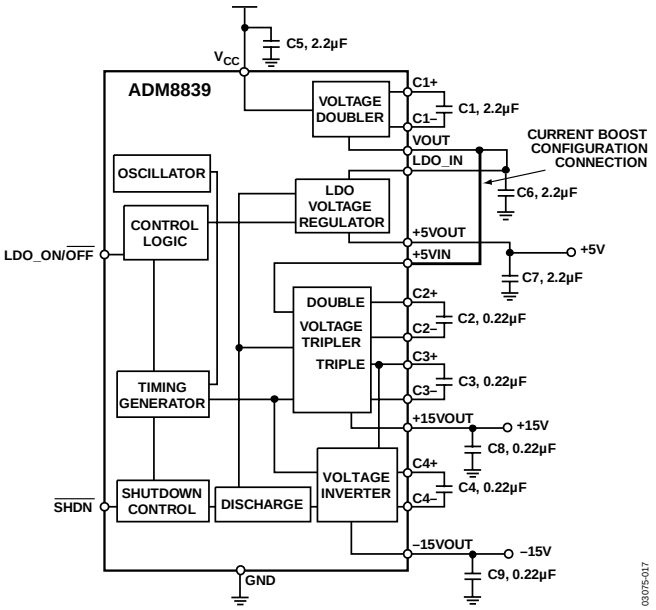


Figure 17. Current Boost Configuration

The configuration in Figure 17 can supply up to 400 µA of current on both the +15 V and the −15 V outputs. If the load on the ±15 V does not draw any current, the voltage on the ±15 V outputs can rise up to ±16.5 V (see Figure 18). In this configuration, VOUT (Pin 2) is connected to +5VIN (Pin 5).

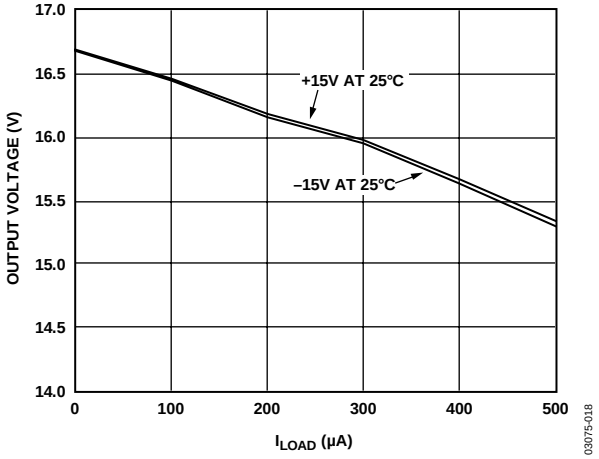
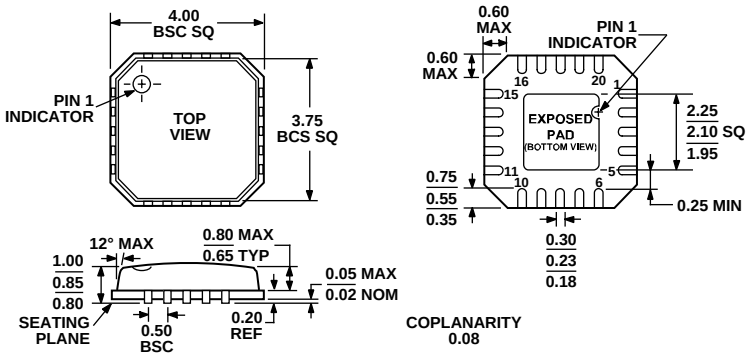


Figure 18. +15 V/−15 V Output Voltage vs. Load Current, Current Boost Configuration

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 19. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Ordering Quantity	Package Description	Package Option
ADM8839ACP	−40°C to +85°C	75	20-Lead LFCSP_VQ	CP-20-1
ADM8839ACP-REEL	−40°C to +85°C	5,000	20-Lead LFCSP_VQ	CP-20-1
ADM8839ACP-REEL7	−40°C to +85°C	1,500	20-Lead LFCSP_VQ	CP-20-1
ADM8839ACPZ[1]	−40°C to +85°C	75	20-Lead LFCSP_VQ	CP-20-1
ADM8839ACPZ-REEL[1]	−40°C to +85°C	5,000	20-Lead LFCSP_VQ	CP-20-1
ADM8839ACPZ-REEL7[1]	−40°C to +85°C	1,500	20-Lead LFCSP_VQ	CP-20-1
EVAL-ADM8839EB			Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES