3 V/5 V CMOS
0.5 Ω SPDT/2:1 Mux in SC70

ADG849

FEATURES

Ultralow on-resistance:
- **0.5 Ω typical**
- **0.8 Ω maximum at 5 V supply**

Excellent audio performance, ultralow distortion:
- **0.13 Ω typical**
- **0.24 Ω maximum R_{ON} flatness**

High current carrying capability:
- **400 mA continuous current**
- **600 mA peak current at 5 V**

Automotive temperature range: –40°C to +125°C

Rail-to-rail operation

Typical power consumption (<0.01 µW)

Pin-compatible upgrade for the ADG749 and ADG779

APPLICATIONS

Cellular phones
PDAs
Battery-powered systems
Audio and video signal routing
Modems
PCMCIA cards
Hard drives
Relay replacement

FUNCTIONAL BLOCK DIAGRAM

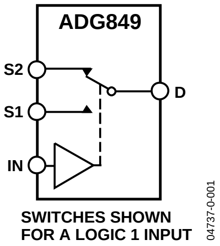

Figure 1.

GENERAL DESCRIPTION

The ADG849 is a monolithic, CMOS SPDT (single pole, double throw) switch that operates with a supply range of 1.8 V to 5.5 V. It is designed to offer ultralow on-resistance values of typically 0.5 Ω. This design makes the ADG849 an ideal solution for applications that require minimal distortion through the switch. The ADG849 also has the capability of carrying large amounts of current, typically 600 mA at 5 V operation.

Each switch of the ADG849 conducts equally well in both directions when on. The device exhibits break-before-make switching action, thus preventing momentary shorting when switching channels.

The ADG849 is available in a tiny, 6-lead SC70 package, making it the ideal candidate for space-constrained applications.

PRODUCT HIGHLIGHTS

1. Very low on-resistance, 0.5 Ω typical.
2. Tiny, 6-lead SC70 package.
3. Low power dissipation. The CMOS construction ensures low power dissipation.
4. High current carrying capability.
5. Low THD + noise (0.01% typ).

Rev. 0

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REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS

Table 1. V_{DD} = 4.5 V to 5.5 V, GND = 0 V[1]

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On-Resistance (R_{ON})	0.5			Ω typ	V_S = 0 V to V_{DD}, I_{DS} = −100 mA
	0.6	0.7	0.8	Ω max	See Figure 15
On-Resistance Match Between Channels (ΔR_{ON})	0.05			Ω typ	V_S = 0.85 V, I_{DS} = −100 mA
	0.095	0.11	0.125	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.13			Ω typ	V_S = 0 V to V_{DD}, I_{DS} = −100 mA
	0.18	0.22	0.24	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V, see Figure 16
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = 1 V, or V_S = V_D = 4.5 V, see Figure 17
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	2.5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	11			ns typ	R_L = 50 Ω, C_L = 35 pF
	15	17	18	ns max	V_S = 3 V, see Figure 18
t_{OFF}	9			ns typ	R_L = 50 Ω, C_L = 35 pF
	13	14	15	ns max	V_S = 3 V, see Figure 18
Break-Before-Make Time Delay, t_{BBM}	5			ns typ	R_L = 50 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 3 V, see Figure 19
			1	ns min	
Charge Injection	50			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 20
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz see Figure 21
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 22
Bandwidth: −3 dB	38			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 23
Insertion Loss	0.04			dB typ	R_L = 50 Ω, C_L = 5 pF, see Figure 23
THD + N	0.01			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, Vs = 2 V p-p
C_S (Off)	52			pF typ	
C_D, C_S (On)	145			pF typ	
POWER REQUIREMENTS					V_{DD} = 5.5 V, Digital Inputs = 0 V or 5.5 V
I_{DD}	0.001			μA typ	
			1.0	μA max	

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[1] The temperature range for the Y version is −40°C to +125°C.

[2] Guaranteed by design, not subject to production test.

Table 2. V_{DD} = 2.7 V to 3.6 V, GND = 0 V[1]

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On-Resistance (R_{ON})	0.72			Ω typ	V_S = 0 V to V_{DD}, I_{DS} = −100 mA
	1.1	1.1	1.2	Ω max	See Figure 15
On-Resistance Match Between Channels (ΔR_{ON})	0.05			Ω typ	V_S = 1.5 V, I_{DS} = −100 mA
	0.095	0.11	0.125	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.3			Ω typ	V_S = 0 V to V_{DD}, I_{DS} = −100 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V, see Figure 16
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1 V, or V_S = V_D = 3 V; see Figure 17
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	V_{DD} = 3 V to 3.6 V
			0.7	V max	V_{DD} = 2.7 V
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	2.5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	16			ns typ	R_L = 50 Ω, C_L = 35 pF
	22	24	26	ns max	V_S = 1.5 V, see Figure 18
t_{OFF}	13			ns typ	R_L = 50 Ω, C_L = 35 pF
	18	20	22	ns max	V_S = 1.5 V, see Figure 18
Break-Before-Make Time Delay, t_{BBM}	7			ns typ	R_L = 50 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 1.5 V, see Figure 19
			1	ns min	
Charge Injection	30			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 20
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 21
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 22
Bandwidth: −3 dB	38			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 23
Insertion Loss	0.04			dB typ	R_L = 50 Ω C_L = 5 pF, see Figure 23
THD + N	0.02			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, Vs = 1 V p-p
C_S (Off)	55			pF typ	f = 1 MHz
C_D, C_S (On)	147			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V
					Digital Inputs = 0 V or 3.6 V
I_{DD}	0.001			μA typ	
			1.0	μA max	

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[1] The temperature range for the Y version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

Table 3. T_A = 25°C, unless otherwise noted

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
Analog Inputs[1]	–0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs	–0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	400 mA
Operating Temperature Range	
Extended	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
SC70 Package	
θ_{JA} Thermal Impedance	332°C/W
θ_{JC} Thermal Impedance	120°C/W
Reflow Soldering	
Peak Temperature	260(0/–5)°C
Time at Peak Temperature	10 sec to 40 sec

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[1] Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table 4. Truth Table

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

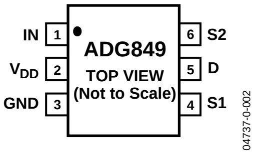


Figure 2. Pin Configuration

Table 5. Terminology

Mnemonic	Function
V_{DD}	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
I_{DD}	Positive Supply Current.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic Resistance between D and S.
ΔR_{ON}	On-Resistance Match Between any Two Channels i.e., R_{ON} Maximum to R_{ON} Minimum.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (Off)	Source Leakage Current with the Switch Off.
I_D, I_S (On)	Channel Leakage Current with the Switch On.
V_D (V_S)	Analog Voltage on Terminals D, S.
V_{INL}	Maximum Input Voltage for Logic 0.
V_{INH}	Minimum Input Voltage for Logic 1.
I_{INL} (I_{INH})	Input Current of the Digital Input.
C_S (Off)	Off Switch Source Capacitance. Measured with reference to ground.
C_D, C_S (On)	On Switch Capacitance. Measured with reference to ground.
t_{ON}	Delay time between the 50% and 90% points of the digital input and switch on condition.
t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch off condition.
t_{BBM}	On or off time measured between the 80% points of both switches when switching from one to another.
Charge Injection	A measure of the glitch impulse transfered from the digital input to the analog output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an off switch.
Bandwidth	The frequency at which the output is attenuated by 3 dB.
On-Response	The frequency response of the on switch.
Insertion Loss	The loss due to the on-resistance of the switch.
THD + N	The ratio of harmonic amplitudes plus the noise of a signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

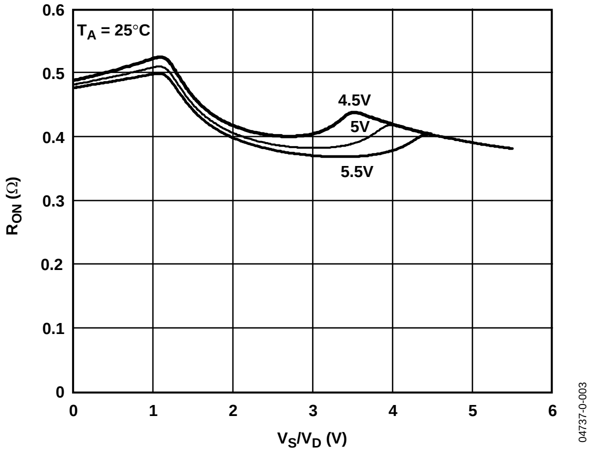


Figure 3. On-Resistance vs. V_D/V_S, V_{DD} = 5 V ±10%

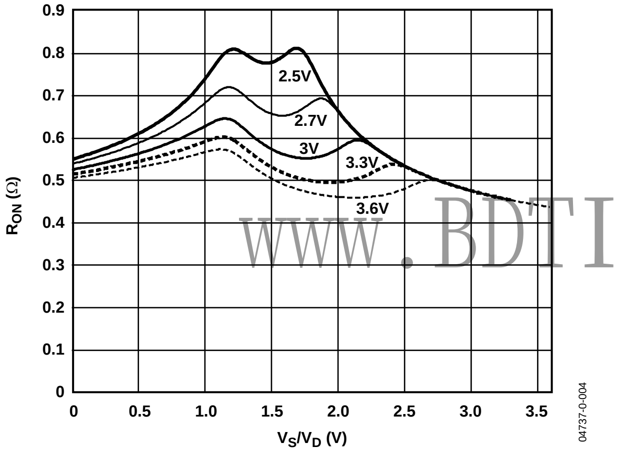


Figure 4. On-Resistance vs. V_D/V_S, V_{DD} = 2.5 V to 3.6 V

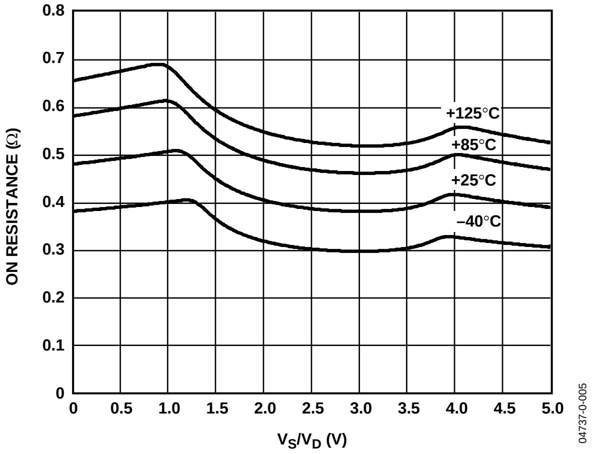


Figure 5. On-Resistance vs. Temperature, V_{DD} = 5 V

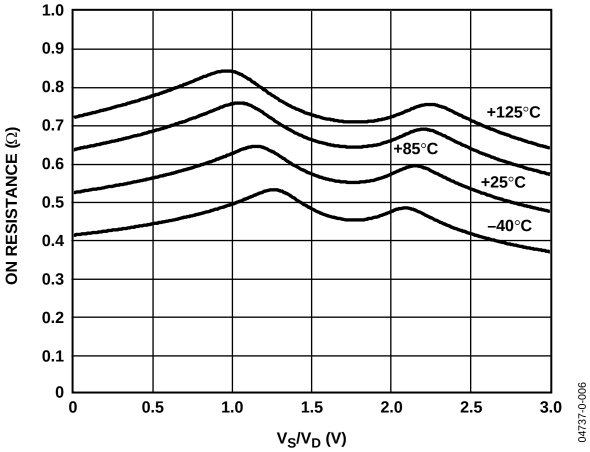


Figure 6. On-Resistance vs. Temperature, V_{DD} = 3 V

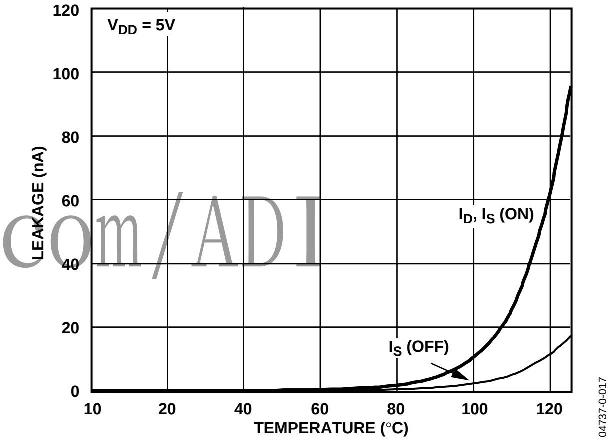


Figure 7. Leakage Currents vs. Temperature, V_{DD} = 5 V

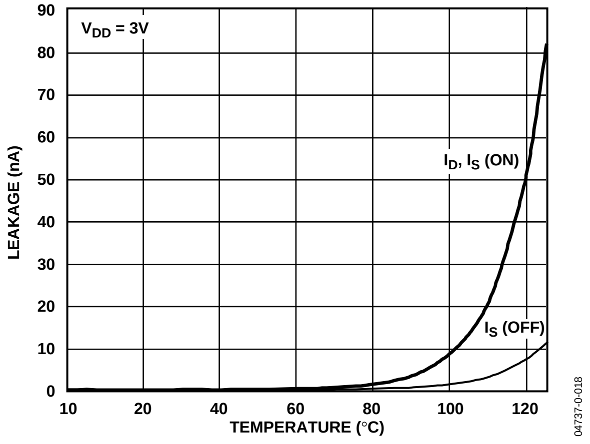


Figure 8. Leakage Currents vs. Temperature, V_{DD} = 3 V

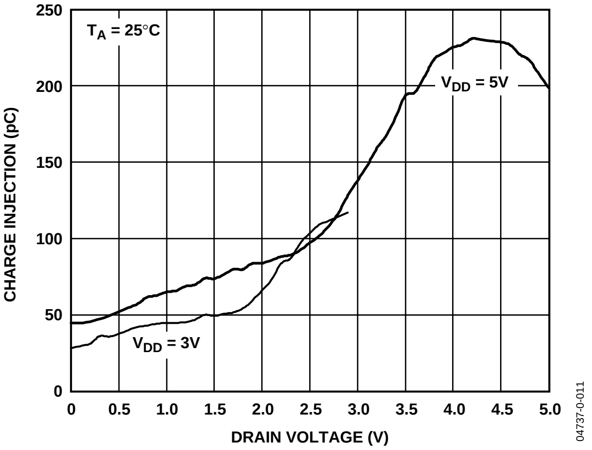


Figure 9. Charge Injection

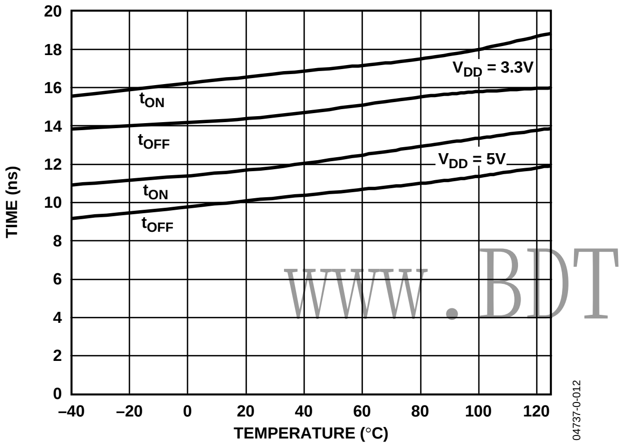


Figure 10. t_{ON}/t_{OFF} vs. Temperature

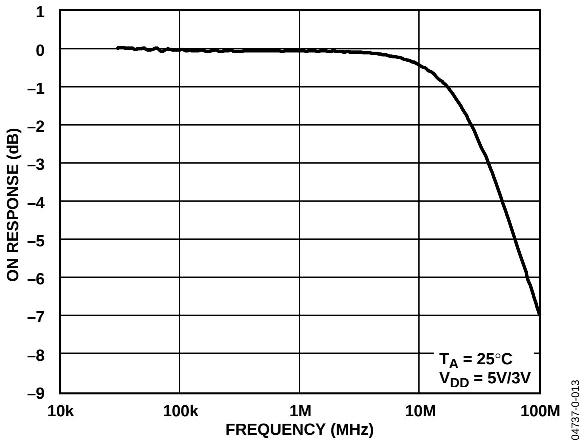


Figure 11. Bandwidth

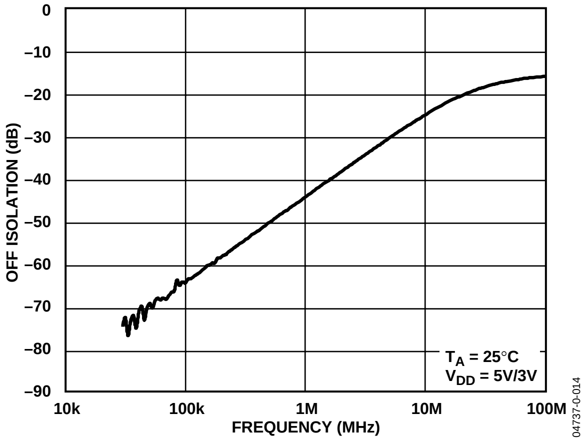


Figure 12. Off Isolation vs. Frequency

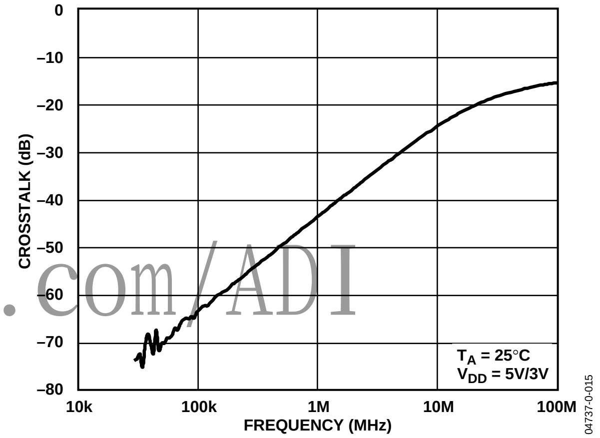


Figure 13. Crosstalk vs. Frequency

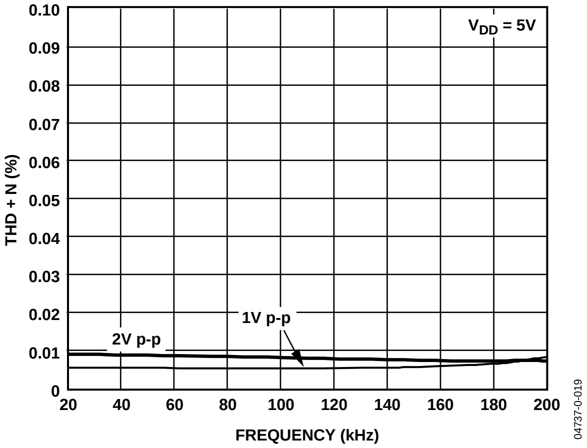


Figure 14. Total Harmonic Distortion + Noise

TEST CIRCUITS

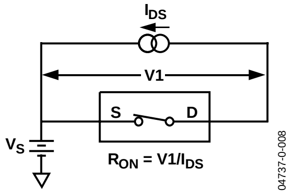


Figure 15. On-Resistance

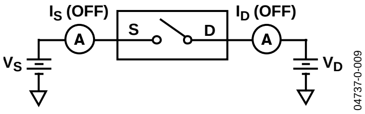


Figure 16. Off-Leakage

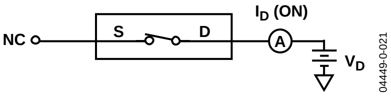


Figure 17. On-Leakage

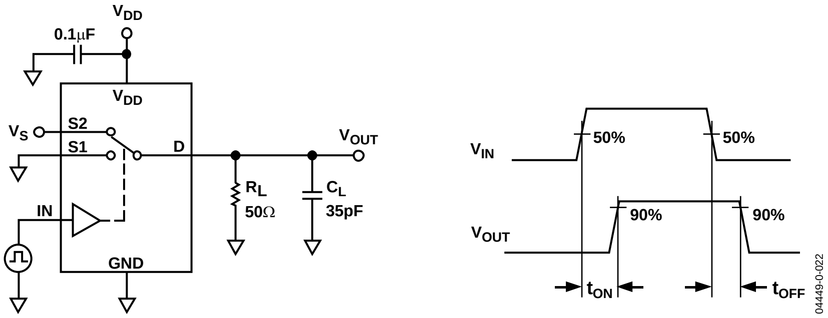


Figure 18. Switching Times, t_{ON}, t_{OFF}

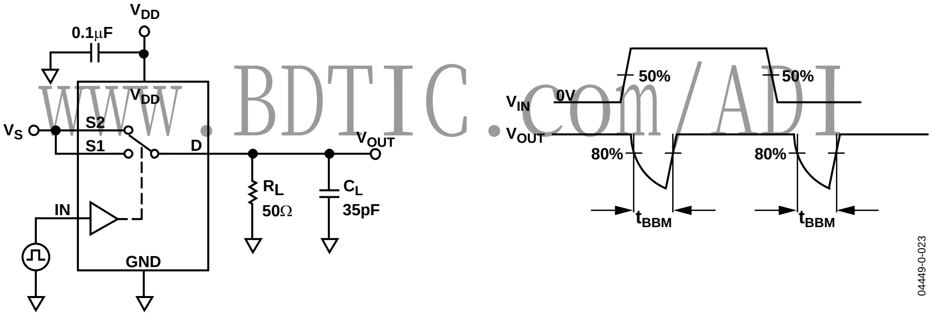


Figure 19. Break-Before-Make Time Delay, t_{BBM}

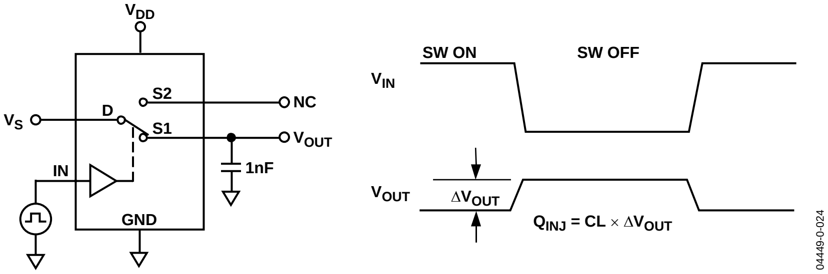


Figure 20. Charge Injection

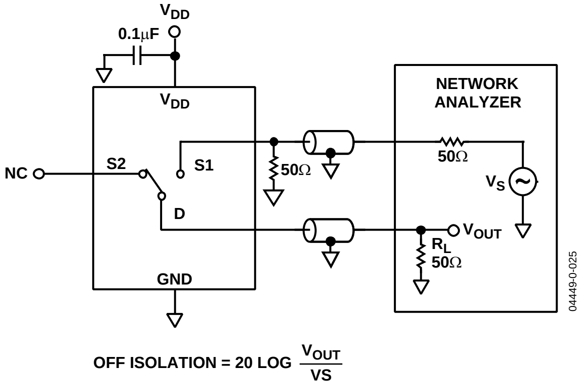


Figure 21. Off Isolation

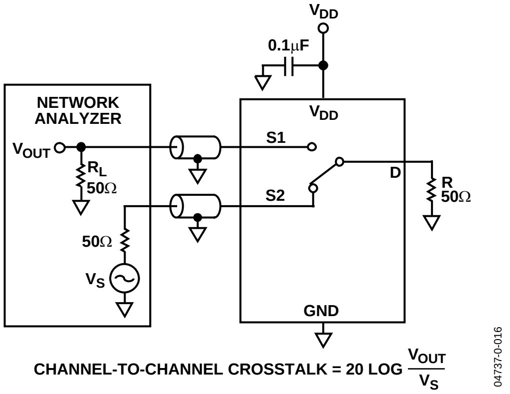


Figure 22. Channel-to-Channel Crosstalk

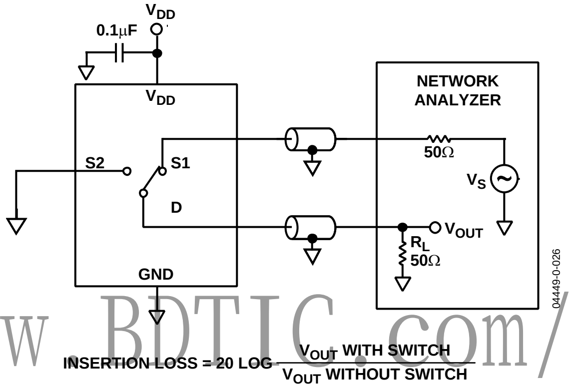
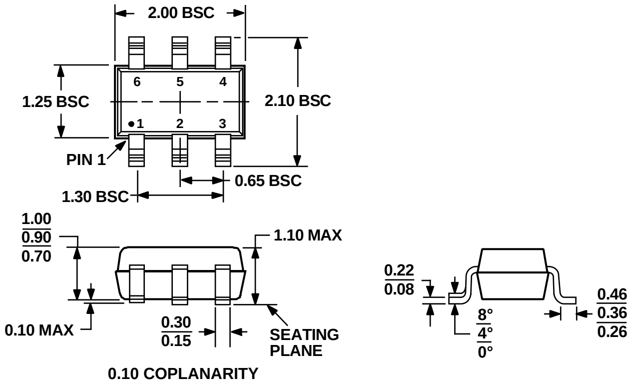


Figure 23. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203AB

Figure 24. 6-Lead SC70 Package
[KS-6]
Dimensions shown in Millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG849YKSZ-500RL7[2]	−40°C to +125°C	SC70 (Plastic Surface Mount)	KS-6	SNA
ADG849YKSZ-REEL[2]	−40°C to +125°C	SC70 (Plastic Surface Mount)	KS-6	SNA
ADG849YKSZ-REEL7[2]	−40°C to +125°C	SC70 (Plastic Surface Mount)	KS-6	SNA

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[1] Branding on all packages is limited to three characters due to space constraints.
[2] Z = Pb-free part.

NOTES

ANALOG DEVICES

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