0.35 Ω CMOS 1.65 V to 3.6 V Single SPDT Switch/2:1 MUX

ADG839

FEATURES

1.65 V to 3.6 V operation
Ultralow on resistance:
- **0.35 Ω typical**
- **0.5 Ω max at 2.7 V supply**

Excellent audio performance, ultralow distortion:
- **0.055 Ω typical**
- **0.09 Ω max R_{ON} flatness**

High current carrying capability:
- **300 mA continuous**
- **500 mA peak current at 3.3 V**

Automotive temperature range: –40°C to +125°C
Rail-to-rail switching operation
Typical power consumption (<0.1 μW)

FUNCTIONAL BLOCK DIAGRAM

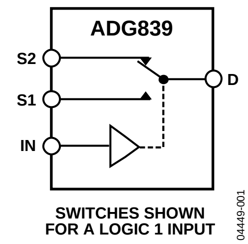

Figure 1.

APPLICATIONS

Cellular phones
PDAs
MP3 players
Power routing
Battery-powered systems
PCMCIA cards
Modems
Audio and video signal routing
Communication systems

PRODUCT HIGHLIGHTS

1. 0.6 Ω over full temperature range of –40°C to +125°C.
2. Compatible with 1.8 V CMOS logic.
3. High current handling capability (300 mA continuous current at 3.3 V).
4. Low THD + N (0.01% typ).
5. Tiny SC70 package.

GENERAL DESCRIPTION

The ADG839 is a low voltage CMOS device containing a single-pole, double-throw (SPDT) switch. This device offers ultralow on resistance of less than 0.6 Ω over the full temperature range. The ADG839 is fully specified for 1.8 V, 2.5 V, and 3.3 V supply operation.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG839 exhibits break-before-make switching action.

The ADG839 is available in a 6-lead SC70 package.

Table 1. ADG839 Truth Table

Logic	Switch 2 (S2)	Switch 1 (S1)
0	Off	On
1	On	Off

Rev. 0

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REVISION HISTORY

10/04—Initial Version: Revision 0

SPECIFICATIONS[1]—2.7 V TO 3.6 V

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	V_{DD} = 2.7 V
On Resistance (R_{ON})	0.35			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}, I_S = 100 mA;
	0.5	0.56	0.61	Ω max	Figure 19
On Resistance Match between	0.04			Ω typ	V_{DD} = 2.7 V, V_S = 0.9 V, I_S = 100 mA
Channels (ΔR_{ON})	0.075	0.085	0.095	Ω max	
On Resistance Flatness	0.055			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD},
($R_{FLAT (ON)}$)	0.07	0.082	0.09	Ω max	I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 0.6 V/3.3 V, V_D = 3.3 V/0.6 V; Figure 20
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 0.6 V or 3.3 V; Figure 21
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	3.2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	12			ns typ	R_L = 50 Ω, C_L = 35 pF
	16	18	19	ns max	V_S = 1.5 V/0 V; Figure 22
t_{OFF}	6.5			ns typ	R_L = 50 Ω, C_L = 35 pF
	8.5	9	9.5	ns max	V_S = 1.5 V; Figure 22
Break-Before-Make Time Delay	5			ns typ	R_L = 50 Ω, C_L = 35 pF; Figure 23
(t_{BBM})			1	ns min	V_{S1} = V_{S2} = 1.5 V;
Charge Injection	70			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Figure 24
Off Isolation	−57			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 25
Channel-to-Channel Crosstalk	−57			dB typ	S1 −S2; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 26
Total Harmonic Distortion (THD + N)	0.013			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 3 V p-p
Insertion Loss	−0.01			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 27
−3 dB Bandwidth	25			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 27
C_S (OFF)	74			pF typ	
C_D, C_S (ON)	120			pF typ	V_{DD} = 3.6 V
POWER REQUIREMENTS					Digital inputs = 0 V or 3.6 V
I_{DD}	0.003			μA typ	
		1	4	μA max	

[1] Temperature range for the Y version is −40°C to +125°C.
[2] Guaranteed by design; not subject to production test.

SPECIFICATIONS[1]—2.3 V TO 2.7 V

V_{DD} = 2.5 V ± 0.2 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to VDD	V	
On Resistance (R_{ON})	0.35			Ω typ	V_{DD} = 2.3 V, V_S = 0 V to V_{DD},
	0.5	0.55	0.6	Ω max	I_S = 100 mA; Figure 19
On Resistance Match between	0.04			Ω typ	V_{DD} = 2.3 V, V_S = 0.95 V,
Channels (ΔR_{ON})	0.075	0.085	0.095	Ω max	I_S = 100 mA
On Resistance Flatness ($R_{FLAT (ON)}$)	0.045			Ω typ	V_{DD} = 2.3 V, V_S = 0 V to V_{DD},
		0.13	0.13	Ω max	I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 2.7 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 0.6 V/2.4 V, V_D = 2.4 V/0.6 V; Figure 20
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 0.6 V or 2.4 V; Figure 21
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.7	V min	
Input Low Voltage, V_{INL}			0.7	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	3.2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	14.5			ns typ	R_L = 50 Ω, C_L = 35 pF
	18	20	21	ns max	V_S = 1.5 V/0 V; Figure 22
t_{OFF}	7.5			ns typ	R_L = 50 Ω, C_L = 35 pF
	9.2	9.5	9.8	ns max	V_S = 1.5 V; Figure 22
Break-before-Make Time Delay (t_{BBM})	7			ns typ	R_L = 50 Ω, C_L = 35 pF; Figure 23
			1	ns min	V_{S1} = V_{S2} = 1.5 V;
Charge Injection	60			pC typ	V_S = 1.25 V, R_S = 0 Ω, C_L = 1 nF; Figure 24
Off Isolation	−57			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 25
Channel-to-Channel Crosstalk	−57			dB typ	S1−S2; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 26
Total Harmonic Distortion (THD + N)	0.021			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p
Insertion Loss	−0.01			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 27
−3 dB Bandwidth	25			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 27
C_S (OFF)	78			pF typ	
C_D, C_S (ON)	127			pF typ	V_{DD} = 2.7 V
POWER REQUIREMENTS					Digital inputs = 0 V or 2.7 V
I_{DD}	0.003			μA typ	
		1	4	μA max	

[1] Temperature range for the Y version is −40°C to +125°C.
[2] Guaranteed by design; not subject to production test.

SPECIFICATIONS[1]—1.65 V TO 1.95 V

V_{DD} = 1.65 V ± 1.95 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.5			Ω typ	V_{DD} = 1.8 V, V_S = 0 V to V_{DD}, I_S = 100 mA;
	0.8	1.2	1.2	Ω max	Figure 19
	1.3	2.5	2.5	Ω max	V_{DD} = 1.65 V, V_S = 0 V to V_{DD}, I_S = 100 mA
On Resistance Match between	0.04			Ω typ	V_{DD} = 1.65 V, V_S = TBD, I_S = 100 mA
Channels (ΔR_{ON})	0.075	0.08	0.08	Ω max	I_S = 100 mA
On Resistance Flatness ($R_{FLAT (ON)}$)	0.3			Ω typ	V_{DD} = 1.65 V, V_S = 0 V to V_{DD}, I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 1.95 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 0.6 V/1.65 V, V_D = 1.65 V/0.6 V; Figure 20
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 0.6 V or 1.65 V; Figure 21
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 V_{DD}	V min	
Input Low Voltage, V_{INL}			0.35 V_{DD}	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	3.2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	20			ns typ	R_L = 50 Ω, C_L = 35 pF
	28	30	31	ns max	V_S = 1.5 Ω/0 V; Figure 22
t_{OFF}	8			ns typ	R_L = 50 Ω, C_L = 35 pF
	10.1	10.5	10.7	ns max	V_S = 1.5 V; Figure 22
Break-before-Make Time Delay (t_{BBM})	12			ns typ	R_L = 50 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = 1 V; Figure 23
Charge Injection	50			pC typ	V_S = 1 V, R_S = 0 V, C_L = 1 nF; Figure 24
Off Isolation	−57			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 25
Channel-to-Channel Crosstalk	−57			dB typ	S1 −S2; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 26
Total Harmonic Distortion (THD + N)	0.033			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 1 V p-p
Insertion Loss	−0.01			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 27
−3 dB Bandwidth	25			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 27
C_S (OFF)	83			pF typ	V_{DD} = 1.95 V
C_D, C_S (ON)	132			pF typ	Digital inputs = 0 V or 1.95 V
POWER REQUIREMENTS					Digital inputs = 0 V or 1.95 V
I_{DD}	0.003			μA typ	
		1	4	μA max	

[1] Temperature range for the Y version is −40°C to +125°C.
[2] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4.6 V
Analog Inputs[1]	−0.3 V to V_{DD} + 0.3 V
Digital Inputs	−0.3 V to 4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SC70 Package	332°C/W
θ_{JA} Thermal Impedance	120°C/W
Lead Temperature, Soldering (10 seconds)	300°C
IR Reflow, Peak Temperature	220°C

[1] Overvoltages at S or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

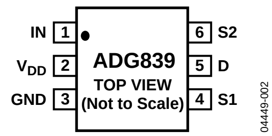

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN	Logic control input.
2	V_{DD}	Most positive power supply potential.
3	GND	Ground (0 V) reference.
4, 6	S1, S2	Source terminal. Can be an input or output.
5	D	Drain terminal. Can be an input or output.

For more information, refer to the Terminology section.

TYPICAL PERFORMANCE CHARACTERISTICS

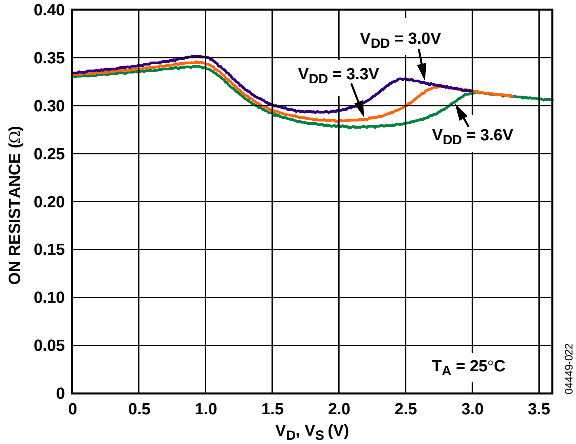

Figure 3. On Resistance vs. V_D (V_S) V_{DD} = 3 V to 3.6 V

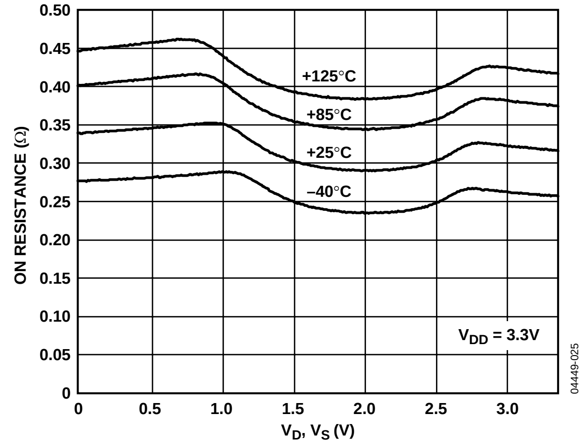

Figure 6. On Resistance vs. V_D (V_S) for Different Temperature, V_{DD} = 3.3 V

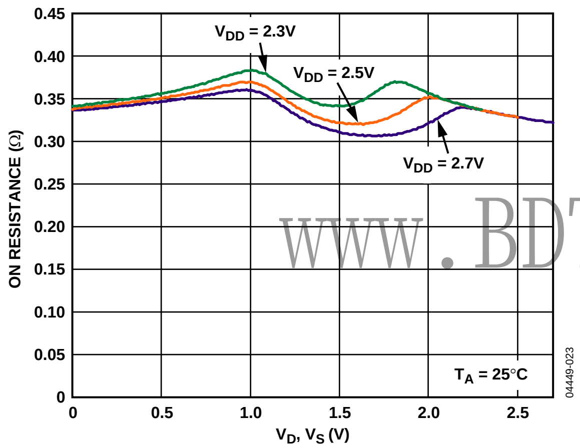

Figure 4. On Resistance vs. V_D (V_S) V_{DD} = 2.5 V ± 0.2 V

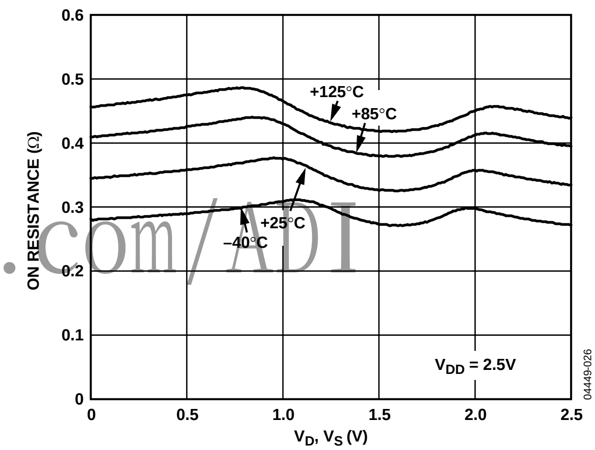

Figure 7. On Resistance vs. V_D (V_S) for Different Temperature, V_{DD} = 2.5 V

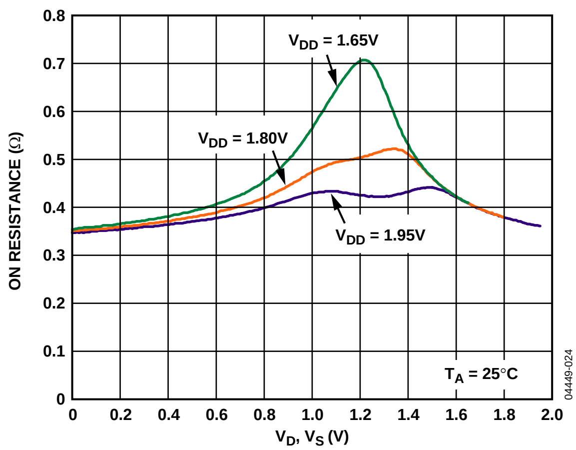

Figure 5. On Resistance vs. V_D (V_S) V_{DD} = 1.8 V ± 0.15 V

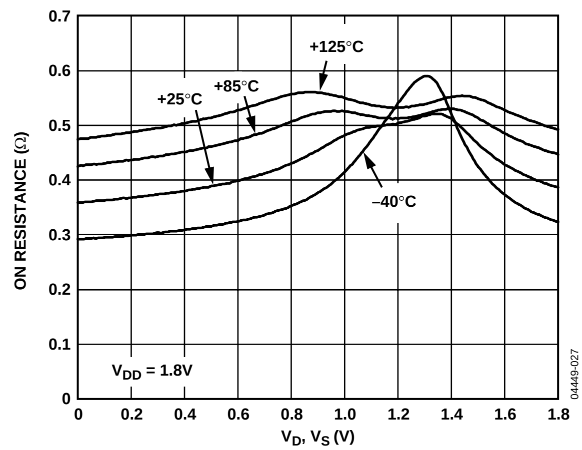

Figure 8. On Resistance vs. V_D (V_S) for Different Temperature, V_{DD} = 1.8 V

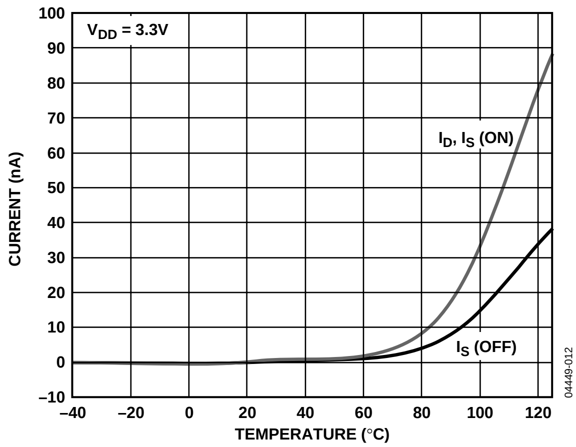

Figure 9. Leakage Current vs. Temperature, V_{DD} = 3.3 V

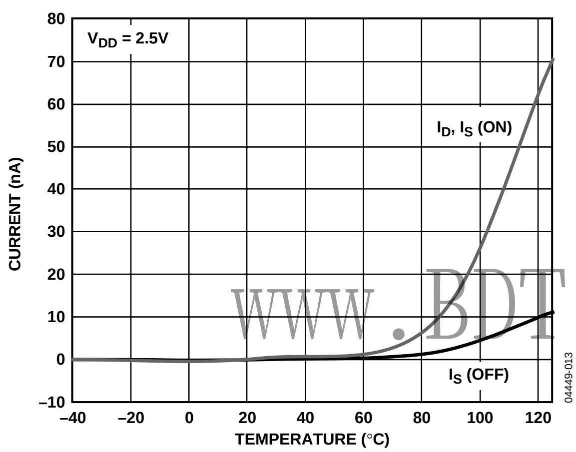

Figure 10. Leakage Current vs. Temperature, V_{DD} = 2.5 V

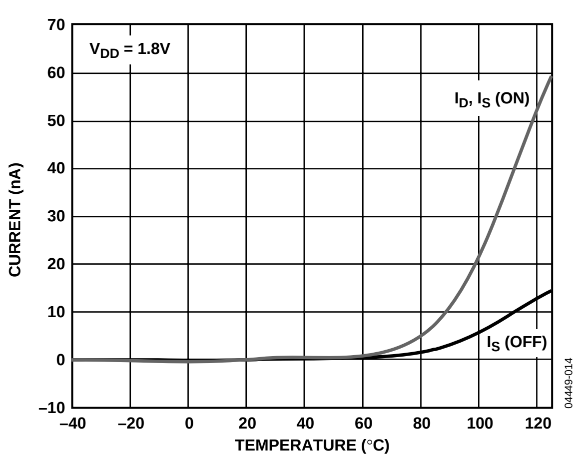

Figure 11. Leakage Current vs. Temperature, V_{DD} = 1.8 V

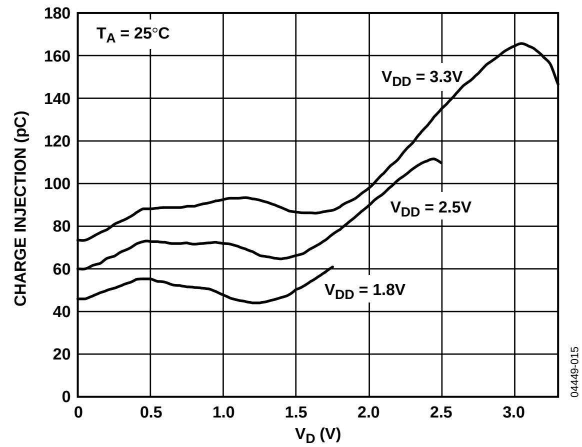

Figure 12. Charge Injection vs. Source Voltage

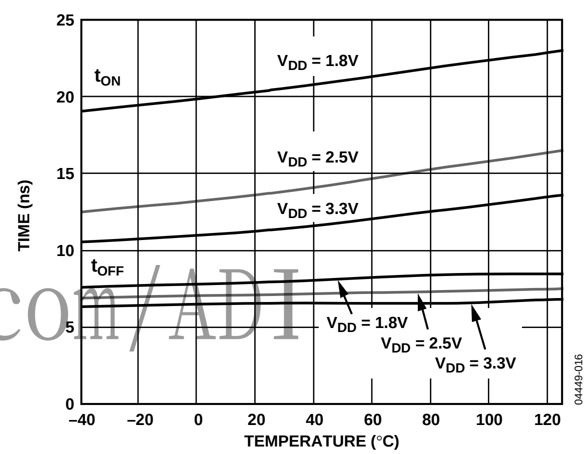

Figure 13. t_{ON}/t_{OFF} Times vs. Temperature

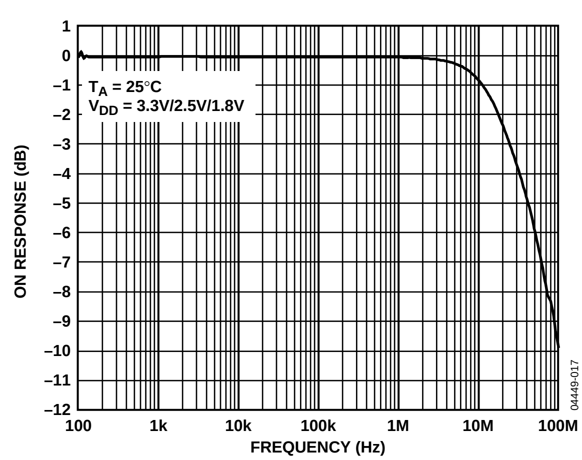

Figure 14. Bandwidth

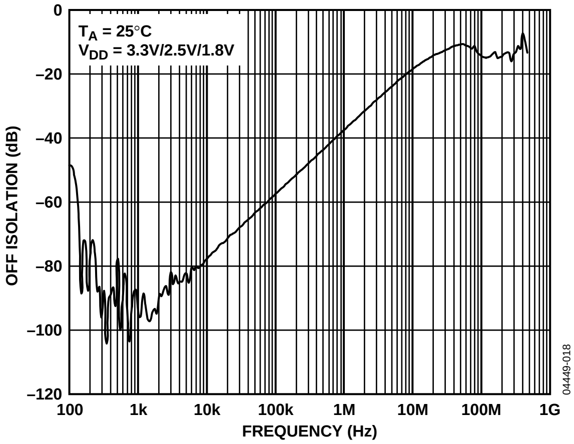

Figure 15. Off Isolation vs. Frequency

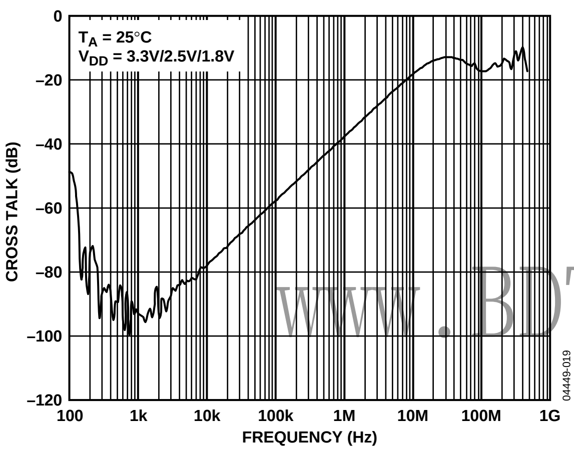

Figure 16. Crosstalk vs. Frequency

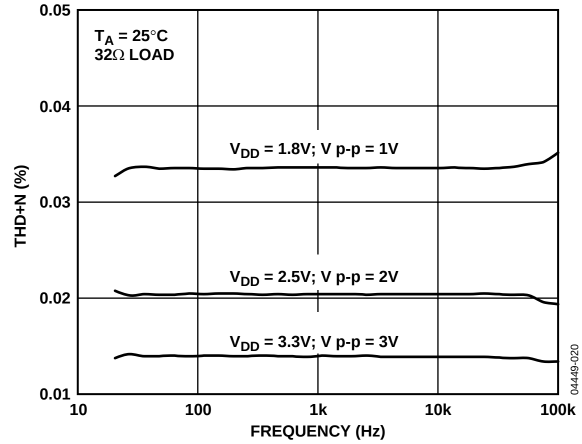

Figure 17. Total Harmonic Distortion + Noise

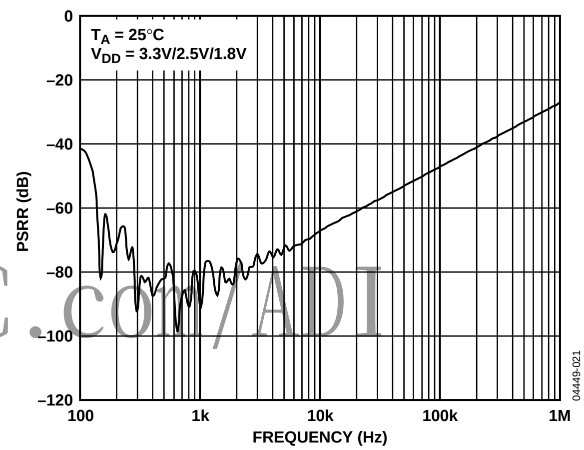

Figure 18. AC PSRR

TERMINOLOGY

I_{DD}
Positive supply current.

V_D (V_S)
Analog voltage on Terminals D and S.

R_{ON}
Ohmic resistance between D and S.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}
On resistance match between any two channels.

I_S (OFF)
Source leakage current with the switch off.

I_D (OFF)
Drain leakage current with the switch off.

I_D, I_S (ON)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (OFF)
Off switch source capacitance. Measured with reference to ground.

C_D (OFF)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (ON)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BBM}
On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The attenuation between the input and output ports of the switch when the switch is in the on condition, and is due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitudes plus noise of a signal to the fundamental.

PSRR
Power Supply Rejection Ratio. This is a measure of the coupling of unwanted ac signals on the power supply to the switch output when the supply is not decoupled.

TEST CIRCUITS

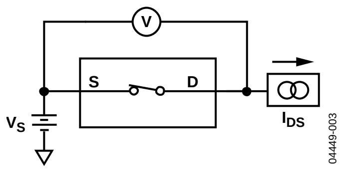

Figure 19. On Resistance

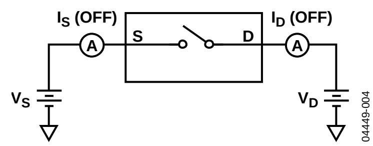

Figure 20. Off Leakage

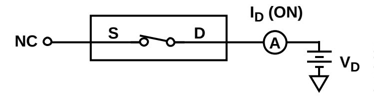

Figure 21. On Leakage

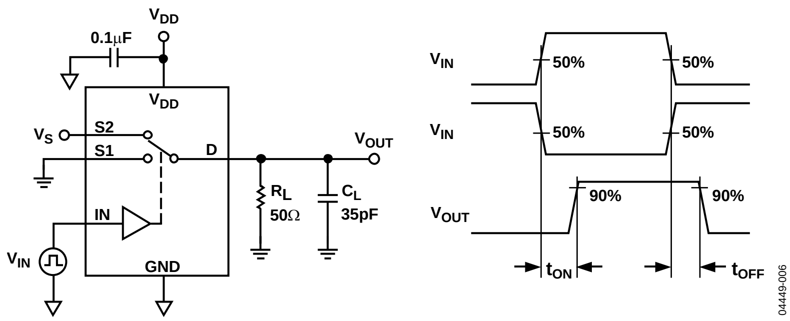

Figure 22. Switching Times, t_{ON}, t_{OFF}

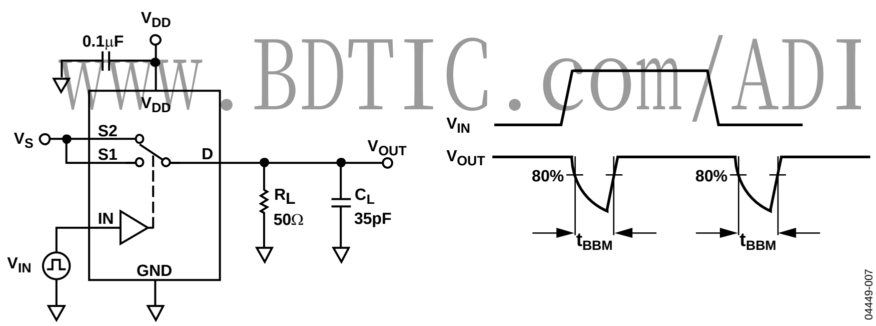

Figure 23. Break-before-Make Time Delay, t_{BBM}

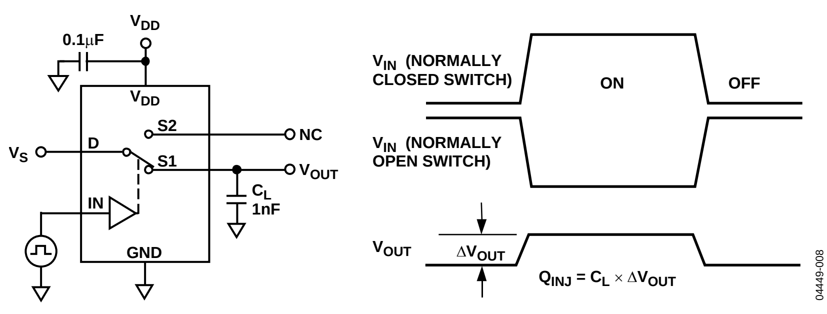

Figure 24. Charge Injection

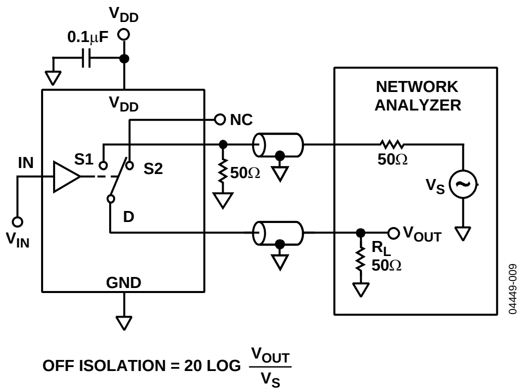

Figure 25. Off Isolation

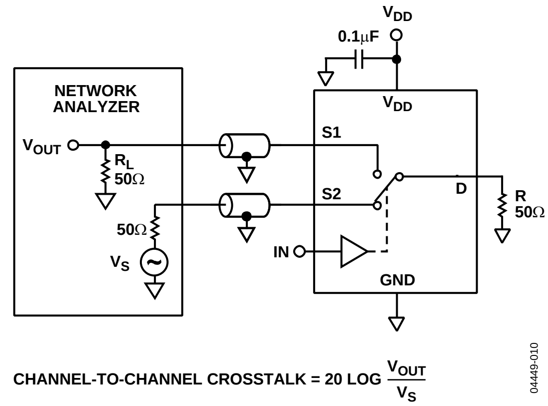

Figure 26. Channel-to-Channel Crosstalk

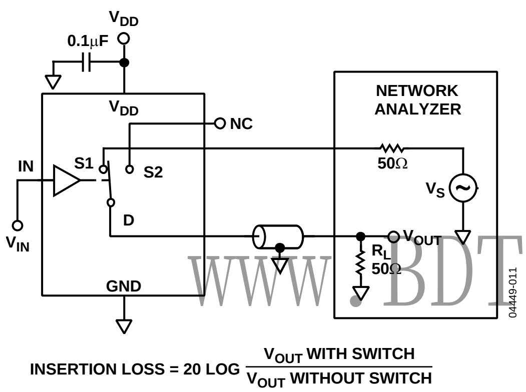

Figure 27. Bandwidth

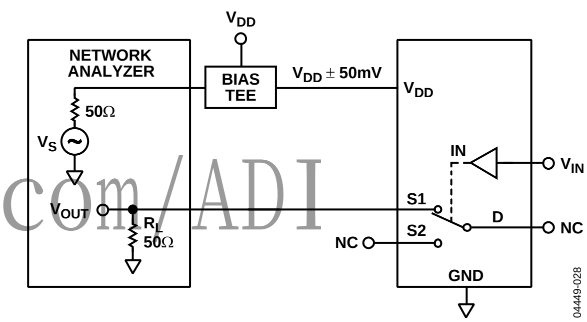

Figure 27. PSRR

OUTLINE DIMENSIONS

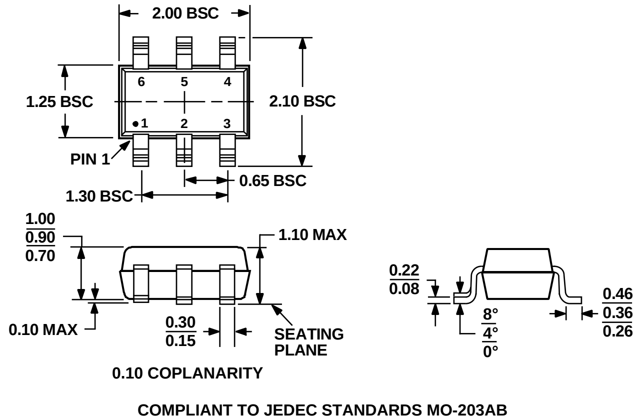

Figure 28. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG839YKSZ-500RL7[2]	–40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package	KS-6	SUA
ADG839YKSZ-REEL[2]	–40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package	KS-6	SUA
ADG839YKSZ-REEL7[2]	–40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package	KS-6	SUA

[1] Branding on this package is limited to three characters due to space constraints.
[2] Z = Pb-free part.

NOTES

NOTES

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