# Quad SPDT Switch

# ADG333A

## FEATURES

- 44 V supply maximum ratings
- $V_{SS}$ to $V_{DD}$ analog signal range
- Low on resistance (45 Ω max)
- Low $\Delta R_{ON}$ (5 Ω max)
- Low $R_{ON}$ match (4 Ω max)
- Low power dissipation
- Fast switching times
  - $t_{ON}$ < 175 ns
  - $t_{OFF}$ < 145 ns
- Low leakage currents (5 nA max)
- Low charge injection (10 pC max)
- Break-before-make switching action

## APPLICATIONS

- Audio and video switching
- Battery-powered systems
- Test equipment
- Communication systems

## FUNCTIONAL BLOCK DIAGRAM

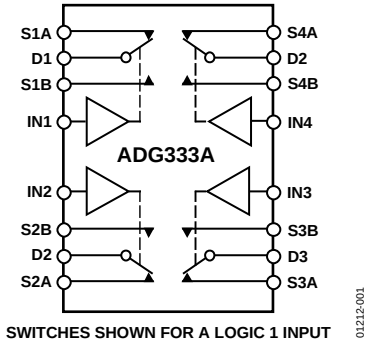


*Figure 1.*

## GENERAL DESCRIPTION



The ADG333A is a monolithic CMOS device comprising four independently selectable SPDT switches. It is designed on an LC²MOS process, which provides low power dissipation yet achieves a high switching speed and a low on resistance.

The on resistance profile is very flat over the full analog input range, ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the part suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable, battery-powered instruments.

When they are on, each switch conducts equally well in both directions and has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge inject

## PRODUCT HIGHLIGHTS

1. Extended signal range.
   The ADG333A is fabricated on an enhanced LC²MOS process, giving an increased signal range which extends to the supply rails.
2. Low power dissipation.
3. Low $R_{ON}$.
4. Single-supply operation.
   For applications where the analog signal is unipolar, the ADG333A can be operated from a single rail power supply. The part is fully specified with a single 12 V supply.

Rev. A


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**10/95—Revision 0: Initial Version**

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD}$ = +15 V, $V_{SS}$ = −15 V, GND = 0 V, unless otherwise noted.[1]

**Table 1.**

| Parameter | +25°C | −40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | $V_{SS}$ to $V_{DD}$ | V | |
| $R_{ON}$ | 20 | | Ω typ | $V_D$ = ±10 V, $I_S$ = −1 mA |
| | 45 | 45 | Ω max | |
| $\Delta R_{ON}$ | | 5 | Ω max | $V_D$ = ±5 V, $I_S$ = −10 mA |
| $R_{ON}$ Match | | 4 | Ω max | $V_D$ = ±10 V, $I_S$ = −10 mA |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = +16.5 V, $V_{SS}$ = −16.5 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.1 | | nA typ | $V_D$ = ±15.5 V, $V_S$ = +15.5 V |
| | ±0.25 | ±3 | nA max | Figure 15 |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.1 | | nA typ | $V_S$ = $V_D$ = ±15.5 V |
| | ±0.4 | ±5 | nA max | Figure 16 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | | ±0.005 | μA typ | $V_{IN}$ = 0 V or $V_{DD}$ |
| | | ±0.5 | μA max | |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{ON}$ | 90 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 175 | ns max | $V_S$ = ±10 V; Figure 17 |
| $t_{OFF}$ | 80 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 145 | ns max | $V_S$ = ±10 V; Figure 17 |
| Break-Before-Make Delay, $t_{OPEN}$ | 10 | | ns min | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | | | $V_S$ = +5 V; Figure 18 |
| Charge Injection | 2 | | pC typ | $V_D$ = 0 V, $R_D$ = 0 Ω, $C_L$ = 10 nF; |
| | 10 | | pC max | $V_{DD}$ = +15 V, $V_{SS}$ = −15 V; Figure 19 |
| OFF Isolation | 72 | | dB typ | $R_L$ = 75 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | $V_S$ = 2.3 V rms; Figure 20 |
| Channel-to-Channel Crosstalk | 85 | | dB typ | $R_L$ = 75 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | $V_S$ = 2.3 V rms; Figure 21 |
| $C_S$ (OFF) | 7 | | pF typ | |
| $C_D$, $C_S$ (ON) | 26 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| $I_{DD}$ | 0.05 | | mA typ | Digital inputs = 0 V or 5 V |
| | 0.25 | 0.35 | mA max | |
| $I_{SS}$ | 0.01 | | μA typ | |
| | 1 | 5 | μA max | |
| $V_{DD}/V_{SS}$ | | ±3/±20 | V min/V max | $\|V_{DD}\| = \|V_{SS}\|$ |

[1] Temperature range is as follows: B version: −40°C to +85°C.
[2] Guaranteed by design; not subject to production test.

## SINGLE SUPPLY

$V_{DD}$ = +12 V, $V_{SS}$ = 0 V ± 10%, GND = 0 V, unless otherwise noted.[1]

**Table 2.**

| Parameter | +25°C | −40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to $V_{DD}$ | V | |
| RON | 35 | | Ω typ | $V_D$ = 1 V, 10 V, $I_S$ = −1 mA |
| | | 75 | Ω max | |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = 13.2 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.1 | | nA typ | $V_D$ = 12.2 V/1 V, $V_S$ = 1 V/12.2 V |
| | ±0.25 | ±3 | nA max | Figure 15 |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.1 | | nA typ | $V_S$ = $V_D$ = 12.2 V/1 V |
| | ±0.4 | ±5 | nA max | Figure 16 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | | ±0.005 | μA typ | $V_{IN}$ = 0 V or $V_{DD}$ |
| | | ±0.5 | μA max | |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{ON}$ | 110 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 200 | ns max | $V_S$ = 8 V; Figure 17 |
| $t_{OFF}$ | 100 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 180 | ns max | $V_S$ = 8 V; Figure 17 |
| Break-Before-Make Delay, $t_{OPEN}$ | 10 | | ns min | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | | ns min | $V_S$ = 5 V; Figure 18 |
| Charge Injection | 5 | | pC typ | $V_D$ = 6 V, $R_D$ = 0 W, $C_L$ = 10 nF; |
| | | | | $V_{DD}$ = 12 V, $V_{SS}$ = 0 V; Figure 19 |
| OFF Isolation | 72 | | dB typ | $R_L$ = 75 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | $V_S$ = 1.15 V rms; Figure 20 |
| Channel-to-Channel Crosstalk | 85 | | dB typ | $R_L$ = 75 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | $V_S$ = 1.15 V rms; Figure 21 |
| $C_S$ (OFF) | 12 | | pF typ | |
| $C_D$, $C_S$ (ON) | 25 | | pF typ | |
| POWER REQUIREMENTS | | | | $V_{DD}$ = 13.5 V |
| $I_{DD}$ | 0.05 | | mA typ | Digital inputs = 0 V or 5 V |
| | 0.25 | 0.35 | mA max | |
| $V_{DD}$ | | ±3/±30 | V min/V max | |

[1] Temperature range is as follows: B Version: −40°C to +85°C.
[2] Guaranteed by design; not subject to production test.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C unless otherwise noted.

**Table 3.**

| Parameter | Min |
|---|---|
| $V_{DD}$ to $V_{SS}$ | +44 V |
| $V_{DD}$ to GND | −0.3 V to +30 V |
| $V_{SS}$ to GND | +0.3 V to −30 V |
| Analog, Digital Inputs[1] | $V_{SS}$ − 2 V to $V_{DD}$ + 2 V or 20 mA, whichever occurs first |
| Continuous Current, S or D | 20 mA |
| Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) | 40 mA |
| Operating Temperature Range | |
| Industrial (B Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +125°C |
| Junction Temperature | 150°C |
| $\theta_{JA}$, Thermal Impedance | |
| PDIP Package | 103°C/W |
| SOIC Package | 74°C/W |
| SSOP Package | 130°C/W |
| Lead Temperature, Soldering (10 sec) | 260°C |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |

[1] Overvoltage at IN, S, or D is clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Truth Table**

| Logic | Switch A | Switch B |
|---|---|---|
| 0 | Off | On |
| 1 | On | Off |



## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# TERMINOLOGY

**$R_{ON}$**

Ohmic resistance between D and S.

**$\Delta R_{ON}$**

$R_{ON}$ variation due to a change in the analog input voltage with a constant load current.

**$R_{ON}$ Match**

Difference between the $R_{ON}$ of any two channels.

**$I_S$ (OFF)**

Source leakage current with the switch off.

**$I_D$ (OFF)**

Drain leakage current with the switch off.

**$I_D$, $I_S$ (ON)**

Channel leakage current with the switch on.

**$V_D$ ($V_S$)**

Analog voltage on Terminals D, S.

**$C_S$ (OFF)**

OFF switch source capacitance.

**$C_D$ (OFF)**

OFF switch drain capacitance.

**$C_D$, $C_S$ (ON)**

ON switch capacitance.

**$t_{ON}$**

Delay between applying the digital control input and the output switching on.

**$t_{OFF}$**

Delay between applying the digital control input and the output switching off.

**$t_{OPEN}$**

Break-before-make delay when switches are configured as a multiplexer.

**$V_{INL}$**

Maximum input voltage for Logic 0.

**$V_{INH}$**

Minimum input voltage for Logic 1.

**$I_{INL}$ ($I_{INH}$)**

Input current of the digital input.

**Crosstalk**

A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

**Off Isolation**

A measure of unwanted signal coupling through an OFF switch.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

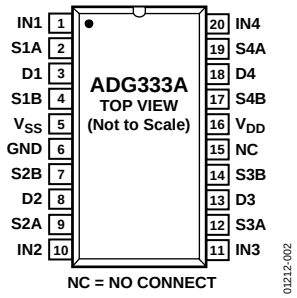



*Figure 2. PDIP Pin Configuration*

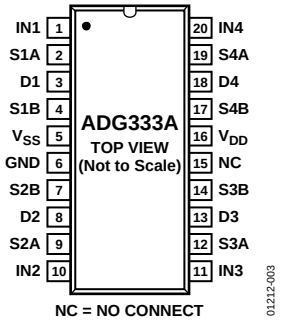



*Figure 3. SOIC Pin Configuration*

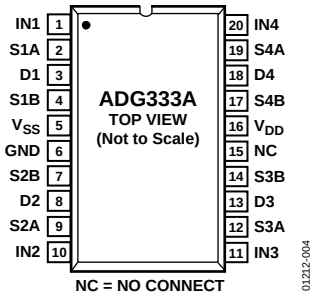



*Figure 4. SSOP Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 10, 11, 20 | IN1, IN2, IN3, IN4 | Logic Control Input. |
| 2, 4, 7, 9, 12, 14, 17, 19 | S1A, S1B, S2B, S2A, S3A, S3B, S4B, S4A | Source Terminal. Can be an input or output. |
| 3, 8, 13, 18 | D1, D2, D3, D4 | Drain Terminal. Can be an input or output. |
| 5 | $V_{SS}$ | Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground. |
| 6 | GND | Ground (0 V) Reference. |
| 15 | NC | No Connect. |
| 16 | $V_{DD}$ | Most Positive Power Supply Potential. |

# TYPICAL PERFORMANCE CHARACTERISTICS

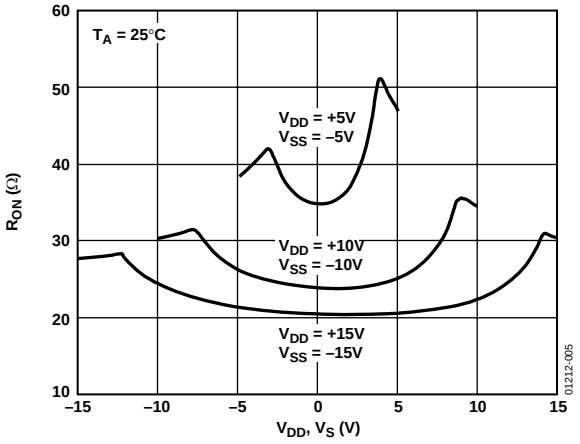



*Figure 5. $R_{ON}$ as a Function of $V_D$ ($V_S$): Dual Supply*

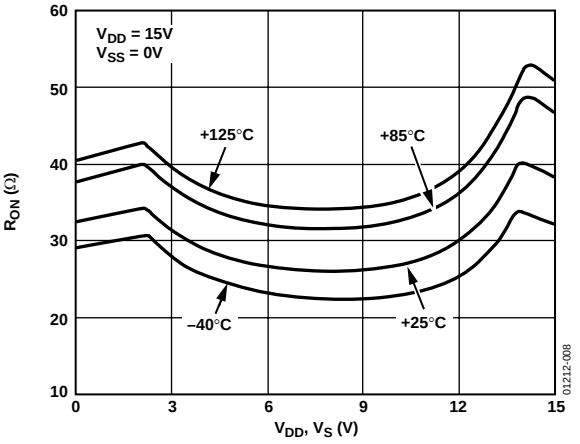



*Figure 8. $R_{ON}$ as a Function of $V_D$ ($V_S$) for Different Temperatures: Single Supply*

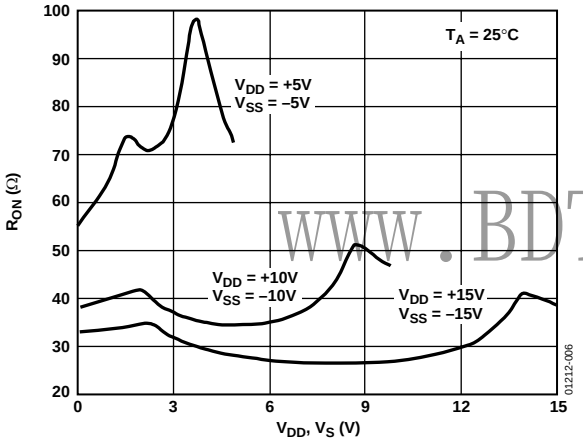



*Figure 6. $R_{ON}$ as a Function of $V_D$ ($V_S$): Single Supply*

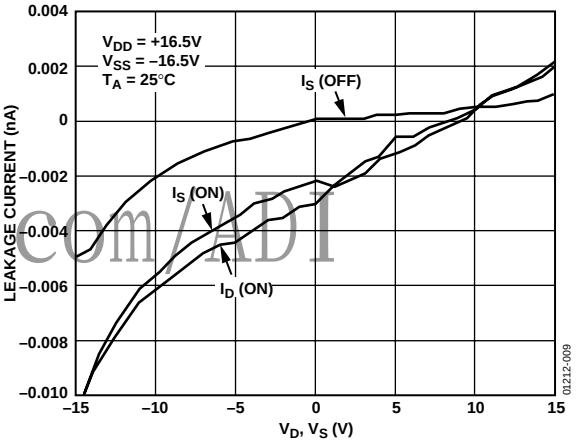



*Figure 9. Leakage Currents as a Function of $V_D$ ($V_S$): Dual Supply*

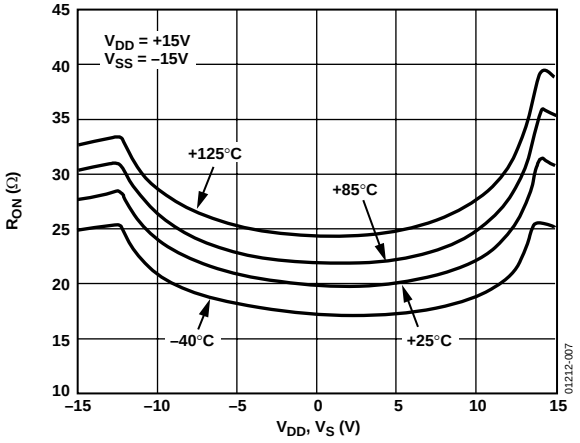



*Figure 7. $R_{ON}$ as a Function of $V_D$ ($V_S$) for Different Temperatures: Dual Supply*

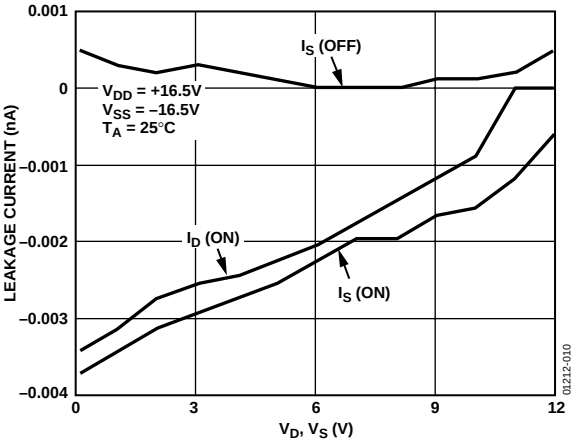



*Figure 10. Leakage Currents as a Function of $V_D$ ($V_S$): Single Supply*

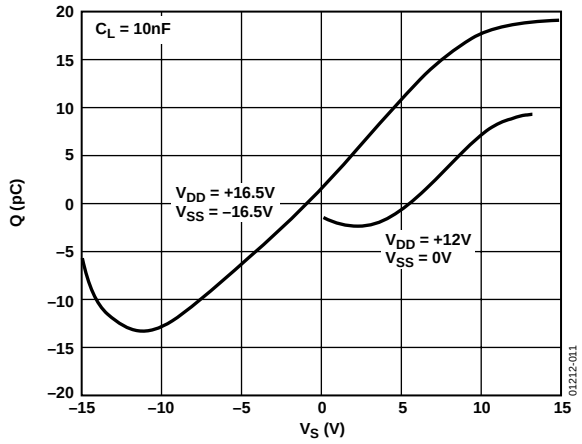



Figure 11. Charge Injection as a Function of $V_S$

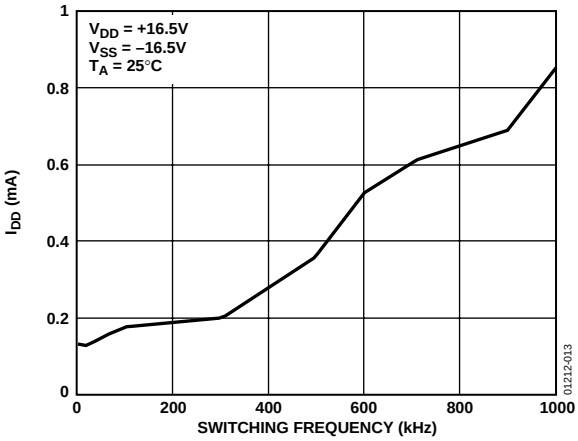



Figure 13. $I_{DD}$ as a Function of Switching Frequency

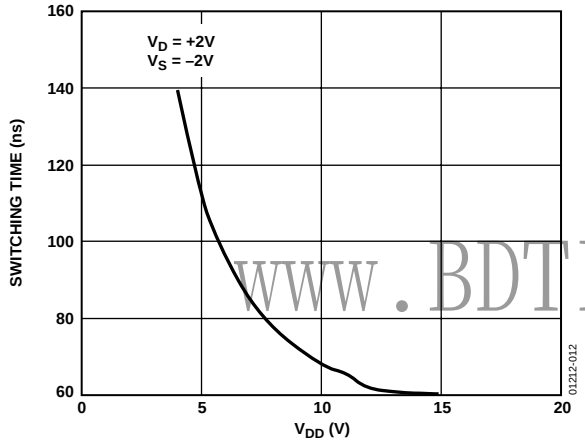



Figure 12. Switching Time as a Function of $V_D$

# TEST CIRCUITS

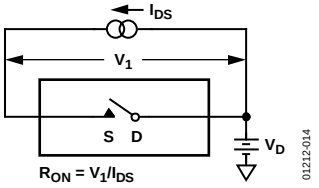



Figure 14. On Resistance

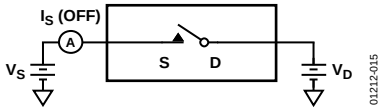



Figure 15. Off Leakage

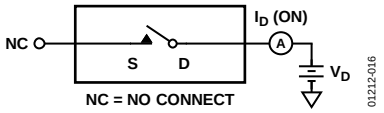
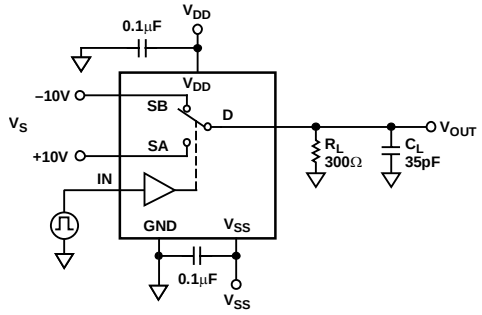



Figure 16. On Leakage



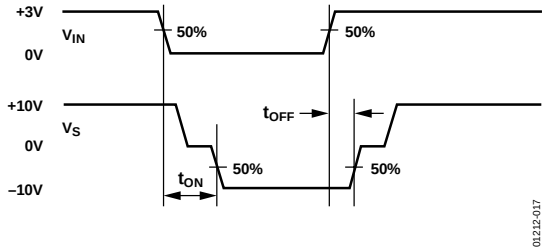
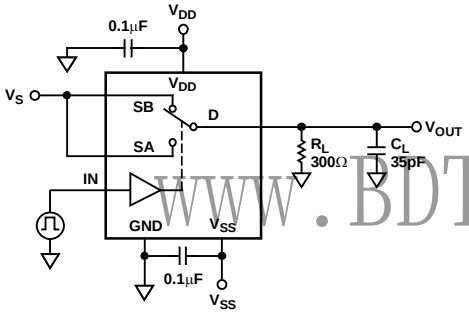




Figure 17. Switching Times



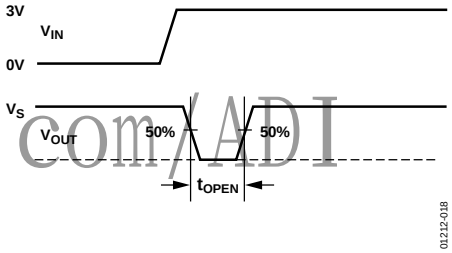
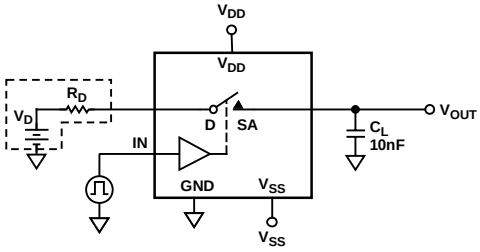






Figure 18. Break-Before-Make Delay, $t_{OPEN}$



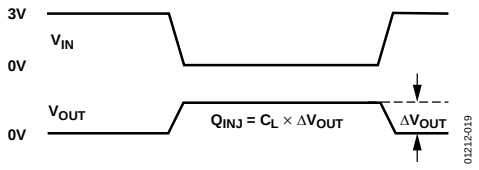




Figure 19. Charge Injection

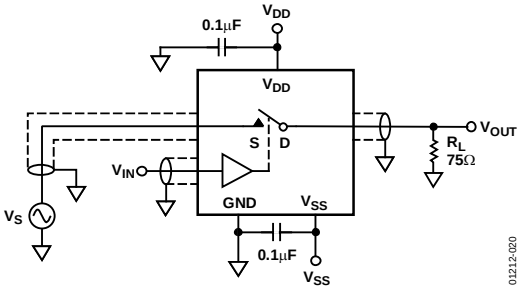



Figure 20. Off Isolation

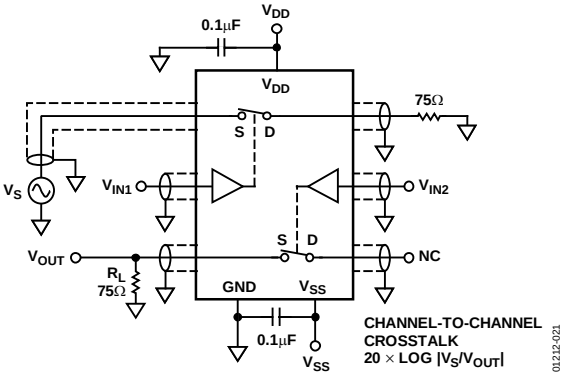



Figure 21. Channel-to-Channel Crosstalk

# APPLICATION INFORMATION

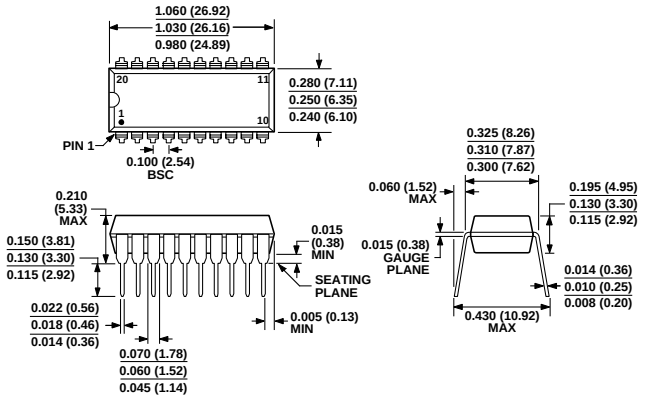
## ADG333A SUPPLY VOLTAGES

The ADG333A can operate from a dual or signal supply. $V_{SS}$ should be connected to GND when operating with a single supply. When using a dual supply, the ADG333A can also operate with unbalanced supplies; for example $V_{DD}$ = 20 V and $V_{SS}$ = −5 V. The only restrictions are that $V_{DD}$ to GND must not exceed 30 V, $V_{SS}$ to GND must not drop below −30 V, and $V_{DD}$ to $V_{SS}$ must not exceed +44 V. It is important to remember that the ADG333A supply voltage directly affects the input signal range, the switch on resistance and the switching times of the part. The effects of the power supplies on these characteristics can be clearly seen from the Typical Performance Characteristics curves.

## POWER SUPPLY SEQUENCING

When using CMOS devices, care must be taken to ensure correct power-supply sequencing. Incorrect power-supply sequencing can result in the device being subjected to stresses beyond those listed in the Absolute Maximum Ratings. This is also true for the ADG333A. Always turn on $V_{DD}$ first, followed by $V_{SS}$ and the logic signals. An external signal within the maximum specified ratings can then be safely presented to the source or drain of the switch

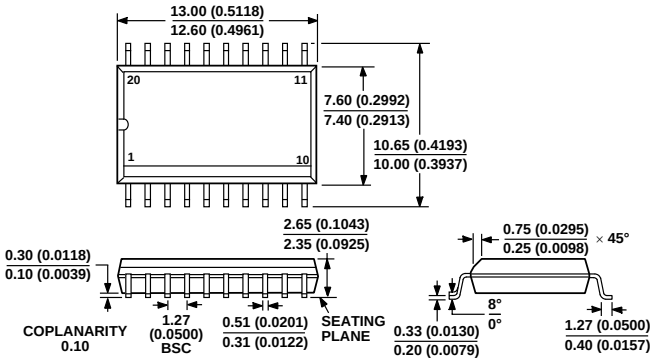
# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-001-AD

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

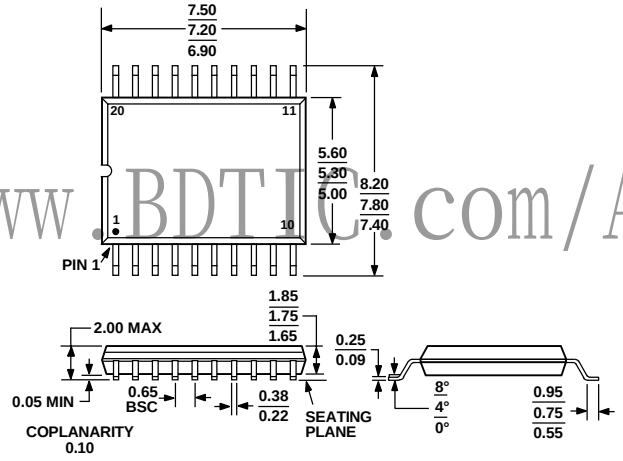
*Figure 22. 20-Lead Plastic Dual In-Line Package [PDIP]*
*Narrow Body (N-20)*
*Dimensions shown in inches and (millimeters)*




COMPLIANT TO JEDEC STANDARDS MS-013AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

*Figure 23. 20-Lead Standard Small Outline Package [SOIC]*
*Wide Body (R-20)*
*Dimensions shown in millimeters and (inches)*






COMPLIANT TO JEDEC STANDARDS MO-150AE

*Figure 24. 20-Lead Shrink Small Outline Package [SSOP]*
*(RS-20)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADG333ABN | −40°C to +85°C | 20-Lead Plastic Dual In-Line Package (PDIP) | N-20 |
| ADG333ABR | −40°C to +85°C | 20-Lead Standard Small Outline Package (SOIC) | R-20 |
| ADG333ABR-REEL | −40°C to +85°C | 20-Lead Standard Small Outline Package (SOIC) | R-20 |
| ADG333ABRZ[1] | −40°C to +85°C | 20-Lead Standard Small Outline Package (SOIC) | R-20 |
| ADG333ABRZ-REEL[1] | −40°C to +85°C | 20-Lead Standard Small Outline Package (SOIC) | R-20 |
| ADG333ABRS | −40°C to +85°C | 20-Lead Shrink Small Outline Package (SSOP) | RS-20 |
| ADG333ABRS-REEL | −40°C to +85°C | 20-Lead Shrink Small Outline Package (SSOP) | RS-20 |
| ADG333ABRSZ[1] | −40°C to +85°C | 20-Lead Shrink Small Outline Package (SSOP) | RS-20 |
| ADG333ABRSZ-REEL[1] | −40°C to +85°C | 20-Lead Shrink Small Outline Package (SSOP) | RS-20 |

[1] Z = Pb-free part.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