

FEATURES

- 1.5 Ω on resistance
- 0.3 Ω on-resistance flatness
- 0.1 Ω on-resistance match between channels
- Up to 400 mA continuous current
- Fully specified at +12 V, ± 15 V, and ± 5 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 14-lead TSSOP and 4 mm \times 4 mm, 16-lead LFCSP

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Communication systems
- Relay replacement

GENERAL DESCRIPTION

The ADG1404 is a complementary metal-oxide semiconductor (CMOS) analog multiplexer, comprising four single channels designed on an *i*CMOS[®] process. *i*CMOS (industrial CMOS) is a modular manufacturing process that combines high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

*i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

FUNCTIONAL BLOCK DIAGRAM

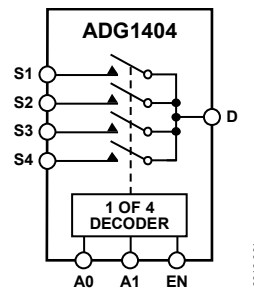


Figure 1.

The ADG1404 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. Logic 0 on the EN pin disables the device. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. 2.6 Ω maximum on resistance over temperature.
2. Minimum distortion.
3. Ultralow power dissipation: <0.03 μ W.
4. 14-lead TSSOP and 16-lead, 4 mm \times 4 mm LFCSP package.

Rev. 0

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REVISION HISTORY

7/08—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	1.5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 22
	1.8	2.3	2.6	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.3			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.03			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.55	± 2	± 12.5	nA max	$V_S = \pm 10\text{ V}$, $V_S = \mp 10\text{ V}$; see Figure 23
Drain Off Leakage, I_D (Off)	± 0.04			nA typ	
	± 0.55	± 4	± 30	nA max	$V_S = \pm 10\text{ V}$, $V_S = \mp 10\text{ V}$; see Figure 23
Channel On Leakage, I_D , I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 24
	± 2	± 4	± 30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	150			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	180	220	250	ns max	$V_S = +10\text{ V}$; see Figure 29
t_{ON} (EN)	100			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	120	145	165	ns max	$V_S = +10\text{ V}$; see Figure 31
t_{OFF} (EN)	110			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	135	165	185	ns max	$V_S = +10\text{ V}$; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	35			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 30
Charge Injection	−20			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	70			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 25
Channel-to-Channel Crosstalk	82			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.011			% typ	$R_L = 110\ \Omega$, 10 V p-p , $f = 20\text{ Hz}$ to 20 kHz ; see Figure 28
−3 dB Bandwidth	55			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
Insertion Loss	−0.17			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
C_S (Off)	23			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
C_D (Off)	90			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
C_D , C_S (On)	170			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
			1	μA max	Digital inputs = 0 V or V_{DD}
I_{DD}	170			μA typ	Digital inputs = 5 V
			280	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/max	$GND = 0\text{ V}$

¹ Guaranteed by design, not subject to production test.

ADG1404

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	2.8 3.5	4.3	4.8	Ω typ Ω max	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 22 $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels (ΔR_{ON})	0.13			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.21 0.6	0.23	0.25	Ω max Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	1.1	1.2	1.3	Ω max	
LEAKAGE CURRENTS					$V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$
Source Off Leakage, I_S (Off)	± 0.02 ± 0.55	± 2	± 12.5	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 23
Drain Off Leakage, I_D (Off)	± 0.03 ± 0.55	± 4	± 30	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 23
Channel On Leakage, I_D , I_S (On)	± 0.1 ± 1.5	± 4	± 30	nA typ nA max	$V_S = V_D = 1\text{ V or }10\text{ V}$; see Figure 24
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, $t_{TRANSITION}$	230 300	375	430	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 29
t_{ON} (EN)	180 240	295	335	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 31
t_{OFF} (EN)	115 160	190	220	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	100		10	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 30
Charge Injection	30			pC typ	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 25
Channel-to-Channel Crosstalk	82			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
−3 dB Bandwidth	35			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
Insertion Loss	−0.3			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
C_S (Off)	39			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
C_D (Off)	150			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
C_D , C_S (On)	217			pF typ	$f = 1\text{ MHz}$, $V_S = 6\text{ V}$
POWER REQUIREMENTS					$V_{DD} = 13.2\text{ V}$
I_{DD}	0.001		1	μA typ μA max	Digital inputs = 0 V or V_{DD}
I_{DD}	170		260	μA typ μA max	Digital inputs = 5 V
V_{DD}			5/16.5	V min/max	$GND = 0\text{ V}$, $V_{SS} = 0\text{ V}$

¹ Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{DD} to V _{SS}	V	
On Resistance (R _{ON})	3.3 4	4.9	5.4	Ω typ Ω max	V _S = ±4.5 V, I _S = −10 mA; see Figure 22 V _{DD} = +4.5 V, V _{SS} = −4.5 V
On-Resistance Match Between Channels (ΔR _{ON})	0.13			Ω typ	V _S = ±4.5 V, I _S = −10 mA
On-Resistance Flatness (R _{FLAT(ON)})	0.22	0.23	0.25	Ω max	V _S = ±4.5 V, I _S = −10 mA
	0.9			Ω typ	
	1.1	1.24	1.31	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.02			nA typ	V _{DD} = +5.5 V, V _{SS} = −5.5 V V _S = ±4.5 V, V _D = ∓4.5 V; see Figure 23
Drain Off Leakage, I _D (Off)	±0.2	±1	±12.5	nA max	V _S = ±4.5 V, V _D = ∓4.5 V; see Figure 23
	±0.02			nA typ	
Channel On Leakage, I _D , I _S (On)	±0.25	±1.2	±15	nA max	V _S = V _D = ±4.5 V; see Figure 24
	±0.05			nA typ	
	±0.25	±1.5	±20	nA typ	
				nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	V _{IN} = V _{GND} or V _{DD}
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.001		±0.1	μA typ μA max	
Digital Input Capacitance, C _{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, t _{TRANSITION}	340	560	615	ns typ	R _L = 300 Ω, C _L = 35 pF
	470			ns max	V _S = 3 V; Figure 29
t _{ON} (EN)	260	430	480	ns typ	R _L = 300 Ω, C _L = 35 pF
	355			ns max	V _S = 3 V; Figure 31
t _{OFF} (EN)	220	365	400	ns typ	R _L = 300 Ω, C _L = 35 pF
	315			ns max	V _S = 3 V; Figure 31
Break-Before-Make Time Delay, t _{BBM}	100		50	ns typ	R _L = 300 Ω, C _L = 35 pF
				ns min	V _{S1} = V _{S2} = 3 V; see Figure 30
Charge Injection	30			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 32
Off Isolation	80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 25
Channel-to-Channel Crosstalk	82			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 27
−3 dB Bandwidth	40			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 26
Insertion Loss	0.27			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 26
Total Harmonic Distortion + Noise	0.03			% typ	R _L = 110 Ω, 2.5 V p-p, f = 20 Hz to 20 kHz; see Figure 28
C _S (Off)	33			pF typ	V _S = 0 V, f = 1 MHz
C _D (Off)	128			pF typ	V _S = 0 V, f = 1 MHz
C _D , C _S (On)	210			pF typ	V _S = 0 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.001		1	μA typ μA max	V _{DD} = 5.5 V, V _{SS} = −5.5 V Digital inputs = 0 V, 5 V, or V _{DD}
I _{SS}	0.001		1	μA typ μA max	Digital inputs = 0 V or V _{DD}
V _{DD} /V _{SS}			±4.5/±16.5	V min/max	GND = 0 V

¹ Guaranteed by design, not subject to production test.

ADG1404

CONTINUOUS CURRENT, S OR D

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, S or D ¹					
15 V Dual Supply					$V_{DD} = +13.5\text{ V}, V_{SS} = -13.5\text{ V}$
ADG1404 TSSOP	350	220	100	mA max	
ADG1404 LFCSP	450	300	140	mA max	
12 V Single Supply					$V_{DD} = 10.8\text{ V}, V_{SS} = 0\text{ V}$
ADG1404 TSSOP	300	220	100	mA max	
ADG1404 LFCSP	400	300	140	mA max	
5 V Dual Supply					$V_{DD} = +4.5\text{ V}, V_{SS} = -4.5\text{ V}$
ADG1404 TSSOP	300	220	100	mA max	
ADG1404 LFCSP	400	300	140	mA max	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	–0.3 V to +25 V
V_{SS} to GND	+0.3 V to –25 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs	GND – 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D ²	Data + 15%
Operating Temperature Range	
Automotive (Y Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
14-Lead TSSOP, θ_{JA} Thermal Impedance (4-layer board)	112°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature, Pb free	260(+0/–5)°C

¹ Overvoltages at IN, S, and D are clamped by internal diodes. Current should be limited to the maximum ratings given.

² See data given in Table 4.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG1404

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

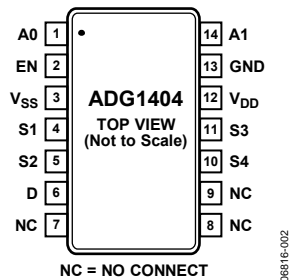


Figure 2. TSSOP Pin Configuration

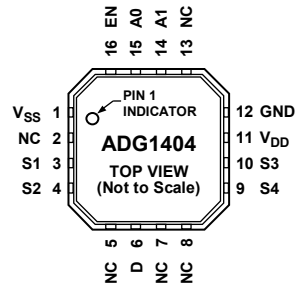


Figure 3. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches.
3	1	V _{SS}	Most Negative Power Supply Potential.
4	3	S1	Source Terminal. Can be an input or an output.
5	4	S2	Source Terminal. Can be an input or an output.
6	6	D	Drain Terminal. Can be an input or an output.
7 to 9	2, 5, 7, 8, 13	NC	No Connection.
10	9	S4	Source Terminal. Can be an input or an output.
11	10	S3	Source Terminal. Can be an input or an output.
12	11	V _{DD}	Most Positive Power Supply Potential.
13	12	GND	Ground (0 V) Reference.
14	14	A1	Logic Control Input.

TRUTH TABLE

Table 7.

EN	A1	A0	S1	S2	S3	S4
0	X	X	Off	Off	Off	Off
1	0	0	On	Off	Off	Off
1	0	1	Off	On	Off	Off
1	1	0	Off	Off	On	Off
1	1	1	Off	Off	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

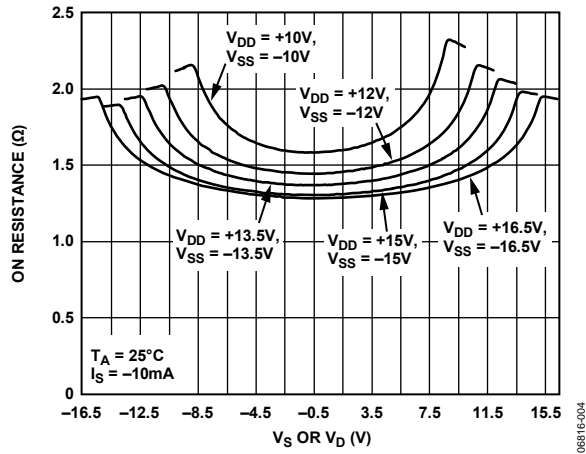


Figure 4. On Resistance as a Function of V_D (V_S), Dual Supply

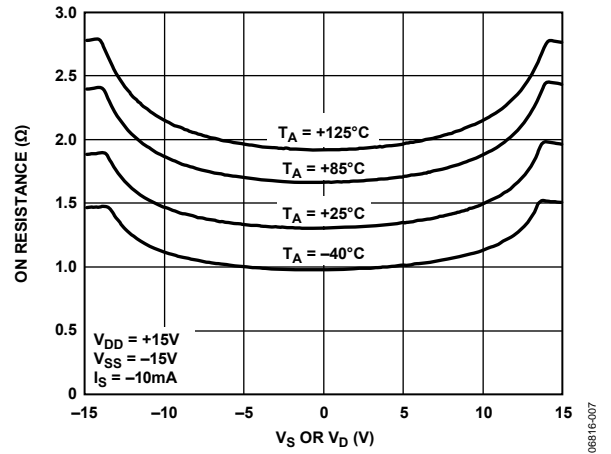


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, 15 V Dual Supply

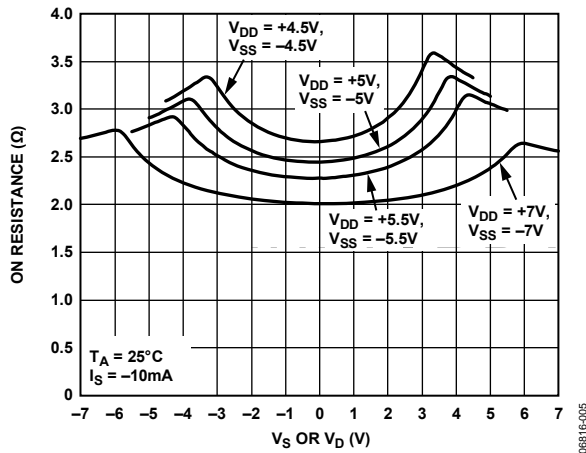


Figure 5. On Resistance as a Function of V_D (V_S), Dual Supply

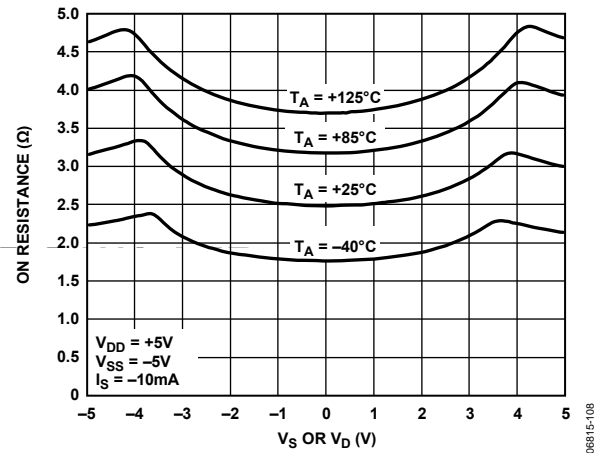


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, 5 V Dual Supply

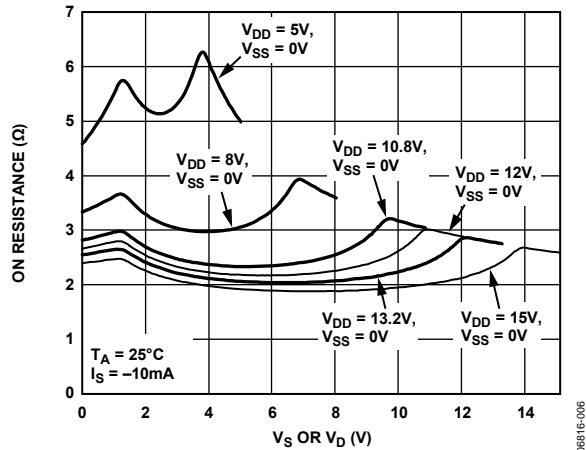


Figure 6. On Resistance as a Function of V_D (V_S), Single Supply

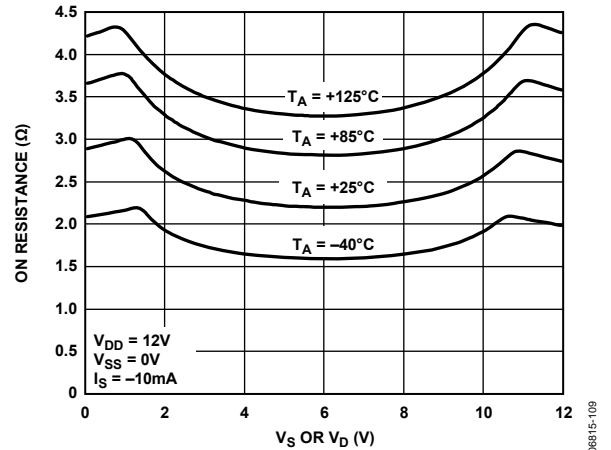


Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

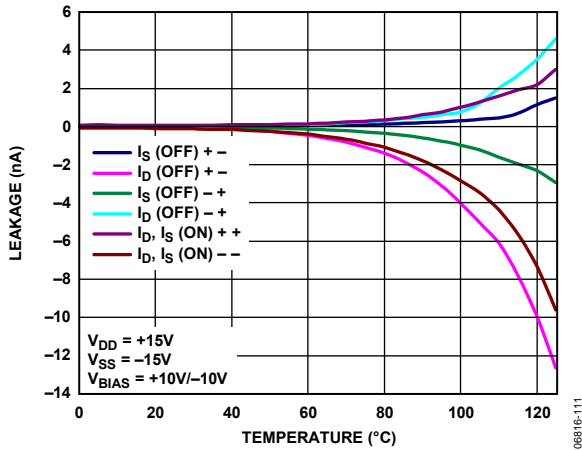


Figure 10. Leakage Currents as a Function of Temperature, 15 V Dual Supply

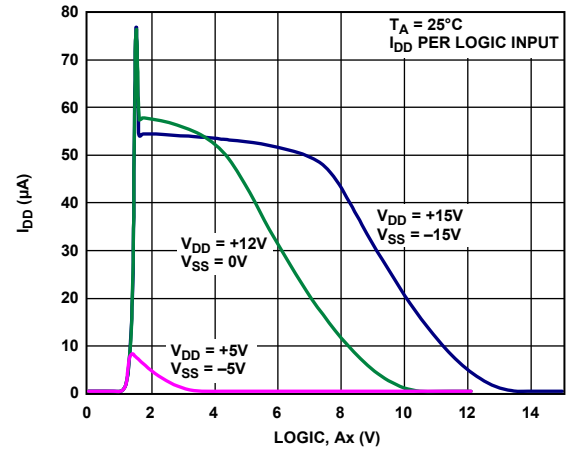


Figure 13. I_{DD} vs. Logic Level

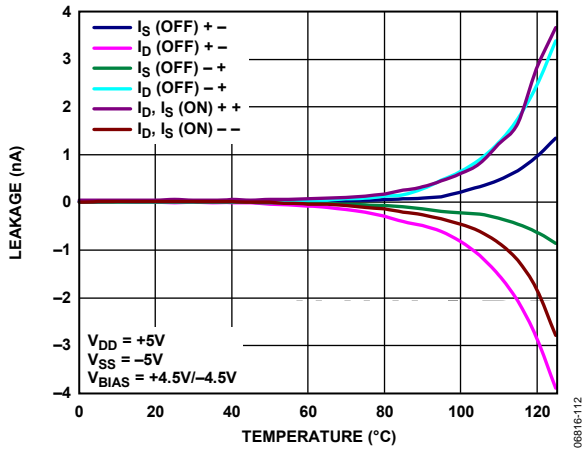


Figure 11. Leakage Currents as a Function of Temperature, 5 V Dual Supply

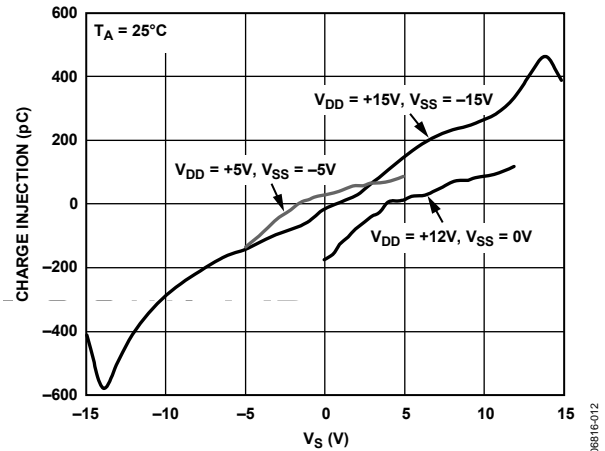


Figure 14. Charge Injection vs. Source Voltage

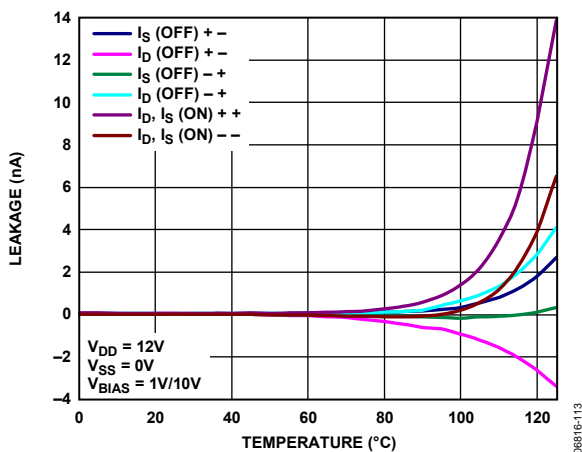


Figure 12. Leakage Currents as a Function of Temperature, 12 V Single Supply

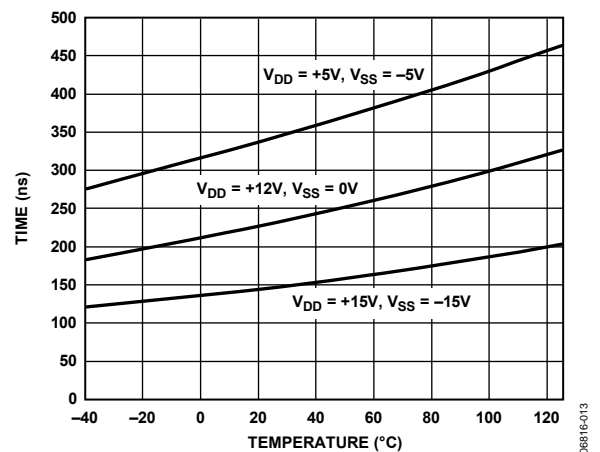


Figure 15. Transition Times vs. Temperature

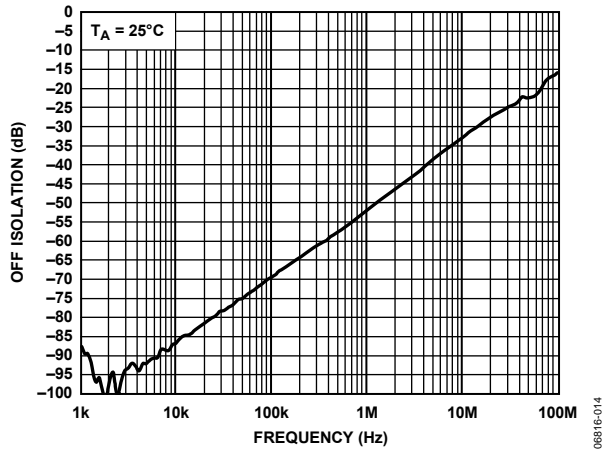


Figure 16. Off Isolation vs. Frequency

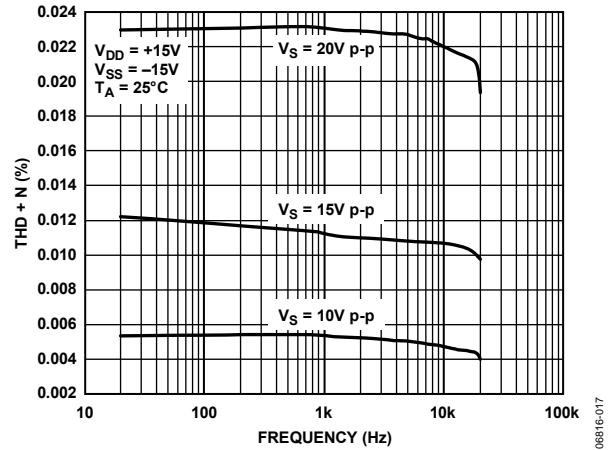


Figure 19. THD + N vs. Frequency at ± 15 V

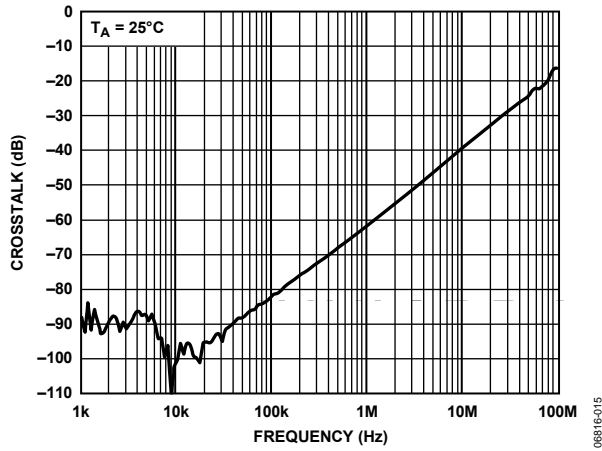


Figure 17. Crosstalk vs. Frequency

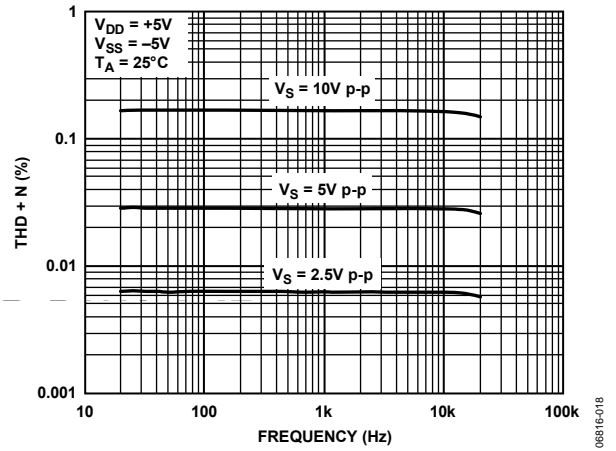


Figure 20. THD + N vs. Frequency at ± 5 V

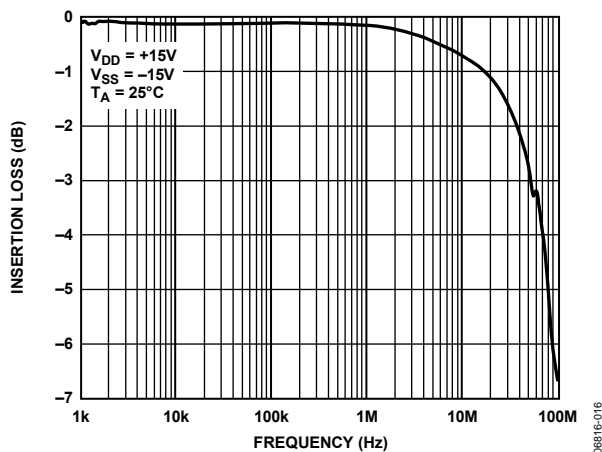


Figure 18. On Response vs. Frequency

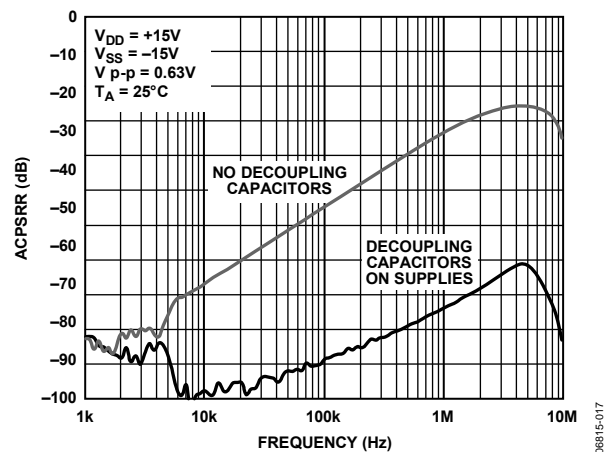


Figure 21. ACPSRR vs. Frequency

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D (V_S)

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

R_{FLAT(ON)}

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL} (I_{INH})

The input current of the digital input.

C_S (Off)

The off switch source capacitance, which is measured with reference to ground.

C_D (Off)

The off switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)

The on switch capacitance, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{TRANSITION}

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

t_{ON} (EN)

The delay between applying the digital control input and the output switching on. See Figure 29, Test Circuit 4.

t_{OFF} (EN)

The delay between applying the digital control input and the output switching off.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

ACPSRR (AC Power Supply Rejection Ratio)

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the part's ability to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

TEST CIRCUITS

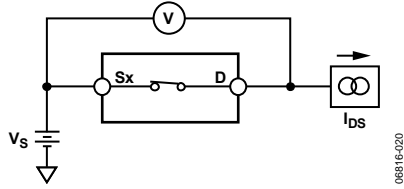


Figure 22. On Resistance

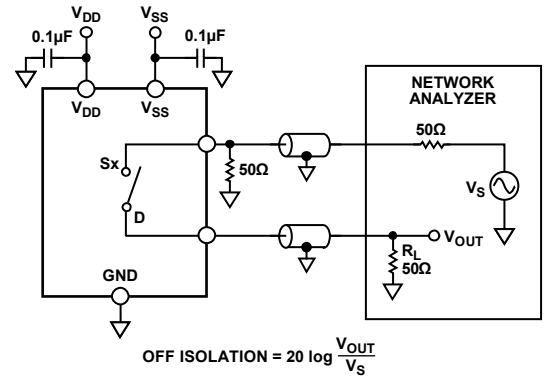


Figure 25. Off Isolation

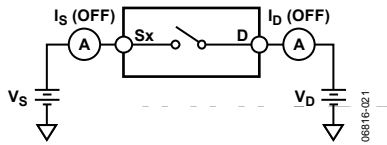


Figure 23. Off Leakage

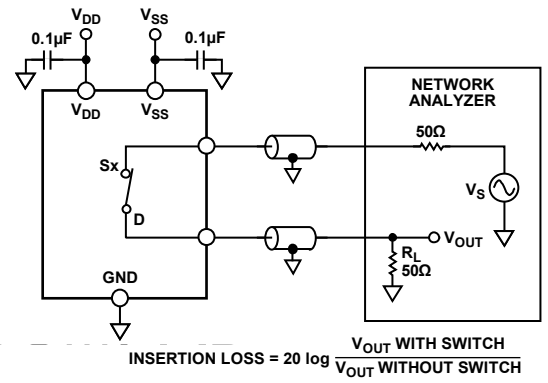


Figure 26. Bandwidth

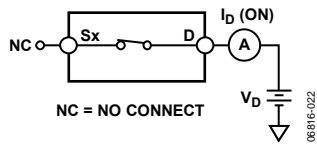


Figure 24. On Leakage

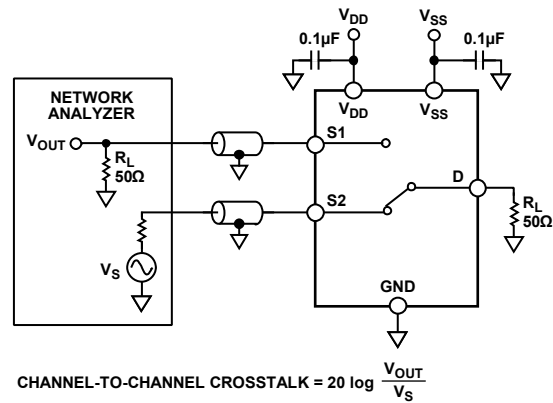


Figure 27. Channel-to-Channel Crosstalk

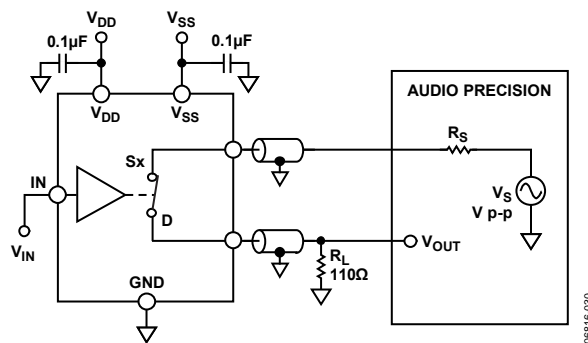


Figure 28. THD + Noise

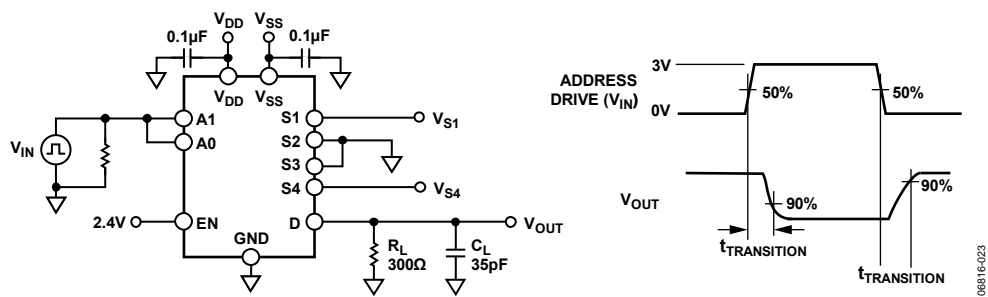


Figure 29. Address to Output Switching Times

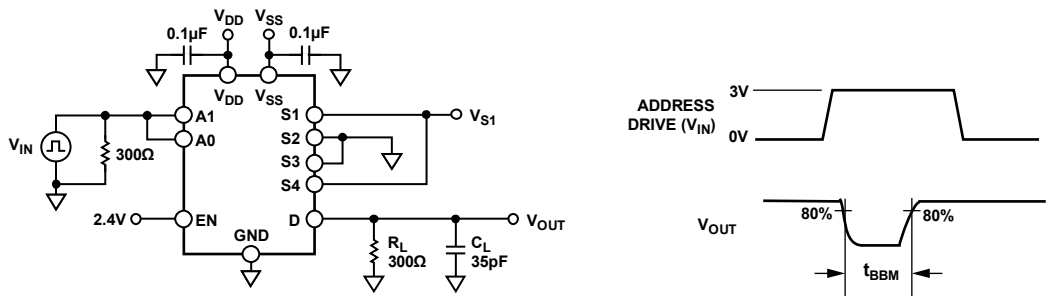


Figure 30. Break-Before-Make Time Delay

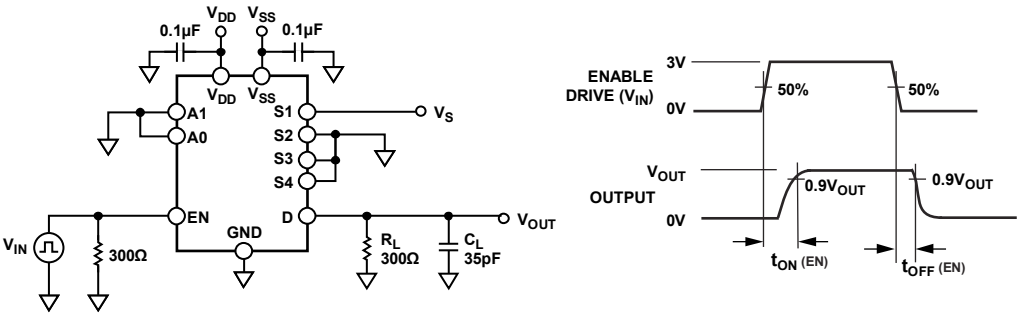


Figure 31. Enable-to-Output Switching Delay

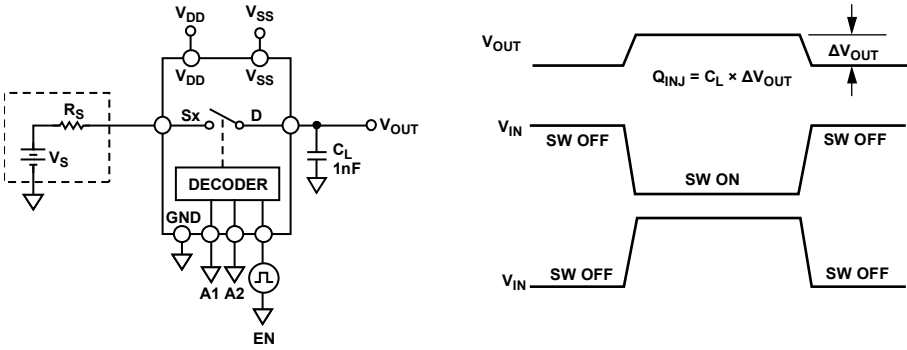
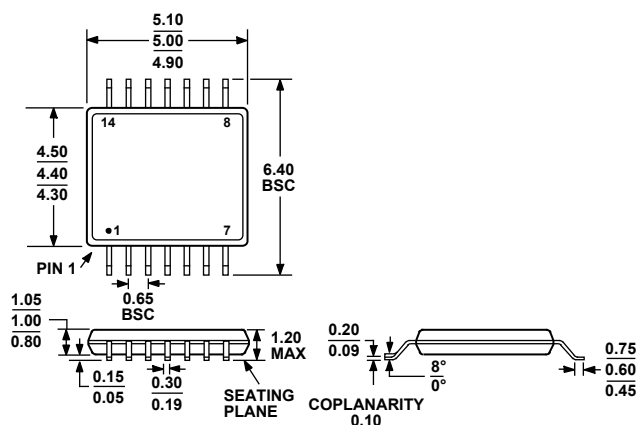


Figure 32. Charge Injection

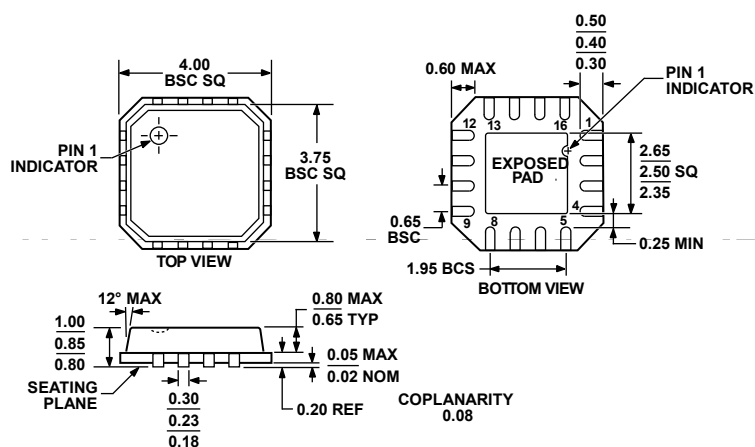
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 33. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimension shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-13)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1404YRUZ ¹	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package (TSSOP)	RU-14
ADG1404YRUZ-REEL7 ¹	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package (TSSOP)	RU-14
ADG1404YCPZ-REEL ¹	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13
ADG1404YCPZ-REEL7 ¹	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-13

¹ Z = RoHS Compliant Part.