Low Capacitance, Low Charge Injection, ±15 V/12 V *i*CMOS™, Dual SPDT Switch

ADG1236

FEATURES

1.3 pF off capacitance
3.5 pF on capacitance
1 pC charge injection
33 V supply range
120 Ω on resistance
Fully specified at +12 V, ±15 V
No V_L supply required
3 V logic-compatible inputs
Rail-to-rail operation
16-lead TSSOP and 12-lead LFCSP packages
Typical power consumption: <0.03 μW

APPLICATIONS

Automatic test equipment
Data acquisition systems
Battery-powered systems
Sample-and-hold systems
Audio/video signal routing
Communication systems

FUNCTIONAL BLOCK DIAGRAM

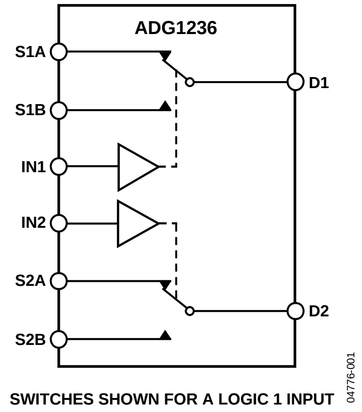


Figure 1.

GENERAL DESCRIPTION

The ADG1236 is a monolithic CMOS device containing two independently selectable SPDT switches. It is designed on an *i*CMOS process. *i*CMOS (industrial CMOS) is a modular manufacturing process combining high voltage complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of the part make it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth makes the part suitable for video signal switching. *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

PRODUCT HIGHLIGHTS

1. 1.3 pF off capacitance (±15 V supply).
2. 1 pC charge injection.
3. 3 V logic-compatible digital inputs: $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V.
4. No V_L logic power supply required.
5. Ultralow power dissipation: <0.03 μW.
6. 16-lead TSSOP and 12-lead 3 mm × 3 mm LFCSP packages.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

9/05—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

	Y Version[1]				
Parameters	**25°C**	**−40°C to +85°C**	**−40°C to +125°C**	**Unit**	**Test Conditions/Comments[1]**
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	120			Ω typ	V_S = ±10 V, I_S = −1 mA; Figure 20
	190	230	260	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels (ΔR_{ON})	3.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	6	10	12	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	20			Ω typ	V_S = −5 V, 0 V, +5 V; I_S = −1 mA
	57	72	79	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = ±10 V, V_S = ∓10 V; Figure 21
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = ±10 V, V_S = ∓10 V; Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = ±10 V; Figure 22
	±0.2	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, t_{TRANS} A_{OFF} B_{ON}	125			ns typ	R_L = 300 Ω, C_L = 35 pF
	150		200	ns max	V_S = 10 V; Figure 23
Transition Time, t_{TRANS} B_{OFF} A_{ON}	70			ns typ	R_L = 300 Ω, C_L = 35 pF
	90		115	ns max	V_S = 10 V; Figure 23
Break-Before-Make Time Delay, t_D	25			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 10 V; Figure 24
Charge Injection	−1			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 25
Off Isolation	80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 26
Channel-to-Channel Crosstalk	85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 27
Total Harmonic Distortion + Noise	0.15			% typ	R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz
−3 dB Bandwidth	1000			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 28
C_S (Off)	1.3			pF typ	f = 1 MHz; V_S = 0 V
	1.6			pF max	f = 1 MHz; V_S = 0 V
C_D, C_S (On)	3.5			pF typ	f = 1 MHz; V_S = 0 V
	4.3			pF max	f = 1 MHz; V_S = 0 V

Parameters	Y Version[1] 25°C	 −40°C to +85°C	 −40°C to +125°C	Unit	Test Conditions/Comments[1]
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	170			μA typ	Digital inputs = 5 V
			230	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 5 V
			1.0	μA max	

[1] Temperature range for Y version is −40°C to +125°C.
[2] Guaranteed by design; not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

	Y Version[1]				
Parameters	**25°C**	**−40°C to +85°C**	**−40°C to +125°C**	**Unit**	**Test Conditions/Comments**
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	300			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA; Figure 20
	475	567	625	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	4.5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	16	26	27	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	60			Ω typ	V_S = 3 V, 6 V, 9 V, I_S = −1 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; Figure 21
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 10 V, Figure 22
	±0.2	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, t_{TRANS} B_{OFF} A_{ON}	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	140		175	ns max	V_S = 8 V; Figure 23
Transition Time, t_{TRANS} A_{OFF} B_{ON}	155			ns typ	R_L = 300 Ω, C_L = 35 pF
	190		255	ns max	V_S = 8 V; Figure 23
Break-Before-Make Time Delay, t_D	50			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 8 V; Figure 24
Charge Injection	−0.8			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; Figure 25
Off Isolation	75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 26;
Channel-to-Channel Crosstalk	85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 27
−3 dB Bandwidth	800			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 28
C_S (Off)	1.6			pF typ	f = 1 MHz; V_S = 6 V
	1.9			pF max	f = 1 MHz; V_S = 6 V
C_D, C_S (On)	4			pF typ	f = 1 MHz; V_S = 6 V
	4.9			pF max	f = 1 MHz; V_S = 6 V
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{DD}	170			µA typ	Digital inputs = 5 V
			230	µA max	

[1] Temperature range for Y version is −40°C to +125°C.

[2] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current per Channel, S or D	25 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance	112°C/W
12-Lead LFCSP, θ_{JA} Thermal Impedance	80°C/W
Reflow Soldering Peak Temperature, Pb Free	260°C

[1] Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE FOR SWITCHES

Table 4.

IN	Switch A	Switch B
0	Off	On
1	On	Off

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

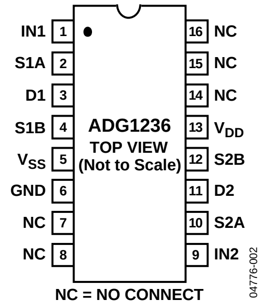


Figure 2. TSSOP Pin Configuration

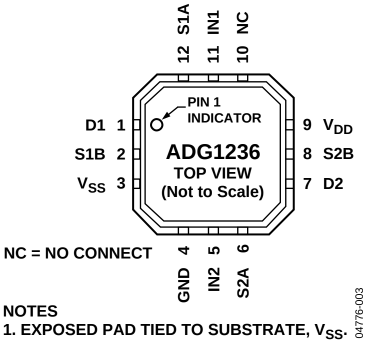


Figure 3. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	11	IN1	Logic Control Input.
2	12	S1A	Source Terminal. Can be an input or output.
3	1	D1	Drain Terminal. Can be an input or output.
4	2	S1B	Source Terminal. Can be an input or output.
5	3	V_{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14 to 16	10	NC	No Connect.
9	5	IN2	Logic Control Input.
10	6	S2A	Source Terminal. Can be an input or output.
11	7	D2	Drain Terminal. Can be an input or output.
12	8	S2B	Source Terminal. Can be an input or output.
13	9	V_{DD}	Most Positive Power Supply Potential.

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminals D and S.

R_{ON}
The ohmic resistance between D and S.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)

The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{TRANS}
The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

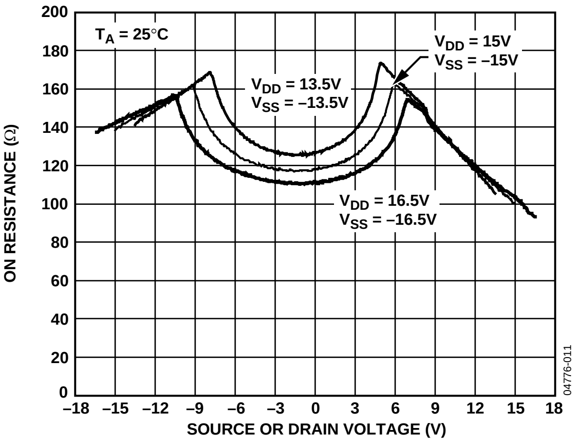


Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

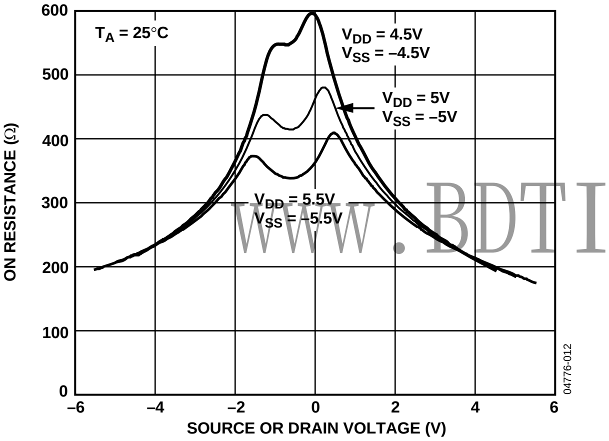


Figure 5. On Resistance as a Function of V_D (V_S) for Dual Supply

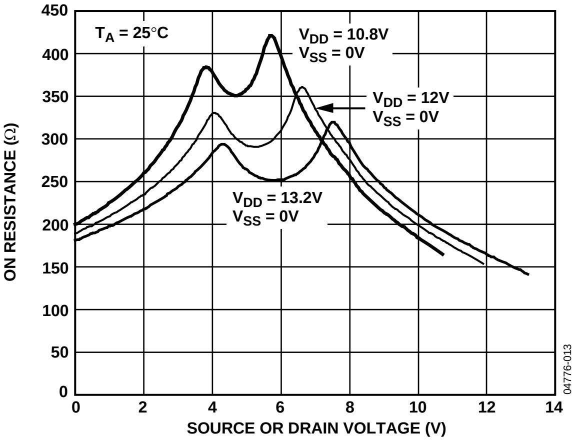


Figure 6. On Resistance as a Function of V_D (V_S) for Single Supply

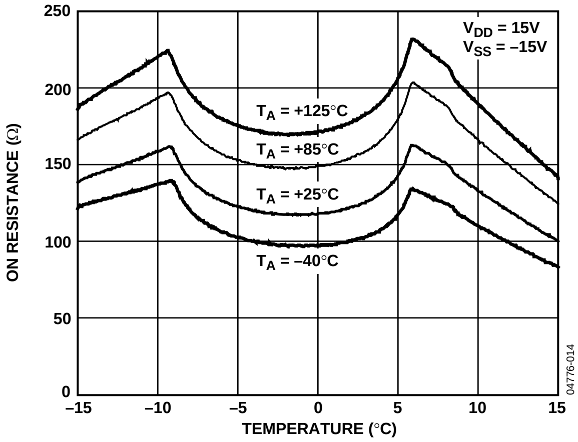


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

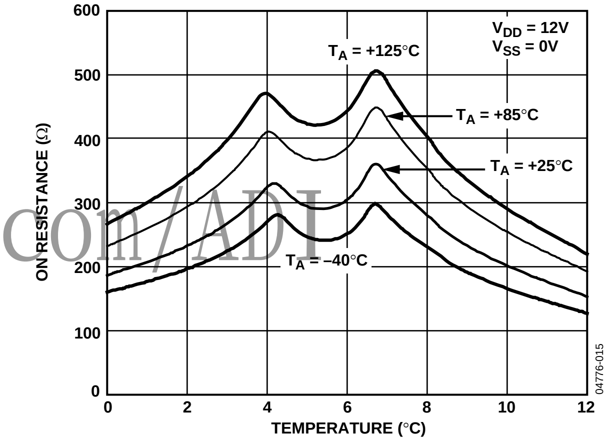


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

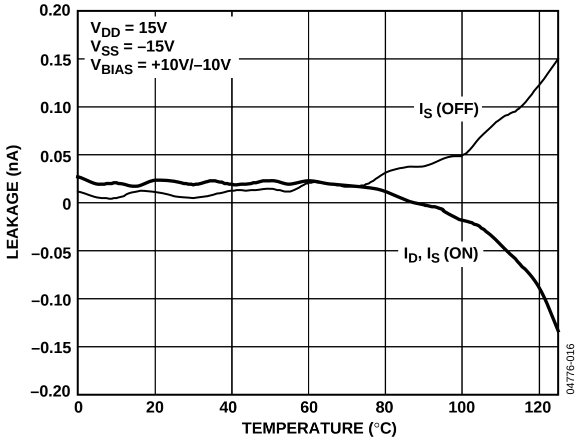


Figure 9. Leakage Currents as a Function of Temperature, Dual Supply

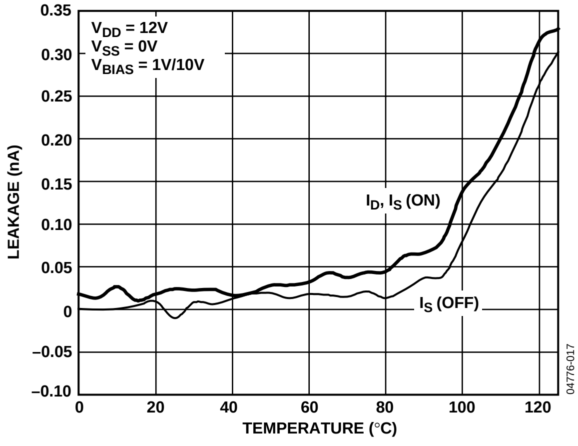


Figure 10. Leakage Currents as a Function of Temperature, Single Supply

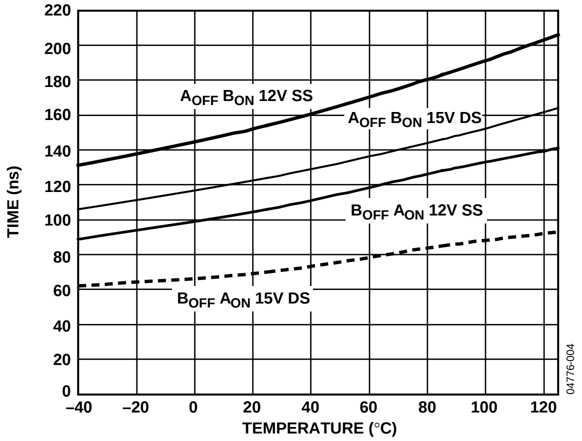


Figure 13. $t_{TRANSITION}$ Times vs. Temperature

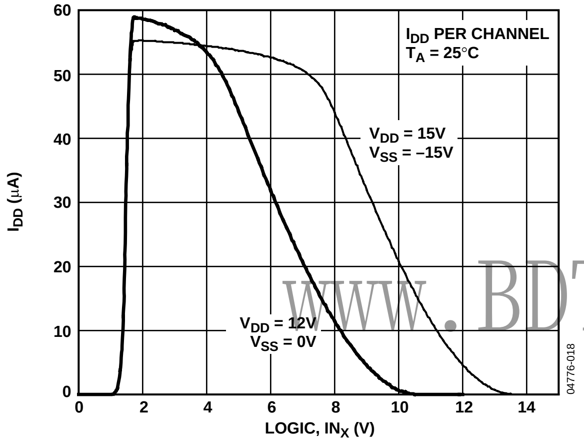


Figure 11. I_{DD} vs. Logic Level

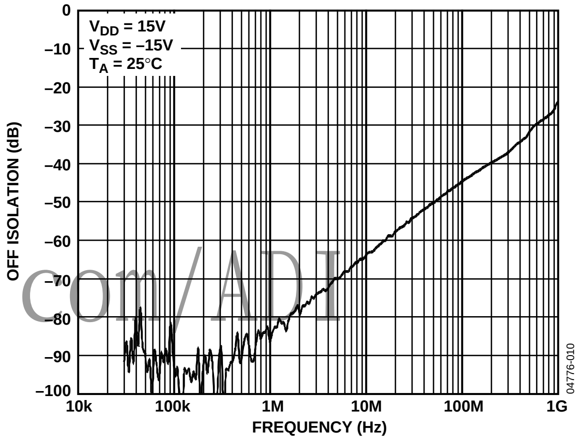


Figure 14. Off Isolation vs. Frequency

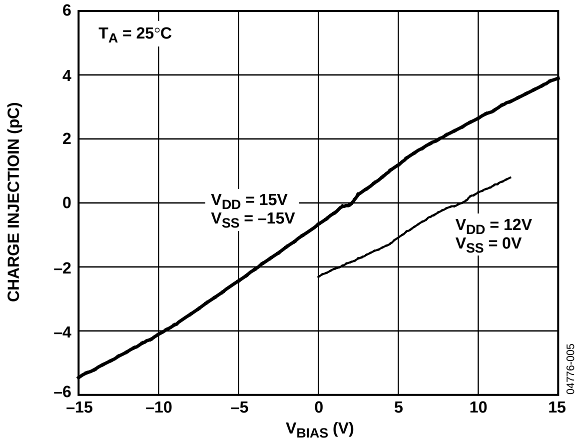


Figure 12. Charge Injection vs. Source Voltage

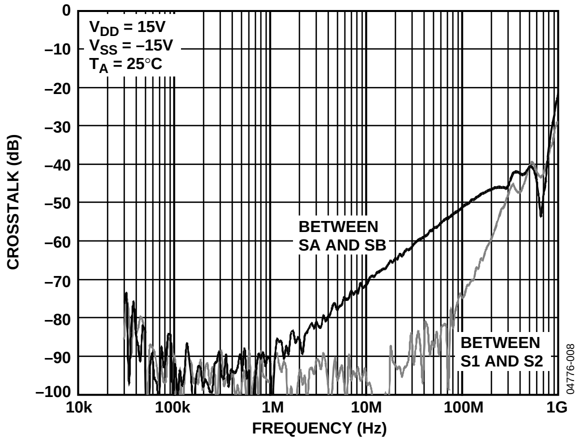


Figure 15. Crosstalk vs. Frequency

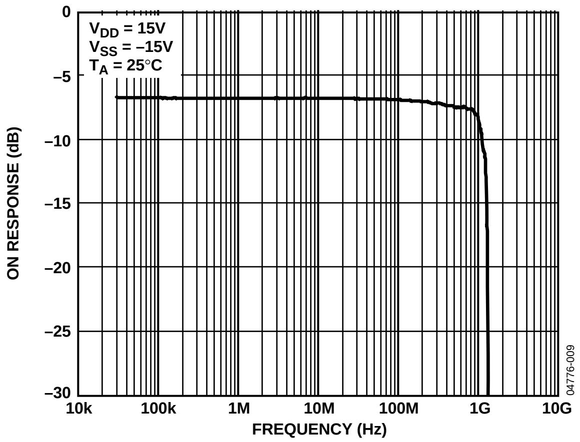


Figure 16. On Response vs. Frequency

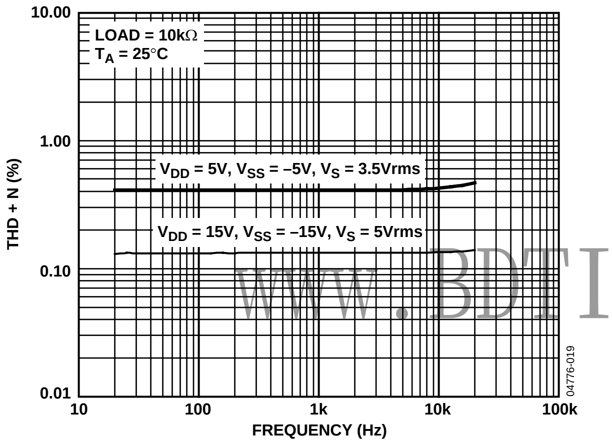


Figure 17. THD + N vs. Frequency

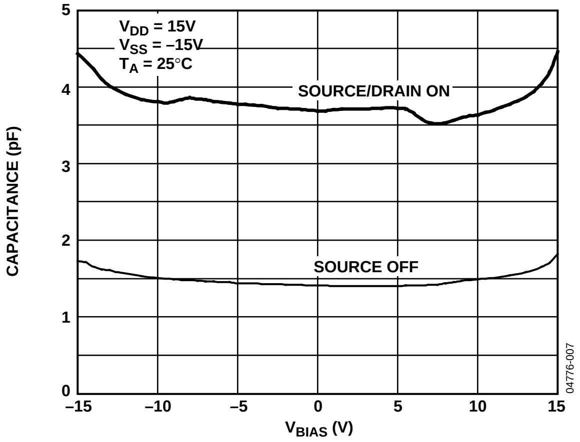


Figure 18. Capacitance vs. Source Voltage for Dual Supply

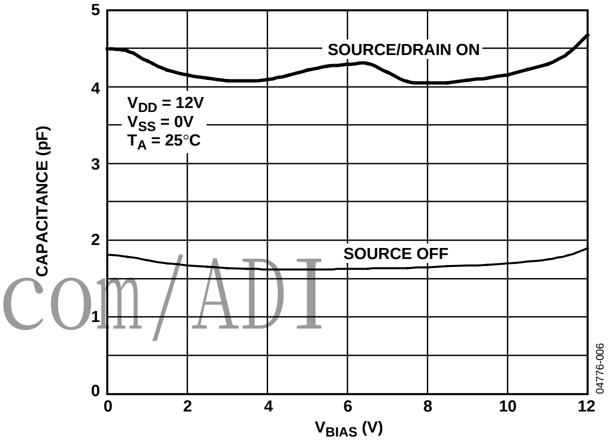


Figure 19. Capacitance vs. Source Voltage for Single Supply

TEST CIRCUITS

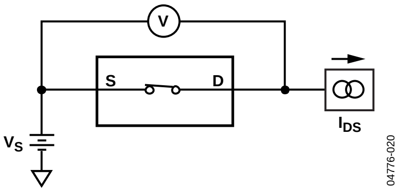


Figure 20. Test Circuit 1—On Resistance

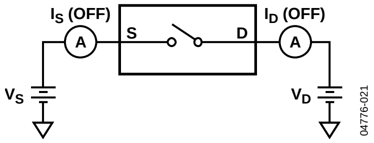


Figure 21. Test Circuit 2—Off Resistance

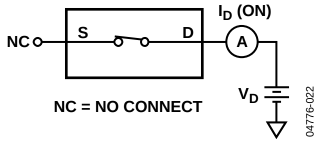


Figure 22. Test Circuit 3—On Leakage

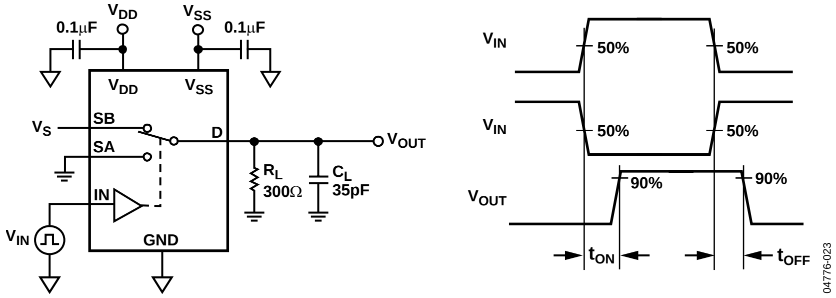


Figure 23. Test Circuit 4—Switching Times

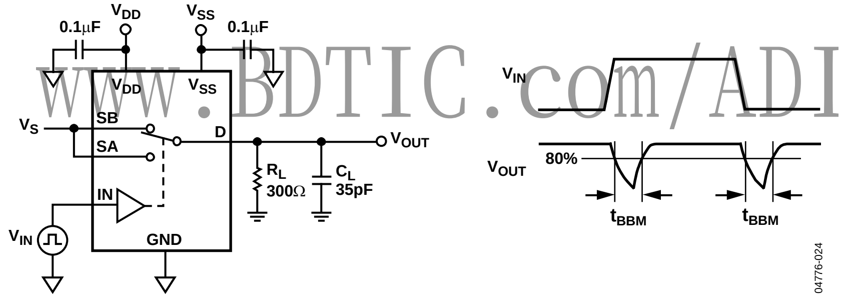


Figure 24. Test Circuit 5—Break-Before-Make Time Delay

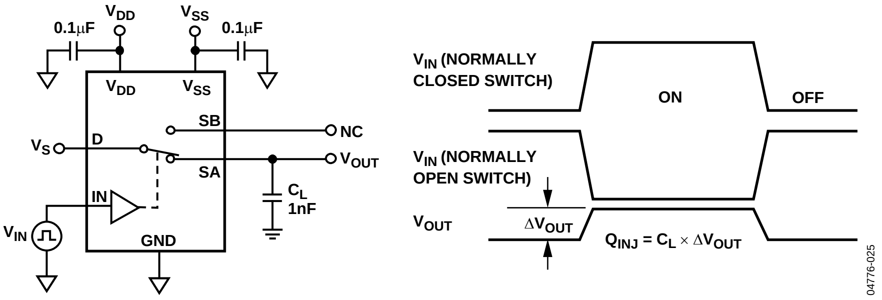


Figure 25. Test Circuit 6—Charge Injection

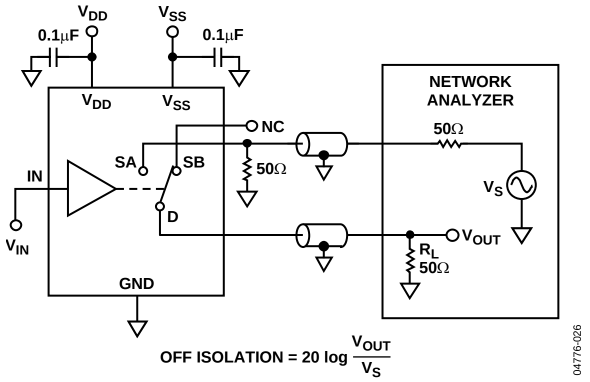


Figure 26. Test Circuit 7—Off Isolation

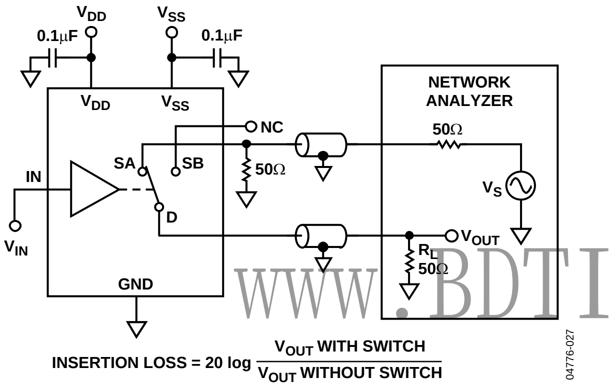


Figure 27. Test Circuit 8—Channel-to-Channel Crosstalk

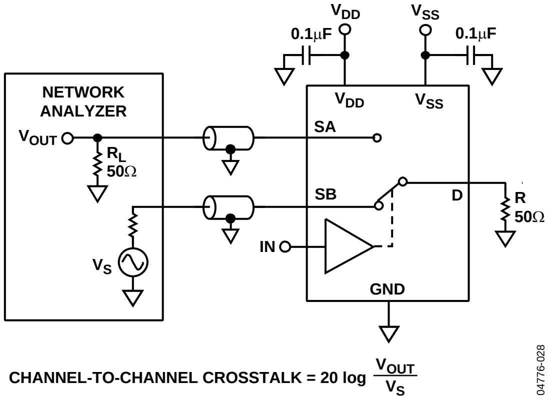


Figure 28. Test Circuit 9—Bandwidth

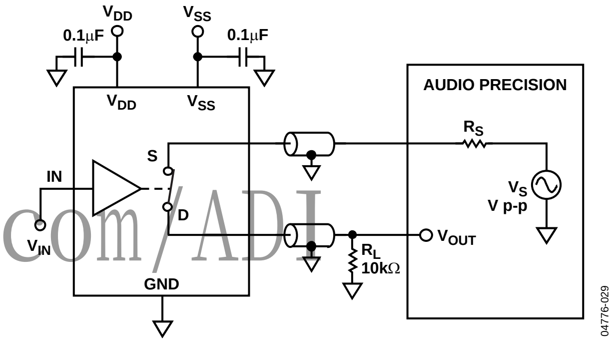
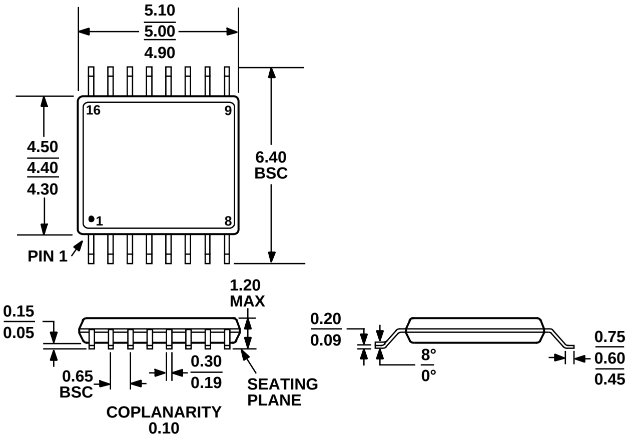


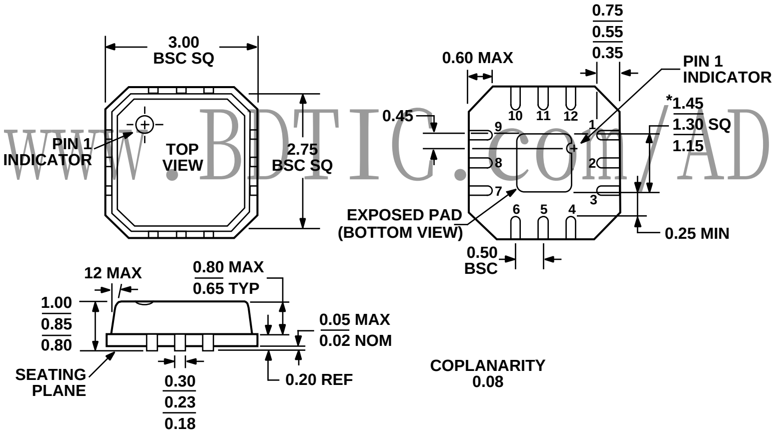
Figure 29. Test Circuit 10—THD + Noise

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-1
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 31. 12-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-12-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1236YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1236YRUZ-REEL[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1236YRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1236YCPZ-500RL7[1]	−40°C to +125°C	12-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-12-1
ADG1236YCPZ-REEL7[1]	−40°C to +125°C	12-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-12-1

[1] Z = Pb-free part.

NOTES

NOTES

D04776–0–9/05(0)