Dual 0.275% Comparators and Reference with Programmable Hysteresis

ADCMP341/ADCMP343

FEATURES

400 mV ± 0.275% threshold
User programmable hysteresis via resistor string
Supply range: 1.7 V to 5.5 V
Low quiescent current: 6.5 μA typical
Input range includes ground
Low input bias current: ±5 nA maximum
Open-drain outputs
Supports wired-AND connections
Input polarities:
  ADCMP341 noninverting
  ADCMP343 inverting
Small SOT-23 package

APPLICATIONS

Portable applications
Li-Ion monitoring
Handheld instruments
LED/relay driving
Optoisolator driving
Control systems

GENERAL DESCRIPTION

The ADCMP341/ADCMP343 consist of two low power, high accuracy comparators with a 400 mV reference in an 8-lead SOT-23 package. Operating within a supply range of 1.7 V to 5.5 V, the devices only draw 6.5 μA (typical), making them ideal for low voltage system monitoring and portable applications.

Hysteresis is determined using three resistors in a string configuration with the upper and lower tap points connected to the ±INA_U and ±INA_L pins of each comparator, respectively. The state of the outputs of the comparators selects which pin is internally connected to the comparators input. Therefore, a change of state in the comparators output results in one of the inputs being switched in to the comparator and the other being switched out. This provides the user with a fully flexible and accurate method of setting the hysteresis. One input of each comparator is internally connected to the reference. The other input is available externally, via an internal mux, through pins ±INA_U or ±INA_L. The state of the output determines which of these pins is connected at any one time.

The comparator outputs are open-drain with the output stage sinking capability guaranteed greater than 5 mA over temperature. The ADCMP341 has noninverting inputs and the ADCMP343 has inverting inputs. The devices are suitable for portable, commercial, industrial, and automotive applications.

FUNCTIONAL BLOCK DIAGRAMS

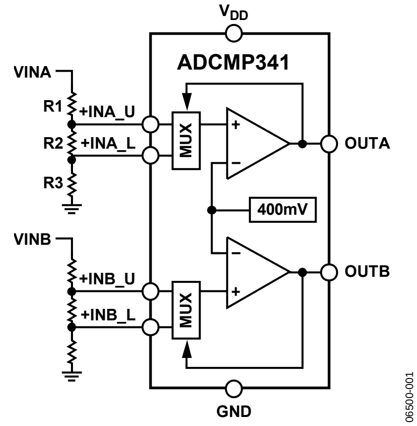

Figure 1. ADCMP341

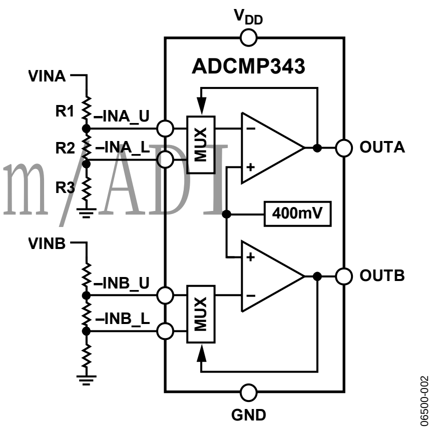

Figure 2. ADCMP343

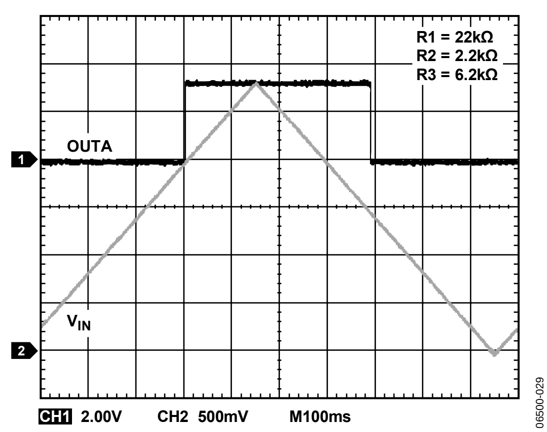

Figure 3. Hysteresis programmed to 513 mV @ V_{IN} on ADCMP341

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

2/07—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 1.7 V to 5.5 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLD[1]					
Threshold Voltage	396.6	400.4	404.3	mV	V_{DD} = 1.7 V, T_A = 25°C
	399.3	400.4	401.5	mV	V_{DD} = 3.3 V, T_A = 25°C
	398.5	400.4	402.2	mV	V_{DD} = 5.5 V, T_A = 25°C
	395.0	400.4	405.8	mV	V_{DD} = 1.7 V, 0°C ≤ T_A ≤ 70°C
	397.4	400.4	403.4	mV	V_{DD} = 3.3 V, 0°C ≤ T_A ≤ 70°C
	396.9	400.4	403.7	mV	V_{DD} = 5.5 V, 0°C ≤ T_A ≤ 70°C
	391.2	400.4	407.7	mV	V_{DD} = 1.7 V, −40°C ≤ T_A ≤ +125°C
	393.4	400.4	405.6	mV	V_{DD} = 3.3 V, −40°C ≤ T_A ≤ +125°C
	393.2	400.4	405.8	mV	V_{DD} = 5.5 V, −40°C ≤ T_A ≤ +125°C
Threshold Voltage Accuracy			±0.275	%	T_A = 25°C, V_{DD} = 3.3 V
Threshold Voltage Temperature Coefficient		16		ppm/°C	
POWER SUPPLY					
Supply Current		6.5	9	μA	V_{DD} = 1.7 V
		7.0	10	μA	V_{DD} = 5.5 V
INPUT CHARACTERISTICS					
Input Bias Current		0.01	5	nA	V_{DD} = 1.7 V, V_{IN} = V_{DD}
		0.01	5	nA	V_{DD} = 1.7 V, V_{IN} = 0.1 V
OPEN-DRAIN OUTPUTS					
Output Low Voltage[2]		140	220	mV	V_{DD} = 1.7 V, I_{OUT} = 3 mA
		140	220	mV	V_{DD} = 5.5 V, I_{OUT} = 5 mA
Output Leakage Current[3]		0.01	1	μA	V_{DD} = 1.7 V, V_{OUT} = V_{DD}
		0.01	1	μA	V_{DD} = 1.7 V, V_{OUT} = 5.5 V
DYNAMIC PERFORMANCE[2, 4]					
High-to-Low Propagation Delay		10		μs	V_{DD} = 5 V, V_{OL} = 400 mV
Low-to-High Propagation Delay		8		μs	V_{DD} = 5 V, V_{OH} = 0.9 × V_{DD}
Output Rise Time		0.5		μs	V_{DD} = 5 V, V_O = (0.1 to 0.9) × V_{DD}
Output Fall Time		0.07		μs	V_{DD} = 5 V, V_O = (0.1 to 0.9) × V_{DD}

[1] R_L = 100 kΩ, V_O = 2 V swing.
[2] 10 mV input overdrive.
[3] V_{IN} = 40 mV overdrive.
[4] R_L = 10 kΩ.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD}	−0.3 V to +6 V
±INA_U, ±INA_L, ±INB_U, ±INB_L	−0.3 V to +6 V
OUTA, OUTB	−0.3 V to +6 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

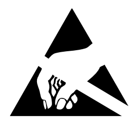
THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOT-23	211.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

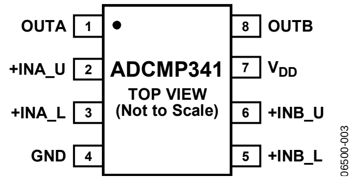


Figure 4. ADCMP341 Pin Configuration

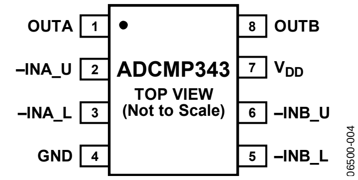


Figure 5. ADCMP343 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUTA	Open-Drain Output for Comparator A.
2	±INA_U	Monitors Analog Input Voltage on Comparator A. Connect to the upper tap point of the resistor string. Connect internally to the noninverting input on the ADCMP341 or the inverting pin on the ADCMP343 via a mux controlled by the output level on Comparator A. The other input of Comparator A is connected to a 400 mV reference.
3	±INA_L	Monitors Analog Input Voltage on Comparator A. Connect to the lower tap point of the resistor string. Connect internally to the noninverting input on the ADCMP341 or the inverting pin on the ADCMP343 via a mux controlled by the output level on Comparator A. The other input of Comparator A is connected to a 400 mV reference.
4	GND	Ground.
5	±INB_L	Monitors Analog Input Voltage on Comparator B. Connect to the lower tap point of the resistor string. Connect internally to the noninverting input on the ADCMP341 or the inverting pin on the ADCMP343 via a mux controlled by the output level on Comparator B. The other input of Comparator B is connected to a 400 mV reference.
6	±INB_U	Monitors Analog Input Voltage on Comparator B. Connect to the upper tap point of the resistor string. Connect internally to the noninverting input on the ADCMP341 or the inverting pin on the ADCMP343 via a mux controlled by the output level on Comparator B. The other input of Comparator B is connected to a 400 mV reference.
7	V_{DD}	Power Supply Pin.
8	OUTB	Open-Drain Output for Comparator B.

TYPICAL PERFORMANCE CHARACTERISTICS

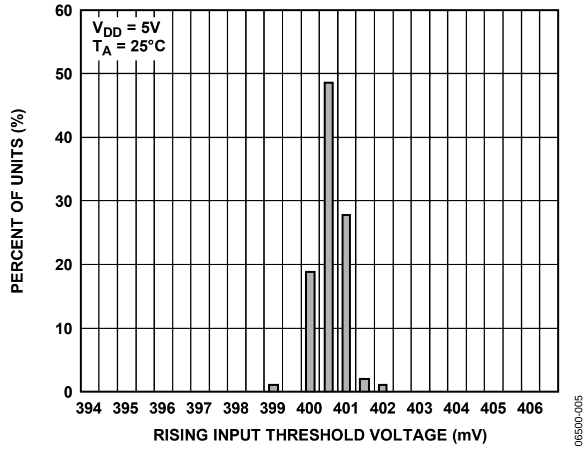


Figure 6. Distribution of Rising Input Threshold Voltage

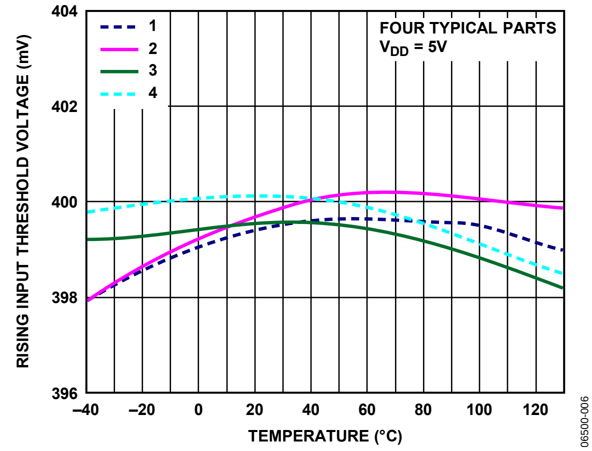


Figure 9. Rising Input Threshold Voltage vs. Temperature

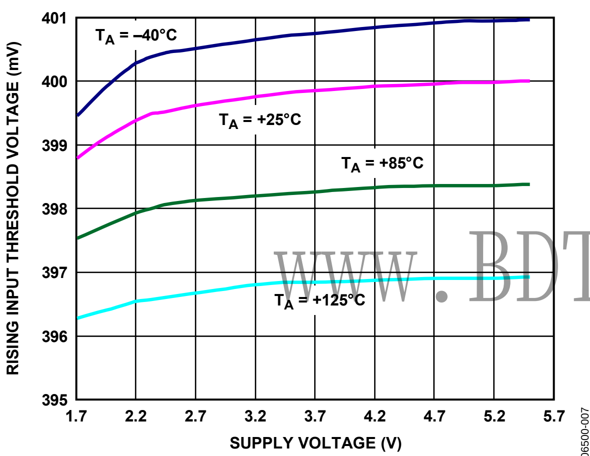


Figure 7. Rising Input Threshold Voltage vs. Supply Voltage

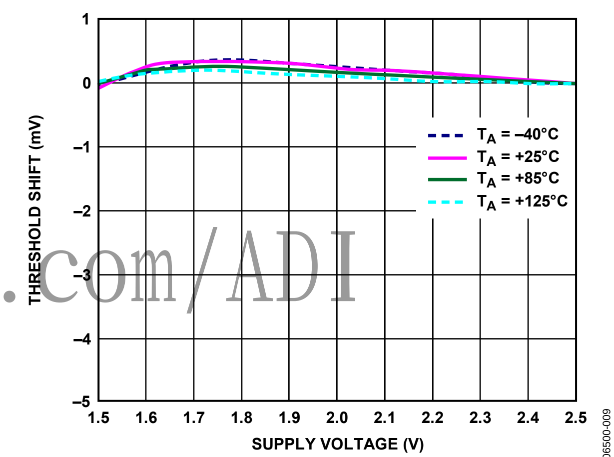


Figure 10. Minimum Supply Voltage

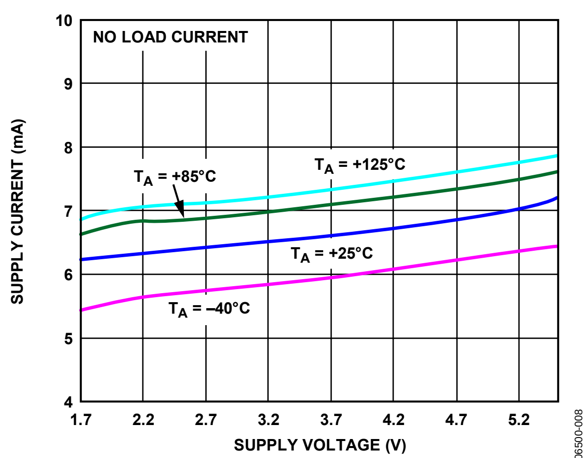


Figure 8. Quiescent Supply Current vs. Supply Voltage

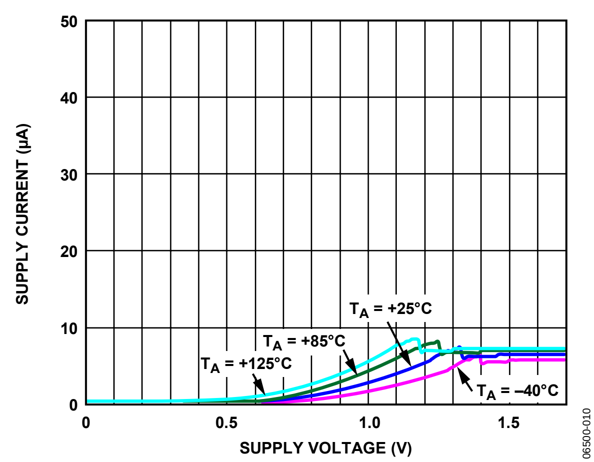


Figure 11. Start-Up Supply Current

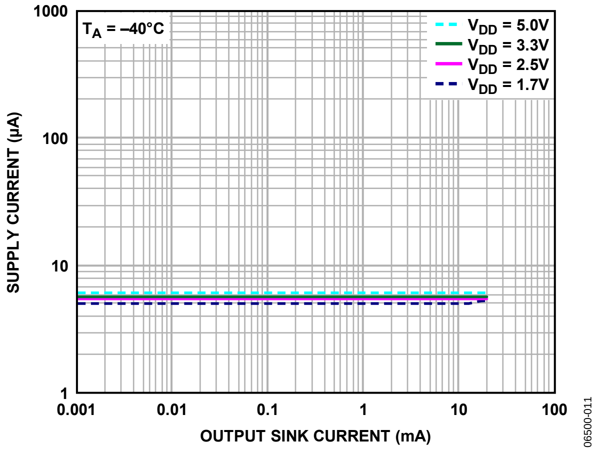


Figure 12. Supply Current vs. Output Sink Current

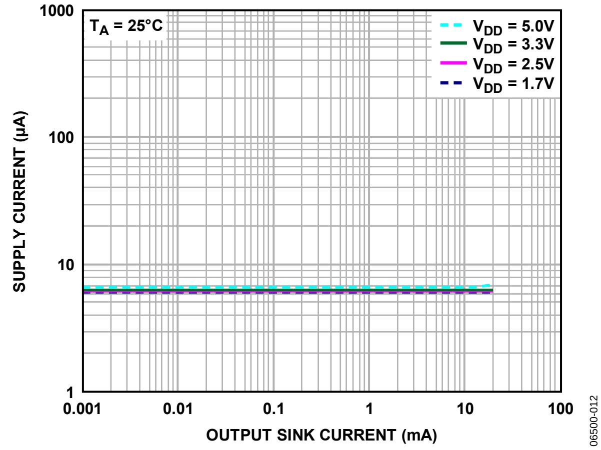


Figure 15. Supply Current vs. Output Sink Current

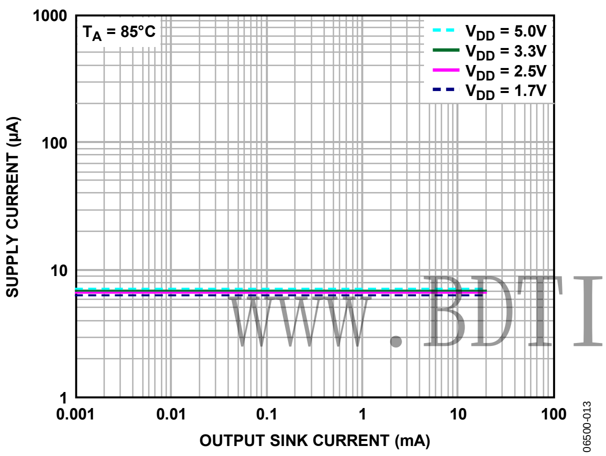


Figure 13. Supply Current vs. Output Sink Current

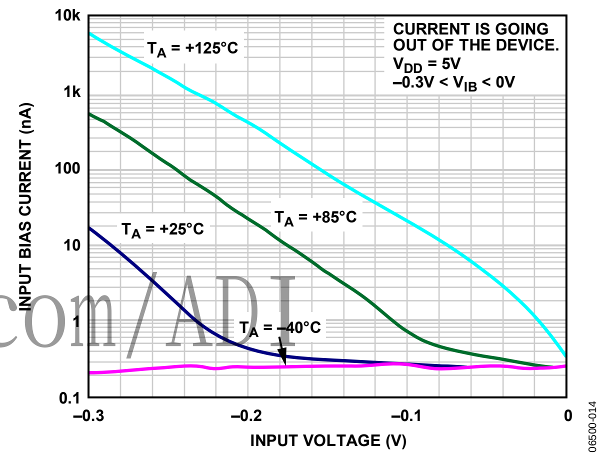


Figure 16. Below Ground Input Bias Current

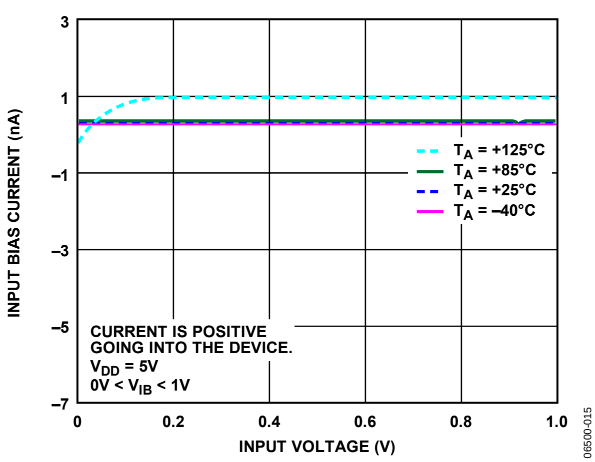


Figure 14. Low Level Input Bias Current

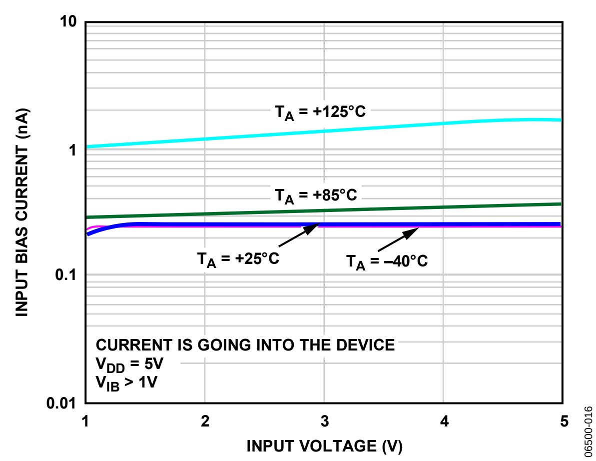


Figure 17. High Level Input Bias Current

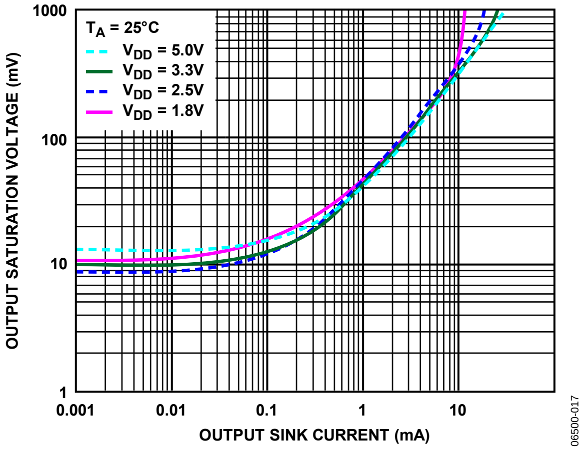


Figure 18. Output Saturation Voltage vs. Output Sink Current

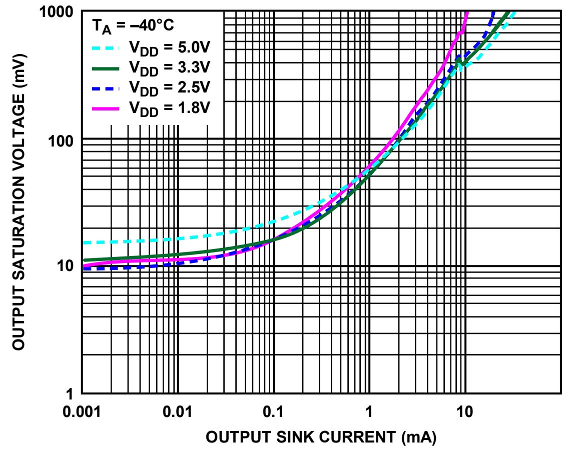


Figure 21. Output Saturation Voltage vs. Output Sink Current

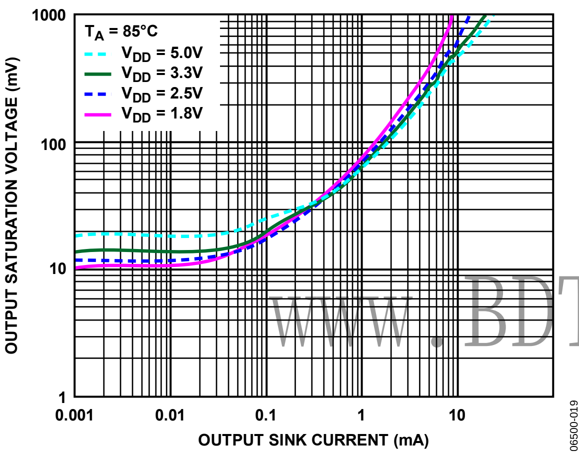


Figure 19. Output Saturation Voltage vs. Output Sink Current

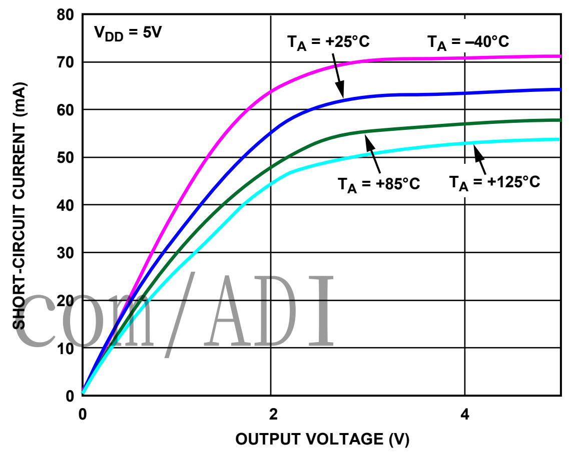


Figure 22. Short-Circuit Current vs. Output Voltage

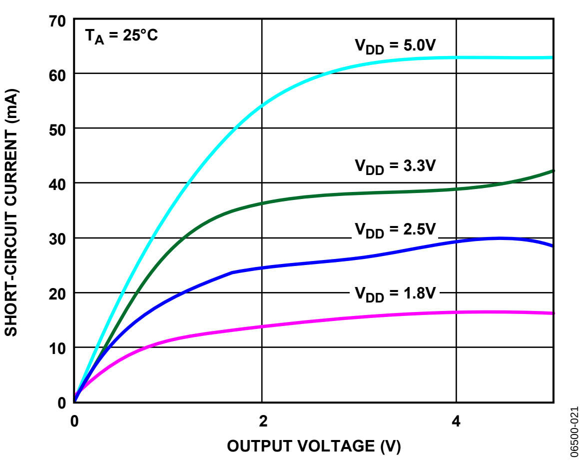


Figure 20. Short-Circuit Current vs. Output Voltage

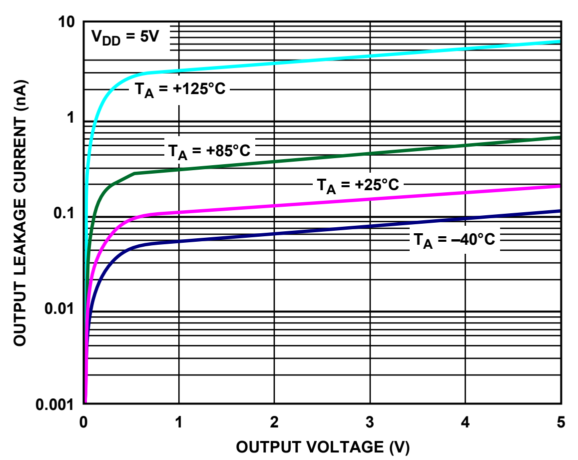


Figure 23. Output Leakage Current vs. Output Voltage

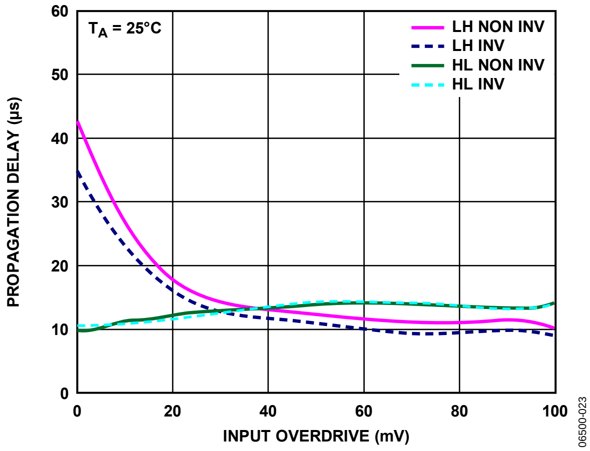


Figure 24. Propagation Delay vs. Input Overdrive

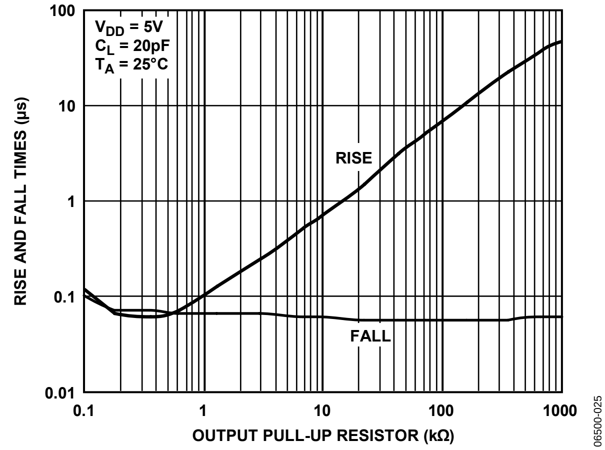


Figure 26. Rise and Fall Times vs. Output Pull-Up Resistor

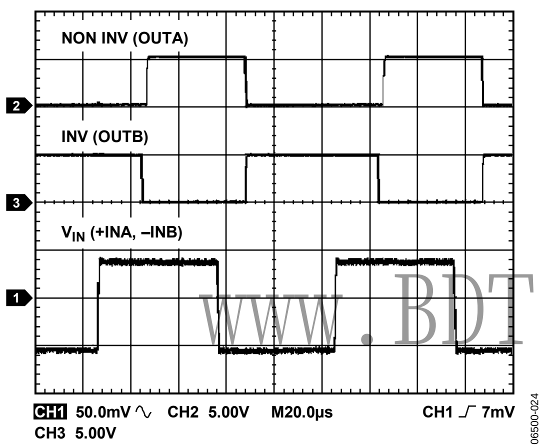


Figure 25. Noninverting and Inverting Comparators Propagation Delay

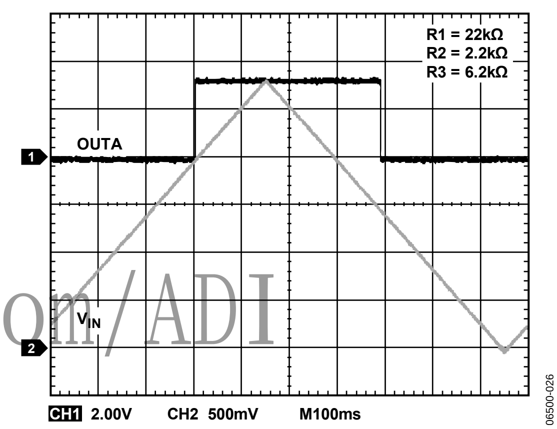


Figure 27. Hysteresis Programmed to ~513 mV at Top of Input String (Hysteresis at ADCMP341 Pins ≈ 104 mV)

APPLICATION INFORMATION

The ADCMP341/ADCMP343 are dual, low power comparators with a built-in 400 mV reference that operates from 1.7 V to 5.5 V. The comparators are 0.275% accurate with fully programmable hysteresis, implemented using a new technique of a three-resistor string on the input. These open-drain outputs are capable of sinking up to 40 mA.

COMPARATORS AND INTERNAL REFERENCE

Each of the comparators has one input available externally; the other comparator inputs are connected internally to the 400 mV reference. The ADCMP341 has two noninverting comparators and the ADCMP343 has two inverting comparators.

There are two input pins available to each comparator. However, these two input pins (±INx_U, ±INx_L) connect to the same input leg of the comparator via a muxing system. This is to provide fully programmable rising and falling trip points. The output of the comparator determines which pin is connected to the input of the same comparator. Using Figure 28 as an example, when OUTA is high, +INA_U is connected to the comparator input. When the input voltage drops and passes below the 400 mV reference, the output goes low. This in turn disconnects +INA_U from the comparator and connects +INA_L. This leg of the string is at a lower voltage and thus instantaneously the effect of hysteresis is applied. Therefore, using a resistor string on the input as shown in Figure 28, the voltages for the rising and falling trip points can be programmed by selecting the appropriate resistors in the string.

POWER SUPPLY

The ADCMP341/ADCMP343 are designed to operate from 1.7 V to 5.5 V. A 0.1 μF decoupling capacitor is recommended between V_{DD} and GND.

INPUTS

The comparator inputs are limited to the maximum V_{DD} voltage range. The voltage on these inputs can be above V_{DD} but never above the maximum allowed V_{DD} voltage.

OUTPUTS

The open-drain comparator outputs are limited to the maximum specified V_{DD} voltage range, regardless of the V_{DD} voltage. These outputs are capable of sinking up to 40 mA. Outputs can be tied together to provide a common output signal.

PROGRAMMING HYSTERESIS

When choosing the resistor values, the input bias current must be considered as a potential source of error. Begin by choosing a resistor value for R3, which takes into account the acceptable error introduced by the maximum specified input bias current. To reduce this error, the current flowing through the Resistor R3 should be considerably greater than the input bias current.

$$I_{R3} >> I_{BIAS}$$

R3 is therefore

$$R3 = \frac{V_{REF}}{I_{R3}}$$

Now R2 can be calculated from the following:

$$R2 = \frac{R_3\left(V_{RISING} - V_{FALLING}\right)}{V_{FALLING}}$$

R1 can then be calculated using the following equation:

$$R1 = \left(R3 \times \left(\frac{V_{RISING}}{V_{REF}} - 1\right)\right) - R2$$

where:

V_{REF} is the specified on chip reference.
I_{BIAS} is the maximum specified input bias current.
R1, *R2,* and *R3* are the three resistors as shown in Figure 28.
I_{R3} is the current flowing through *R3*.
$V_{FALLING}$ is the desired falling trip voltage and lower of the two.
V_{RISING} is the desired rising trip voltage and higher of the two.

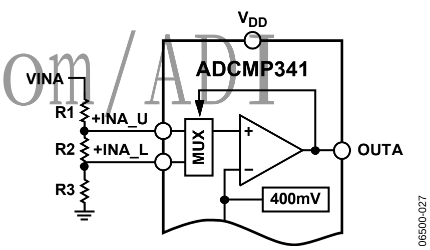


Figure 28. Programming Hysteresis Example

LAYOUT RECOMMENDATIONS

Correct layout is very important to increase noise immunity. Long tracks from the input resistors to the device can lead to noise being coupled onto the inputs. To avoid this, it is best to place the input resistors as close as possible to the device. It is also recommended that a GND plane is used under this layout. The combination of small hysteresis and the use of a large R3 resistor further increases susceptibility to noise. In this case, a decoupling capacitor (CA, CB) may be required on the ±INx_U node to help reduce any noise. A recommended layout example can be seen in Figure 29.

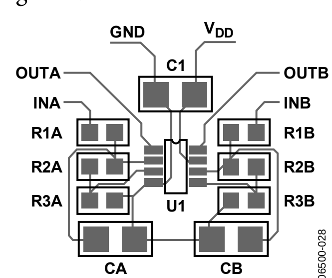


Figure 29. Recommended Layout Example

OUTLINE DIMENSIONS

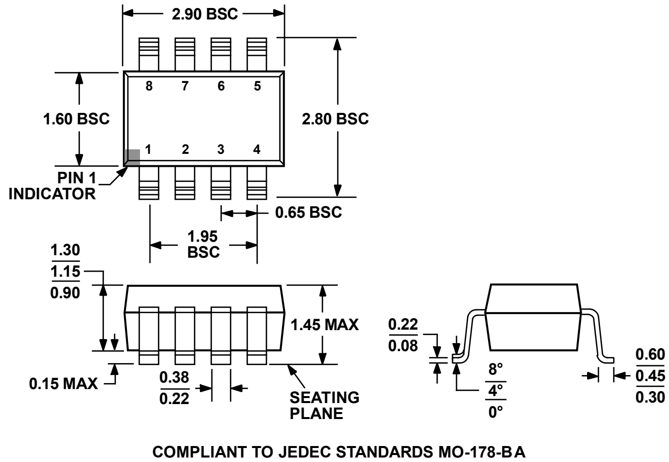


Figure 30. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADCMP341YRJZ-REEL7[1]	–40°C to +125°C	8-Lead SOT-23	RJ-8	M8Y
ADCMP343YRJZ-REEL7[1]	–40°C to +125°C	8-Lead SOT-23	RJ-8	M91

[1] Z = Pb-free part.

NOTES