Multiservice Clock Generator

Preliminary Technical Data

AD9551

FEATURES

Translation between any two standard network rates
Dual reference inputs and dual clock outputs
Pin programmable for standard network rate translation
SPI programmable for arbitrary rational rate translation
Output frequencies from 10 MHz to 777.6 MHz
Input frequencies from 19.44 MHz to 806 MHz
On-chip VCO
Jitter: <0.5 ps rms (12kHz to 20 MHz)
Supports standard forward error correction (FEC) rates
Supports holdover operation
Supports hitless switchover and phase build out (even with unequal reference frequencies)
SPI compatible 3 wire programming interface
Single Supply (3.3V)

APPLICATIONS

Multi-service switches
Multi-service routers
Exact network clock frequency translation
General purpose frequency translation

OVERVIEW

The AD9551 accepts one or two reference input signals from which it generates one or two output signals. The frequencies of the two output signals are harmonically related by a programmable factor from 1 to 63. The AD9551 precisely translates the reference frequency to the desired output frequency. The input receivers and output drivers provide both single-ended and differential operation.

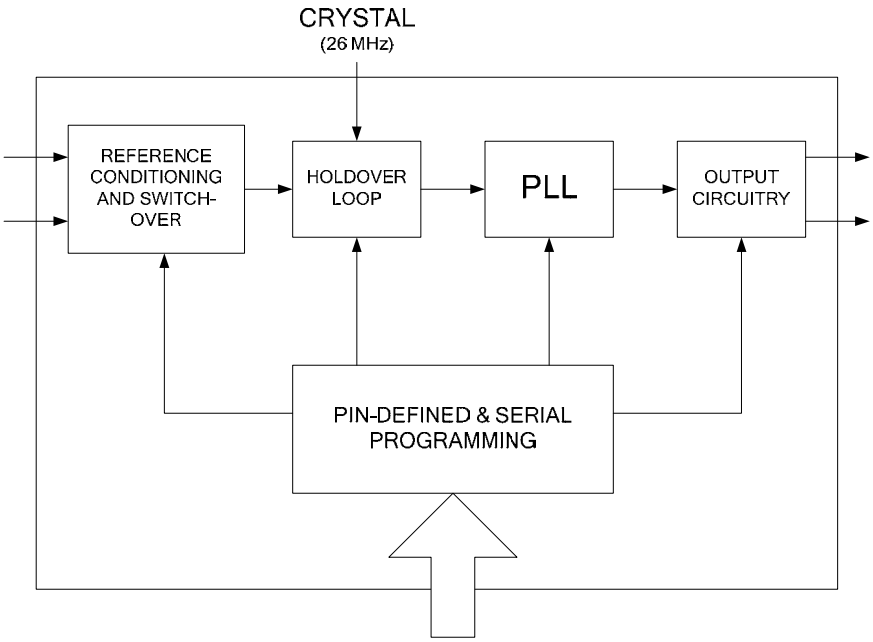
Reference conditioning and switchover circuitry internally synchronizes the two references so that if one reference fails, there is virtually no phase perturbation at the output.

The AD9551 uses an external 26 MHz crystal (nominal) and internal DCXO to provide for holdover operation. Should both references fail, the device maintains a steady output signal.

A fractional N PLL enables ultra fine precision in tuning the output frequency. All currently defined network standards (including FEC ratios) are possible (assuming the use of a 26 MHz crystal).

The AD9551 provides pin selectable preset divider values offering an assortment of frequency ratios. A SPI interface provides further flexibility by offering the ability to program most any desired frequency ratio

BASIC BLOCK DIAGRAM



Rev. PrJ

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REVISION HISTORY

9/08 Rev. PrJ: First preliminary publication version.

SPECIFICATIONS

REFERENCE CLOCK INPUT CHARACTERISTICS

Table 1:

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
Frequency Range					
Normal input mode	77.76		806	MHz	Minimum based on a 19.44 MHz crystal with the input divider in divide-by-4 integer mode
19.44 MHz input mode		19.44		MHz	With a 19.44 MHz crystal
Input Capacitance		3		pF	
Input Impedance		4800		Ω	
Duty Cycle	40		60	%	
Refclk Input Power	-15		+3	dBm	50Ω external termination
Refclk Input Voltage Swing (Differential)	250		TBD	mV pk-pk	
Refclk Input Voltage Swing (Single-Ended)	250		TBD	mV pk-pk	

OUTPUT CHARACTERISTICS

Table 2:

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL Mode					Output driver static
Differential Output Voltage Swing	TBD	1700	TBD	mV	
Common-Mode Output Voltage	TBD	AVDD3-1.3	TBD	V	
LVDS Mode					
Differential Output Voltage Swing					
Common-Mode Output Voltage					
Short Circuit Output Current			TBD	mA	
CMOS Mode					Output driver static; standard drive strength setting
Output Voltage High (V_{OH})					
I_{OH} = 10 mA	TBD			V	
I_{OH} = 1 mA	TBD				
Output Voltage Low (V_{OL})					
I_{OL} = 10 mA			TBD	V	
I_{OL} = 1 mA			TBD		
OUTPUT FREQUENCY RANGE					
LVPECL	0		900	MHz	
LVDS	0		900	MHz	
CMOS (3.3V)					
Standard drive strength setting	0		200	MHz	
Low drive strength setting	0		TBD	MHz	
RISE/FALL TIME (20%-80%)					
LVPECL		115	TBD	ps	100 Ω termination across output pair
LVDS		115	TBD	ps	100 Ω termination across output pair
CMOS (3.3V)					
Standard drive strength setting		3	4.6	ns	With 10 pF load
Low drive strength setting		TBD	4.6	ns	With 10 pF load
DUTY CYCLE	45		55	%	Applies to all logic families and at their maximum output frequencies

JITTER CHARACTERISTICS (xxx Hz Loop Bandwidth)

Table 3:

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
Jitter Generation					
Bandwidth: 12 kHz – 20 MHz				ps rms	
Bandwidth: 50 kHz – 80 MHz				ps rms	
Jitter Transfer Bandwidth				Hz	See Typical Performance Characteristics section
Jitter Transfer Peaking				dB	See Typical Performance Characteristics section
Jitter Tolerance					See Typical Performance Characteristics section

CRYSTAL OSCILLATOR CHARACTERISTICS

Table 4:

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
Frequency Range	19.44	26	30.72	MHz	Assumes nominal 10pF shunt capacitance on each input pin
Input Capacitance		3-21		pF	Variable via automatic or program control (see the Input PLL section)

NOTE: Proper device operation requires the use of a crystal with a frequency tolerance of 20 ppm or better.

POWER CONSUMPTION

Table 5:

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
Total Current		140		mA	At maximum output frequency with both output channels active
VDD (pin 9)		TBD		mA	
VDD (pin 23)		TBD		mA	
VDD (pin 27)		TBD		mA	
VDD (pin 34)		TBD		mA	
Output Driver (LVPECL)		TBD		mA	100 Ω termination across output pair

LOGIC INPUT PINS

Table 6:

NOTE: The A(3:0), B(3:0), Y(3:0) and OUTSEL pins have 100 kΩ internal pull-up resistors.

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
INPUT CHARACTERISTICS					
Logic 1 Voltage, V_{IH}	1.2			V	For the CMOS inputs, a static logic 1 results from either a pull up resistor or no connection.
Logic 0 Voltage, V_{IL}			0.8	V	
Logic 1 Current, I_{IH}			3	µA	
Logic 0 Current, I_{IL}			30	µA	

RESET PIN

Table 7:

NOTE: The RESET pin has a 100 kΩ internal pull-up resistor, so the default state of the device is reset.

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
INPUT CHARACTERISTICS					
Input High Voltage (V_{IH})	2.0			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current High (I_{INH})		TBD	TBD	µA	
Input Current Low (I_{INL})		TBD	TBD		
MINIMUM PULSE WIDTH HIGH	TBD			ns	

LOGIC OUTPUT PINS

Table 8:

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
Output Voltage High, V_{OH}	2.7			V	
Output Voltage Low, V_{OL}			0.4	V	

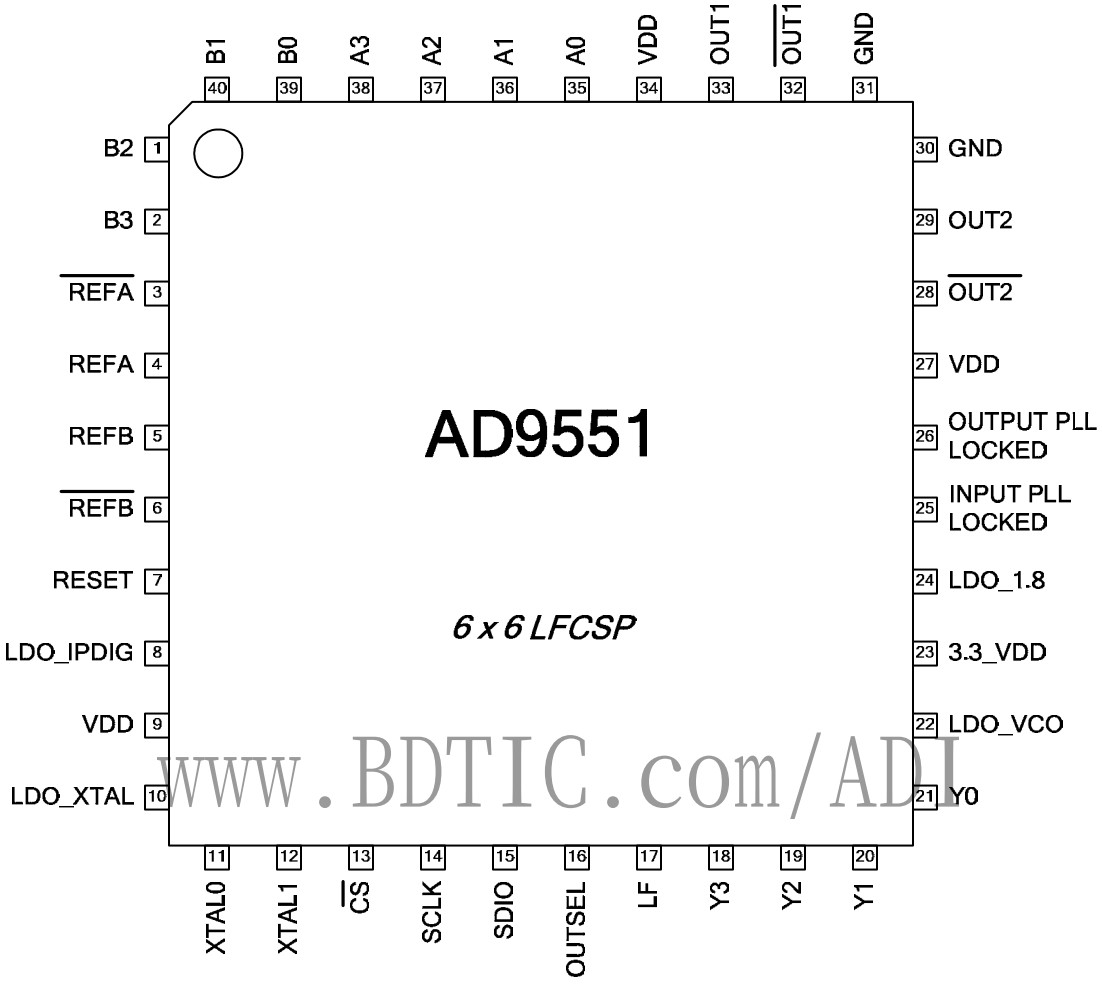
SERIAL CONTROL PORT

Table 9:

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$					Internal 30 kΩ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			3	µA	
Input Logic 0 Current		110		µA	
Input Capacitance		2		pF	
SCLK					Internal 30 kΩ pull-down resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		µA	
Input Logic 0 Current			1	µA	
Input Capacitance		2		pF	
SDIO					
As an input					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		2		pF	
As an output					
Output Logic 1 Voltage	2.7			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
SDO					
Output Logic 1 Voltage	2.7			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
TIMING					
SCLK					
Clock Rate, $1/t_{CLK}$			25	MHz	
Pulse Width High, t_{HI}	16			ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse Width Low, t_{LO}	16			ns	
SDIO to SCLK Setup, t_{DS}	4			ns	
SCLK to SDIO Hold, t_{DH}	1.1			ns	
SCLK to Valid SDIO and SDO, t_{DV}			1	ns	
$\overline{CS}$ to SCLK Setup (t_S) and Hold (t_C)	2			ns	
$\overline{CS}$ Minimum Pulse Width High	3			ns	

PIN DIAGRAM



PIN DESCRIPTION & NOMENCLATURE

Table 10: Pin Descriptions

Pin #	Mnemonic	I/O	Description
9, 23, 27, 34	VDD	P	Power Supply Connection: 3.3V Analog Supply.
30	GND	P	Analog Ground.
31	GND	P	Analog Ground.
4	REFA	I	Analog input(active high): Reference clock input A.
3	$\overline{\text{REFA}}$	I	Analog input(active high): Complementary reference clock input A.
5	REFB	I	Analog input(active high): Reference clock input B.
6	$\overline{\text{REFB}}$	I	Analog input(active high): Complementary reference clock input B.
13	$\overline{\text{CS}}$	I	Digital input (active low) Chip Select.
14	SCLK	I	Serial data clock.
15	SDIO	I/O	Digital serial data input/output.
7	RESET	I	Digital input (active high). Resets internal logic to default states. This pin has an internal 100 KΩ pull-down resistor, so the default state of the device is reset.
11	XTL0	I	Pin for connecting an external crystal (20-30 MHz).
12	XTL1	I	Pin for connecting an external crystal (20-30 MHz).
33	OUT1	O	Square wave clocking output #1
32	$\overline{\text{OUT1}}$	O	Complementary square wave clocking output #1
29	OUT2	O	Square wave clocking output #2
28	$\overline{\text{OUT2}}$	O	Complementary square wave clocking output #2
17	LF	I/O	Loop filter node for the output PLL. Connect an external 12 nF capacitor between this pin and ground.
26	OUTPUT PLL LOCKED	O	An active high "locked" status indicator for the output PLL
25	INPUT PLL LOCKED	O	An active high "locked" status indicator for the input PLL
16	OUTSEL	I	A logic 0 selects LVDS and a logic 1 selects LVPECL compatible levels for both OUT1 and OUT2 when the outputs are not under SPI port control (may be overridden via the programming registers).
8, 10, 22, 24	LDO_IPDIG, DO_XTAL, LDO_VCO, LDO_1.8	P/O	LDO decoupling pins. Connect a 0.47µF decoupling capacitor from each of these pins to ground.
35	A0	I	Control pins to select preset values for the REFA dividers.
36	A1	I	
37	A2	I	
38	A3	I	
39	B0	I	Control pins to select preset values for the REFB dividers.
40	B1	I	
1	B2	I	
2	B3	I	
21	Y0	I	Control pins to select preset values for the output PLL feedback dividers and OUT1 dividers.
20	Y1	I	
19	Y2	I	
18	Y3	I	

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1: Phase Noise

Figure 4: Output Waveforms

Figure 2: Jitter Transfer

Figure 5: Supply Current vs. Output Frequency

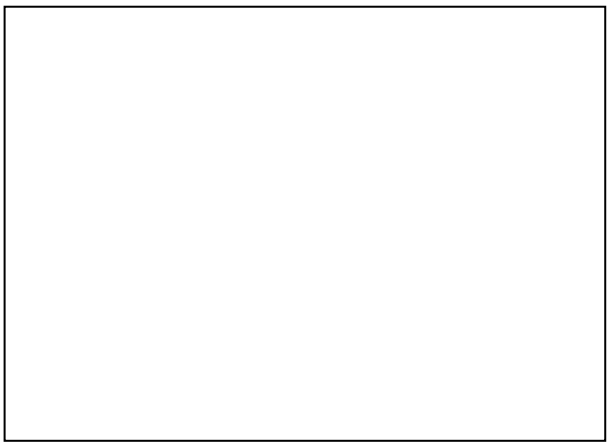


Figure 3: Jitter Tolerance

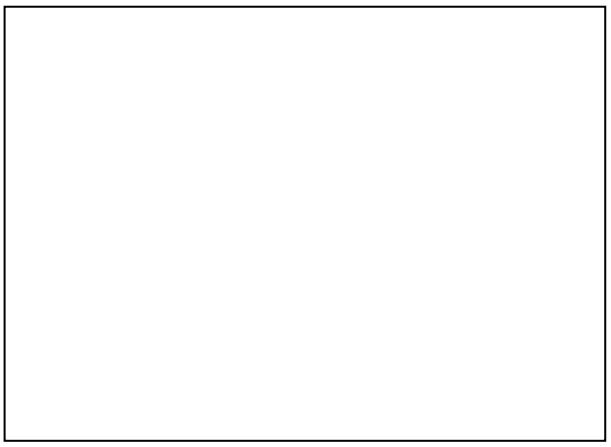


Figure 6: Duty Cycle vs. Output Frequency

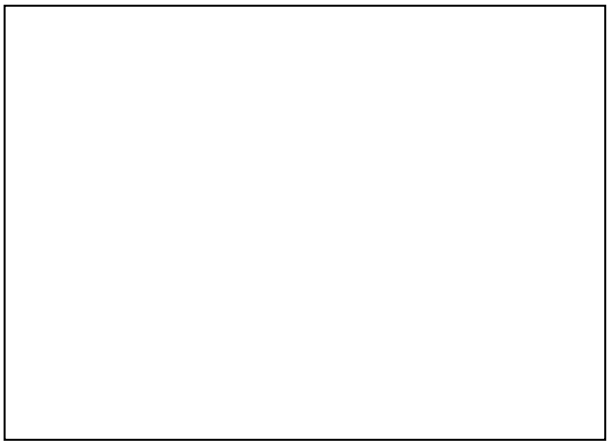


Figure 7: Peak-to-Peak Output Voltage vs. Frequency

Figure 8: Power Consumption

GENERAL DESCRIPTION

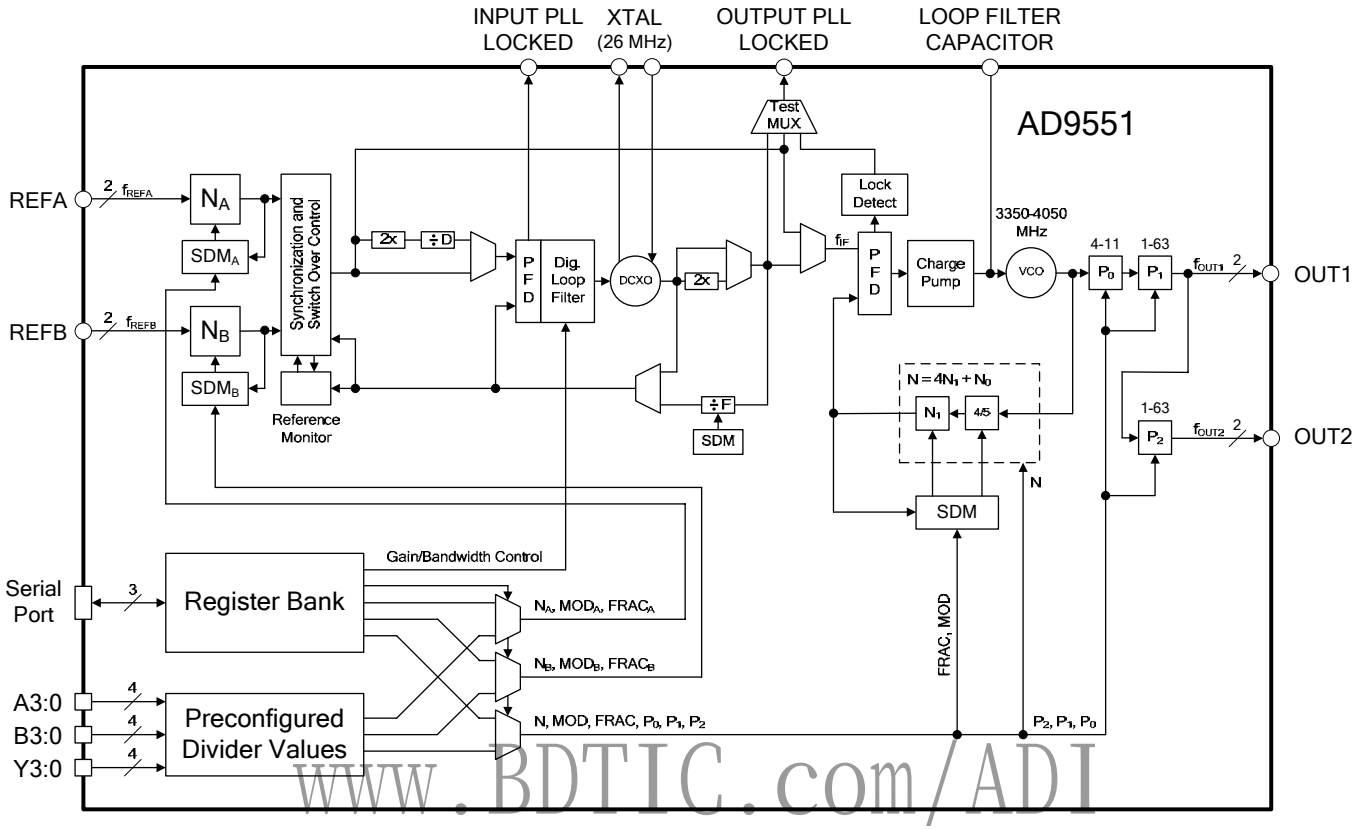


Figure 9: AD9551 Detailed Block Diagram

The AD9551 is a clock generator that employs fractional-N based phase locked loops (PLL) using sigma-delta modulators (SDMs). The fractional frequency synthesis capability enables the device to meet the frequency and feature requirements for Multiservice switch applications. The AD9551 precisely generates a wide range of standard frequencies when using any one of those same frequencies as a timing base (reference). The primary challenge of this function is the precise generation of the desired output frequency; any inaccuracy in the output frequency will result in system failure as the frequency error eventually results in cycle slippage. This fact necessitates the use of a fractional-N based PLL architecture with variable modulus.

The device architecture consists of two cascaded PLL stages. The first stage consists of fractional division (via SDM) followed by a digital PLL that uses a crystal resonator based DCXO. The DCXO operates in a narrow band within a 20-30 MHz operating range (established by the crystal). This PLL has a loop bandwidth of only a few hertz providing initial jitter cleanup of the input reference signal. The second stage is a frequency multiplying PLL that translates the first stage output frequency (20-30 MHz) up to ~3.7 GHz. This PLL incorporates an SDM-based fractional feedback divider that enables fractional frequency multiplication. Programmable integer dividers follow this second PLL establishing a final output frequency of 806 MHz, or less. It is important to understand that this architecture produces an output frequency that is most likely not coherent with the input reference frequency. As a result, there is generally no relationship between the phase of the input and output signals.

The AD9551 includes reference signal processing blocks that enable a smooth switching transition between two reference inputs. This circuitry automatically detects the presence of the reference input signals. If only one input is present, the device uses it as the active reference. If both are present, one becomes the active reference and the other the alternate reference. The circuitry edge-aligns the backup reference with the active reference. If the active reference fails, the circuitry automatically switches to the backup reference (if available) making it the new active reference. Meanwhile, if the failed reference is once again available, it becomes the new backup reference and is edge-aligned with the new active reference (a precaution against failure of the new active reference). In the event that neither reference is useable, the AD9551 supports a holdover mode. The user must provide a 20-30 MHz external crystal to utilize the switchover and holdover functionality, as well as to serve as the clock source for the reference synchronization and monitoring functions.

The AD9551 is easily configured via external control pins (A3:0, B3:0 and Y3:0). The logic state of these pins sets predefined divider values that establish a specific input to output frequency ratio. In addition, any of the divider settings are programmable via the serial programming port, enabling a wide range of input/output frequency ratios under program control.

The AD9551 relies on a single external capacitor for the output PLL loop filter. With proper termination, the output is compatible with LVPECL, LVDS, or CMOS logic levels, though the AD9551 is implemented in a strictly CMOS process.

The AD9551 operates over the extended industrial temperature range of -40°C to +85°C.

PRESET FREQUENCY RATIOS

The frequency selection pins (A3:0, B3:0 and Y3:0) allow the user to hardwire the device for preset input and output divider values based on the pin logic states. The A3:0 pins control the REFA dividers, the B3:0 pins the REFB dividers, and the Y3:0 pins the feedback and output dividers. The pins decode ground or open connections as logic 0 or 1, respectively. To override the preset divider settings use the serial I/O port to program the desired divider values.

Table 11 lists the input divider values based on the logic state of the frequency selection pins. The table headings are:

- A3:0,B3:0: The logic state of the A3:0 or B3:0 pins.
- $N_{A,B}$: The integer part of the REFA input divider (N_A) or the REFB input divider (N_B).
- $MOD_{A,B}$: The modulus of the REFA input divider SDM (MOD_A) or the REFB input divider SDM (MOD_B).
- $FRAC_{A,B}$: The fractional part of the REFA input divider SDM ($FRAC_A$) or the REFB input divider SDM ($FRAC_B$).
- $fREF_{A,B}$: The frequency of the REFA input ($fREF_A$) or the REFB input ($fREF_B$).

The divider settings shown in Table 11 cause the frequency at the reference input of the output PLL's PFD (f_{IF}) to operate at exactly 26 MHz when using the indicated input reference frequency, $fREF_A$ or $fREF_B$ (assumes the use of a 26 MHz external crystal).

Table 11: Preset Input Settings

A3:0 B3:0	$N_{A,B}$	$MOD_{A,B}$	$FRAC_{A,B}$	$fREF_{A,B}$ (MHz)
0000	23	130,000	110,800	622.08
0001	24	130,000	-120,000	625
0010	24	154,050	-114,594	$622.08\left(\frac{239}{237}\right) \approx 627.33$
0011	24	130,000	45,200	$622.08\left(\frac{66}{64}\right) \equiv 641.52$
0100	24	166,400	96,400	$625\left(\frac{66}{64}\right) \equiv 644.53125$
0101	25	104,000	-44,625	$\frac{10518.75}{16} \equiv 657.421875$
0110	25	198,016	-42,891	$\frac{10518.75}{16}\left(\frac{239}{238}\right) \approx 660.18$
0111	25	154,700	41,820	$622.08\left(\frac{255}{238}\right) \approx 666.51$
1000	25	154,050	74,970	$622.08\left(\frac{255}{237}\right) \approx 669.33$
1001	25	182,000	93,000	$625\left(\frac{15}{14}\right) \approx 669.64$
1010	25	153,400	108,120	$622.08\left(\frac{255}{236}\right) \approx 672.16$
1011	26	197,184	67,998	$625\left(\frac{255}{237}\right)\left(\frac{66}{64}\right) \approx 693.48$
1100	26	146,900	83,612	$622.08\left(\frac{253}{226}\right) \approx 696.40$
1101	27	198,016	-161,755	$\frac{10518.75}{16}\left(\frac{255}{238}\right) \approx 704.38$
1110	27	197,184	-115,995	$\frac{10518.75}{16}\left(\frac{255}{237}\right) \approx 707.35$
1111	19.44 MHz input mode			

Pins Y3:0 select the divider values for the feedback path of the output PLL as well as for the OUT1 dividers (P_0 and P_1). The OUT2 divider, P_2, defaults to unity unless otherwise programmed via the serial port. Table 12 and Table 13 list the feedback and output divider values based on the logic state of the Y3:0 frequency selection pins. Table 12 gives the divider values for the normal input mode and Table 13 for the 19.44 MHz input mode. The headings for both tables are as follows:

- Y3:0: The logic state of the Y3:0 pins.
- N: The integer part of the feedback divider.
- MOD: The modulus of the feedback SDM.
- FRAC: The fractional part of the feedback SDM.
- P_0/P_1: The P_0 and P_1 divider values.
- f_{OUT1}: The frequency of the OUT1 output.

The divider settings shown in Table 12 produce the indicated frequency at OUT1 given that the frequency at the reference input of the output PLL's PFD (f_{IF}) is exactly 26 MHz.

Table 12: Preset Output Settings, Normal Input Mode

Y3:0	N	MOD	FRAC	P_0/P_1	f_{OUT1} (MHz)
0000	143	520,000	289,600	6/1	622.08
0001	144	520,000	120,000	6/1	625
0010	144	308,100	236,736	6/1	$622.08\left(\frac{239}{237}\right) \approx 627.33$
0011	148	520,000	22,400	6/1	$622.08\left(\frac{66}{64}\right) \equiv 641.52$
0100	148	465,920	343,840	6/1	$625\left(\frac{66}{64}\right) \equiv 644.53125$
0101	151	520,000	370,625	6/1	$\frac{10518.75}{16} \equiv 657.421875$
0110	152	465,920	163,160	6/1	$\frac{10518.75}{16}\left(\frac{239}{238}\right) \approx 660.18$
0111	153	465,920	377,856	6/1	$622.08\left(\frac{255}{238}\right) \approx 666.51$
1000	154	328,640	151,168	6/1	$622.08\left(\frac{255}{237}\right) \approx 669.33$
1001	154	460,096	245,216	6/1	$625\left(\frac{15}{14}\right) \approx 669.64$
1010	155	490,880	56,192	6/1	$622.08\left(\frac{255}{236}\right) \approx 672.16$
1011	133	328,640	119,005	5/1	$625\left(\frac{255}{237}\right)\left(\frac{66}{64}\right) \approx 693.48$
1100	133	470,080	433,856	5/1	$622.08\left(\frac{253}{226}\right) \approx 696.40$
1101	135	349,440	159,975	5/1	$\frac{10518.75}{16}\left(\frac{255}{238}\right) \approx 704.38$
1110	136	394,368	11,577	5/1	$\frac{10518.75}{16}\left(\frac{255}{237}\right) \approx 707.35$
1111	149	520,000	280,000	5/1	$622.08\left(\frac{10}{8}\right) \equiv 777.6$

The divider settings shown in Table 13 produce the indicated frequency at OUT1 when using a 19.44 MHz external crystal.

Table 13: Preset Output Settings, 19.44 MHz Input Mode

Y3:0	N	MOD	FRAC	P_0/P_1	f_{OUT1} (MHz)
0000	96	777,600	0	6/1	622.08
0001	96	777,600	350,400	6/1	625
0010	96	460,728	373,248	6/1	$622.08\left(\frac{239}{237}\right) \approx 627.33$
0011	99	777,600	0	6/1	$622.08\left(\frac{66}{64}\right) \equiv 641.52$
0100	99	777,600	361,350	6/1	$625\left(\frac{66}{64}\right) \equiv 644.53125$
0101	101	777,600	353,025	6/1	$\frac{10518.75}{16} \equiv 657.421875$
0110	101	870,912	766,638	6/1	$\frac{10518.75}{16}\left(\frac{239}{238}\right) \approx 660.18$
0111	102	465,920	399,360	6/1	$622.08\left(\frac{255}{238}\right) \approx 666.51$
1000	103	328,640	95,680	6/1	$622.08\left(\frac{255}{237}\right) \approx 669.33$
1001	103	435,456	148,032	6/1	$625\left(\frac{15}{14}\right) \approx 669.64$
1010	103	917,568	668,736	6/1	$622.08\left(\frac{255}{236}\right) \approx 672.16$
1011	89	819,072	149,467	5/1	$625\left(\frac{255}{237}\right)\left(\frac{66}{64}\right) \approx 693.48$
1100	89	878,688	489,888	5/1	$622.08\left(\frac{253}{226}\right) \approx 696.40$
1101	90	322,560	188,350	5/1	$\frac{10518.75}{16}\left(\frac{255}{238}\right) \approx 704.38$
1110	90	546,048	527,535	5/1	$\frac{10518.75}{16}\left(\frac{255}{237}\right) \approx 707.35$
1111	100	777,600	0	5/1	$622.08\left(\frac{10}{8}\right) \equiv 777.6$

THEORY OF OPERATION

COMPONENT BLOCKS

Input Dividers

Each reference input feeds a dedicated reference divider block. The input dividers provide division of the reference frequency in integer steps from 1 to 63. They provide the bulk of the frequency prescaling necessary to reduce the reference frequency to accommodate the bandwidth limitations of both the input and output PLLs.

Input Sigma-Delta Modulators

Each of the two input dividers is coupled with an optional 2nd order sigma-delta modulator (SDM) enabling fractional division of the input reference frequency. With both integer and fractional divide capability, the AD9551 can accept two different reference frequencies that span a wide range of possible input frequency ratios.

A typical SDM offers fractional division of the form, N+F/M, where N is the integer part, M is the modulus, and F is the fractional part (F<M). All three parameters are positive integers. The input SDMs are atypical in that they implement fractional division in the form, N + ½ + F/(2M) with F being a signed integer and |F|<M.

NOTE: When the SDM is in use, the minimum integer divide value is 4.

Both SDMs have an integrated pseudorandom binary sequence (PRBS) generator. The PRBS generator serves to suppress spurious artifacts by adding a random component to the SDM output. By default, the PRBS is active in both input SDMS, but the user has the option to disable the PRBSs via Register 1E<2>.

Reference Monitor

The reference monitor verifies the presence/absence of the prescaled REFA and REFB signals (i.e. after division by the input dividers). The status of the reference monitor guides the activity of the synchronization and switchover control logic.

NOTE: The DCXO must be operational in order for the reference monitor to function.

Synchronization/Switchover Control

Reference synchronization occurs after the input reference dividers as shown in Figure 10, which is a block diagram of the hitless reference switchover circuit. The synchronization and switchover functionality relies on the reference monitor logic to control the operation of three delay locked loops (DLLs). The delay block of the three DLLs are identical, so that they exhibit the same time delay for a given delay value setting.

NOTE: The DCXO must be operational in order for the synchronization and switchover control to operate.

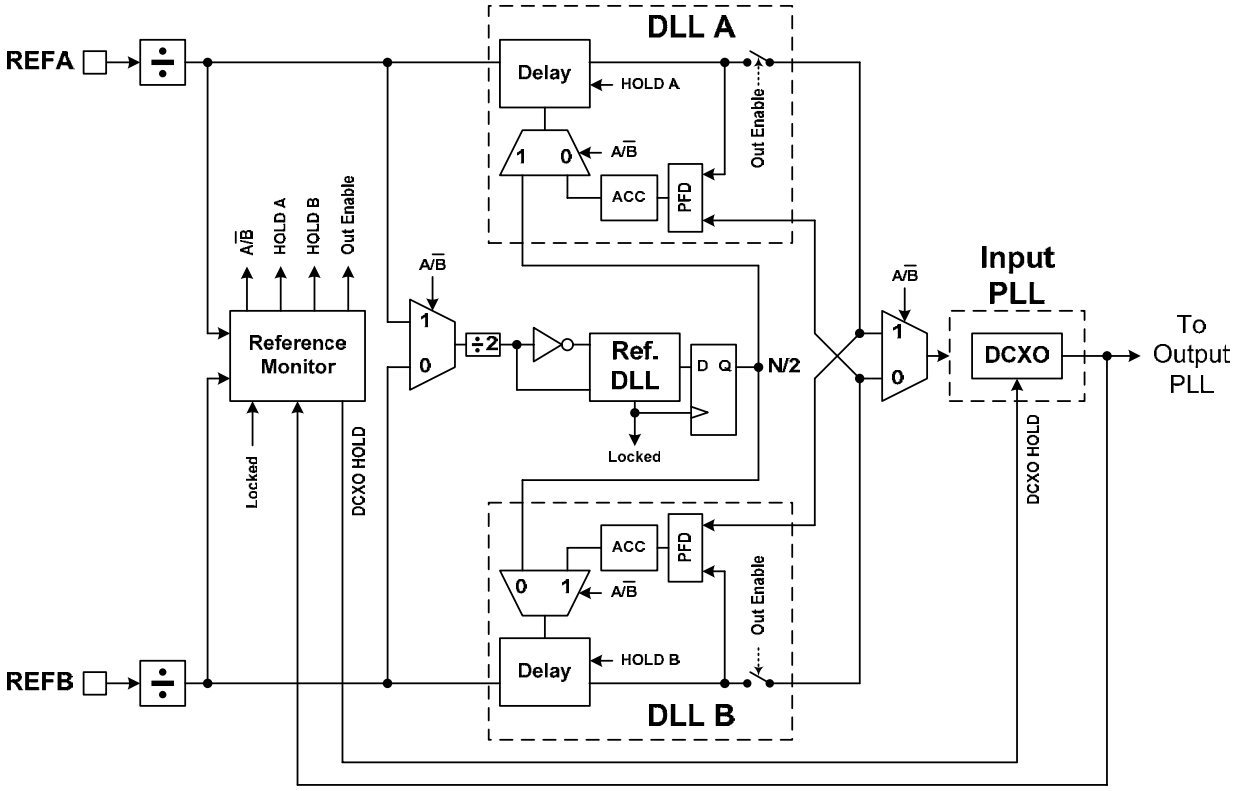


Figure 10: Synchronization Block Diagram

Both the REFA and REFB path have a dedicated DLL (DLL A and DLL B, respectively). DLL A and DLL B are each capable of operating in either an open- or closed-loop mode under the direction of the reference monitor status signals. When the reference monitor selects one of the references as the 'active' reference, the DLL associated with the active reference operates in open-loop mode. While in open-loop mode, the DLL delays the active reference by a constant time interval based on a fixed delay value. So long as one of the references is the active reference, the other is by default the 'alternate' reference. The DLL associated with the alternate reference operates in closed-loop mode. While in closed-loop mode, the DLL automatically adjusts its delay so that the rising edge of the delayed alternate reference is edge aligned with the rising edge of the delayed active reference.

Whenever the reference monitor selects one of the references as the 'active' reference, it switches the output mux to select the output of the DLL associated with the active reference and simultaneously routes the active reference to the reference DLL. The reference DLL automatically measures the period of the active reference (with approximately 250ps accuracy). When the reference DLL locks, the value of its delay setting (N) represents one period of the active reference. Upon acquiring lock, the reference DLL captures N and divides it by two (N/2 corresponds to a delay value that represents a half-cycle of the active reference). Both DLL A and DLL B have access to the N/2 value generated by the reference DLL.

The following paragraphs describe the typical sequence of events that results from a device reset, power-up, or return from holdover mode. The reference monitor is continuously checking for the presence of the divided REFA and/or REFB signals. If both are available, the device arbitrarily selects one of them as the active reference making the other the alternate reference. If only one of the references is available, then it becomes the active reference making the other the alternate reference (assuming it ever becomes available). In either case, two events occur:

1) the output mux selects the output of the active DLL as the source to the input PLL
2) the input mux selects the active reference as the source to the reference DLL

The reference DLL measures the period of the active reference and produces the required N/2 delay value. When the reference DLL locks, three events occur:

1) both DLL A and DLL B are enabled
2) the DLL associated with the active reference enters open-loop mode
3) the DLL associated with the alternate reference enters closed-loop mode.

This implies that the signal driving the input PLL is the active reference (after division by its input divider) delayed by a half cycle.

Since the alternate DLL is in closed-loop mode, and assuming that the alternate reference is available, the output of the alternate DLL is edge-aligned with the delayed output of the active DLL. Furthermore, the closed-loop operation of the alternate DLL causes its delay value to adjust dynamically so that it maintains nominal edge-alignment with the output of the active DLL. Edge alignment of the active and alternate references is the key to the hitless switchover capability of the AD9551.

If the reference monitor detects the loss of the active reference, then it initiates three simultaneous operations:

1) the output mux selects the output of the alternate DLL
2) the alternate DLL holds its most recent delay setting (that is, the delay setting that edge-aligned the output of the alternate DLL with the output of the active DLL).
3) the new active reference is connected to the reference DLL in order to measure its period (i.e. a new N/2 value).

It is item 2) above that ensures hitless switching between references.

Since the failed alternate reference is assigned to the alternate DLL, then upon its return the alternate DLL (which is in closed loop mode) automatically edge aligns the delayed alternate reference with the delayed active reference. Thus, should the new active reference fail, switchover to the alternate reference occurs in a hitless manner. This method of swapping the functionality of DLL A and DLL B as either active (open-loop) or alternate (closed-loop) allows for continuous hitless switching from one reference to the other as needed (assuming the availability of an alternate reference upon failure of the active reference).

NOTE: In the event that both references fail, the device enters holdover mode. In this case, the reference monitor holds the DCXO at its last setting prior to the holdover condition and the DCXO free runs at this setting until the holdover condition expires.

Because the synchronization mechanism autonomously switches between references, the user has no way of knowing which reference is currently the active reference. However, the user can force the device to select a specific input reference as the active reference. For example, to force REFA to be the active reference, power down the REFB input receiver by programming the appropriate registers (or simply disconnect the REFB signal source). The absence of a REFB signal will cause to device to perform a hitless switchover to REFA. If REFA were already the active reference, then the absence of REFB results in no action, and REFA remains the active reference. In this way, the user can ensure that REFA is the

active reference. Likewise, by using the same procedure but reversing the roles of the two references, the user can force the device to select REFB as the active reference.

Input PLL

Fundamentally, the input PLL is a phase-frequency detector (PFD), digital loop filter and digitally controlled crystal oscillator (DCXO) operating in a closed loop. In addition, it contains two frequency doublers, two integer dividers (D and F), an SDM (associated the F divider) and switching logic as shown in Figure 11.

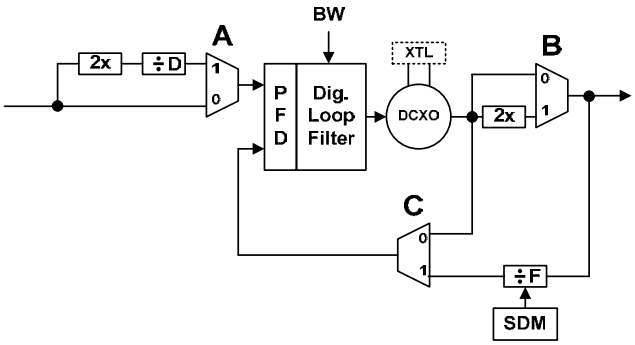


Figure 11: Input PLL

The configuration of the input PLL depends on several factors. These include the state of the frequency selections pins, the state of the bandwidth control bits (Register 33<7:6>), and the state of the frequency doubler bit (Register 1D<2>). A configuration summary appears in Table 14. The Input Mode column is a function of the A(3:0) and B(3:0) frequency selection pins such that if A(3:0)=1111b or B(3:0)=1111b, then the input mode is 19.44 MHz. Otherwise, the input mode is NORMAL.

Table 14: Input PLL configurations

CONTROL SIGNALS				CONFIGURATION						
Input Mode	Register Settings			DCXO Freqeuncy Doubler	MUX A, B & C Control Settings			D & F Divider Settings		SDM (F-divider)
	33		1D							
	Bit 7	Bit 6	Bit 2		A	B	C	D	F	
NORMAL	0	0	0	Disabled	0	0	0	X	X	Disabled
NORMAL	0	0	1	Active	0	1	0	X	X	Disabled
NORMAL	0	1	X	Disabled	1	0	1	4	2	Disabled
NORMAL	1	0	X	Disabled	1	0	1	8	4	Disabled
NORMAL	1	1	X	Disabled	1	0	1	16	8	Disabled
19.44 MHz	X	X	X	Active	1	1	1	5	5	Active

The DCXO relies on an external crystal as its frequency source. The crystal is typically 26 MHz in the normal input mode and 19.44 MHz in the 19.44 MHz input mode. The control loop of the input PLL adjusts the load capacitance on the crystal resonator to push or pull the nominal crystal frequency over a small range (approximately 50 ppm). The control loop allows the DCXO output to lock to the active reference signal. In order to function properly, the AD9551 requires a crystal with a specified load capacitance of 10 pF and frequency tolerance of 20 ppm (see NDK's NX3225SA, for example).

The restricted tuning range of the DCXO has two implications. First, the user must properly choose the divide ratio of the input reference divider in order to establish a frequency that is within the DCXO tuning range. Second, when configuring the AD9551 so that the DCXO is the reference source for the output PLL (default), the jitter/wander associated with the input signal must be low enough to ensure the stability of the DCXO control loop. Generally, the latter implication necessitates the use of the input SDMs because of the additional input jitter

rejection they provide, but this means that fractional division is a requirement in such applications.

The very narrow loop bandwidth of the input PLL (programmable from approximately 3 Hz to 50 Hz) allows the AD9551 to reduce jitter that appears on the input reference signal. This offers improved phase noise performance at the device output by reducing noise that falls within the loop bandwidth of the output PLL (the next stage in the signal chain). Reduced in-band noise delivered to the output PLL results in reduced noise at the final output.

The programming registers allow for bypassing of the entire input PLL section. With the input PLL bypassed the prescaled active input reference signal (after synchronization) routes directly to the PFD of the output PLL. However, even when bypassed the user must still provide an external crystal so that the DCXO is functional, as the reference monitor and reference synchronization blocks use the DCXO output as a clock source.

2x Frequency Multiplier

In normal input mode with the bandwidth control bits in their default state (00b), an optional 2x frequency multiplier is available at the output of the DCXO. This allows the user to take advantage of an increased input frequency delivered to the output PLL, which allows for greater separation between the frequency generated by the output PLL and the associated reference spur. However, increased reference spur separation comes at the expense of the harmonic spurs introduced by the frequency multiplier. As such, beneficial use of the frequency multiplier is application specific.

In normal input mode but with any of the bandwidth control bits set to logic 1, the 2x frequency multiplier is disabled. This is the reason that the divide ratio of the input PLL's F divider is twice that of the D divider when operating in this mode.

When configured for the 19.44 MHz input mode, the device automatically includes the 2x frequency multiplier as part of the input PLL.

Output PLL

The output PLL consists of a phase-frequency detector (PFD), an integrated voltage controlled oscillator (VCO), and a feedback divider with an optional 3rd order SDM that allows for fractional divide ratios. The output PLL produces a nominal 3.7 GHz signal phase-locked to the prescaled active input reference signal.

Phase Frequency Detector and Charge Pump

The PFD of the output PLL drives a charge pump that increases, decreases, or holds constant the charge stored on the loop filter capacitors. The stored charge results in a voltage that sets the output frequency of the VCO. The feedback loop of the PLL causes the VCO control voltage to vary in a way that phase locks the PFD input signals.

The gain of the output PLL is proportional to the current delivered by the charge pump. The device automatically controls the charge pump current based on the prevailing device control settings. However, the user has the ability to override the charge pump current setting, and thereby the PLL gain, via the programming registers.

Loop Filter Capacitor

The output PLL loop filter requires the connection of an external 12 nF capacitor between the LF pin and ground. This value sets the loop bandwidth at approximately 50 kHz and ensures loop stability over the intended operating parameters of the device.

Voltage Controlled Oscillator

The VCO has 128 frequency bands spanning a range of 3350 MHz to 4050 MHz (3700 MHz nominal). However, the actual operating frequency within a particular band depends on the control voltage that appears on the loop filter capacitor. The control voltage causes the VCO output frequency to vary linearly within the selected band. This frequency variability allows the control loop of the output PLL to synchronize the VCO output signal with the reference signal applied to the PFD.

In normal operation, the device automatically selects the appropriate band as part of its calibration process (invoked via the VCO Control register). However, the user can override the automatically selected VCO frequency band via the VCO Band Control bits in the VCO Control register.

Feedback Divider

The feedback divider enables the output PLL to provide integer frequency multiplication (assuming that the feedback SDM is disabled). The integer factor, N, is variable from 0 to 255 via an 8-bit programming register. However, the minimum practical value of N is 64, as this sufficiently reduces the VCO frequency in the feedback path of the output PLL.

Feedback Sigma Delta Modulator

The feedback divider alone provides only integer frequency multiplication. However, the feedback divider is coupled to an optional 3rd order SDM providing fractional division, thereby enabling fractional frequency multiplication. The feedback SDM offers fractional division of the form, N+F/M, where N is the integer part (8 bits), M is the modulus (20 bits), and F is the fractional part (20 bits) with all three parameters being positive integers. The feedback SDM makes it possible for the AD9551 to support a wide range of output frequencies with exact frequency ratios relative to the input reference.

PLL Locked Indicators

Both the input and output PLLs provide a status indicator that appears at an external pin. The indicator signifies when the PLL has acquired a locked condition. The input PLL provides

the INPUT PLL LOCKED signal and the output PLL provides the OUTPUT PLL LOCKED signal.

Output Dividers

Three integer dividers exist in the output chain. The first divider (P_0) yields an integer sub-multiple of the VCO frequency. The second divider (P_1) establishes the frequency at OUT1 as an integer sub-multiple of the output frequency of the P_0 divider. The third divider (P_2) establishes the output frequency at OUT2 as an integer sub-multiple of the OUT1 frequency.

Output Drivers

The user has control over the following output driver parameters via the programming registers:

1. Logic family and pin functionality
2. Polarity (for CMOS family, only)
3. Drive current
4. Power down

The logic families include LVDS, LVPECL and CMOS. Selection of the logic family is via the mode bits in the OUT1 and OUT2 Driver Control register (see Table 15). Regardless of the selected logic family, the output drivers each use two pins. This enables support the differential signals associated with the LVDS and LVPECL logic families. CMOS, on the other hand, is a single ended signal requiring only one output pin, but both output pins are available for optional provision of a dual single-ended CMOS output clock (see the first entry in Table 15).

Table 15: Output Channel Logic Family and Pin Functionality

Mode Bits <2:0>	Logic Family and Pin Functionality
000	CMOS (both pins)
001	CMOS (positive pin), Tri-State (negative pin)
010	Tri-State (positive pin), CMOS (negative pin)
011	Tri-State (both pins)
100	LVDS
101	LVPECL
110	undefined
111	undefined

Assuming that the mode bits indicate the CMOS logic family, the user has control of the logic polarity associated with each CMOS output pin via the OUT1 and OUT2 Driver Control registers.

Assuming that the mode bits indicate the CMOS or LVDS logic family, the user can select whether the output driver uses weak or strong drive capability via the OUT1 and OUT2 Driver Control registers. In the case of the CMOS family, the strong setting simply allows for driving increased capacitive loads. In the case of the LVDS family, the nominal weak and strong drive currents are 3.5 mA and 7 mA, respectively.

The OUT1 and OUT2 Driver Control registers also have a power down bit to enable/disable the output drivers. The power down function is independent of the logic family selection.

Note that unless the user programs the device to allow SPI port control of the output drivers, the drivers default to LVPECL or LVDS depending on the logic level on the OUTSEL pin. For OUTSEL=0 both outputs are LVDS and for OUTSEL=1 both outputs are LVPECL. In the default LVDS mode, the user still can control the drive strength via the SPI port.

HOLDOVER

In the absence of both input references, the device enters holdover mode. Holdover is a secondary function provided by the input PLL. Since the DCXO has an external crystal as its frequency source, it continues to operate in the absence of the input reference signals. When the device switches to holdover the DCXO is held at the frequency it was operating at just prior to switchover. The device continues operating in this mode until a reference signal becomes available. At which point the device exits holdover mode and the input PLL resynchronizes with the active reference.

19.44 MHZ INPUT MODE

This is a special operating mode invoked by the frequency selection pins and occurs when either A(3:0)=1111b or B(3:0)=1111b. This mode allows the AD9551 to support an input rate of 19.44 MHz (a rate common to synchronized network applications).

When the 19.44 MHz input mode is active, the reference input dividers provide programmable divide ratios of 1, 2 or 4 via Register 1E<1:0>. Therefore, the input SDMs are inactive and unavailable. The integer divide ratios allow the device to support the commonly available input rates of 38.88 MHz and 77.76 MHz. Furthermore, when pin programming the device for 19.44 MHz mode the REFA and REFB frequencies must be the same if both input references are used.

In the 19.44 MHz input mode the input PLL architecture includes a frequency scale down of 2/5 at the reference input to its PFD as well as in the feedback path. In this mode, the DCXO's feedback divider includes a 3rd order SDM with a fixed modulus, zero-offset frequency and a PRBS to randomize the SDM output. Note that this SDM is not user-programmable.

When operated with a 19.44 MHz input reference (or a 2x or 4x multiple thereof), the use of a 19.44 MHz external crystal is implied. Under this condition, the input frequency to the DCXO is 7.776 MHz, the output frequency of the DCXO is 19.44 MHz, and the frequency driving the output PLL (f_{IF}) is 38.88 MHz.

Although the 19.44 MHz input mode limits the input divide ratio to 1, 2 or 4, the user still has full control over the output section. This includes the integer and fractional components of

the output PLL feedback divider and the final output dividers (P_0, P_1 and P_2), enabling the synthesis of wide range of output frequencies.

OUTPUT/INPUT FREQUENCY RELATIONSHIP

Below are the three equations that define the frequency at OUT1 and OUT2 (f_{OUT1} and f_{OUT2}, respectively).

$$f_{IF} = f_{REF_{A,B}}\left(\frac{K}{N_{A,B}+\left(\frac{1}{2}+\frac{FRAC_{A,B}}{2(MOD_{A,B})}\right)}\right) \quad \text{EQ 1}$$

$$f_{OUT1} = f_{IF}\left(\frac{N+\frac{FRAC}{MOD}}{P_0 P_1}\right) \quad \text{EQ 2}$$

$$f_{OUT2} = \frac{f_{OUT1}}{P_2} \quad \text{EQ 3}$$

f_{REF} : Input reference frequency with the A or B subscript indicating REFA or REFB, respectively

P_0 , P_1: OUT1 divider values

P_2: OUT2 divider value

K: Input mode scale factor

f_{IF}: Frequency at the input of the output PLL's PFD

$N_{A,B}$, $FRAC_{A,B}$, $MOD_{A,B}$
Input reference divider values with the A or B subscript indicating REFA or REFB, respectively

N , FRAC , MOD
Feedback divider values for the output PLL

The divider values, K, f_{IF} and have the following constraints:

$N_{A,B} \in \{1, 2, \cdots, 63\}$ integer mode

$N_{A,B} \in \{3, 4, \cdots, 63\}$ fractional mode

$FRAC_{A,B} \in \{-1{,}048{,}576, -1{,}048{,}575, \cdots, 1{,}048{,}575\}$

$MOD_{A,B} \in \{1, 2, \cdots, 1{,}048{,}575\}$

$N \in \{64, 65, \cdots, 255\}$

$FRAC \in \{0, 1, \cdots, 1{,}048{,}575\}$

$MOD \in \{1, 2, \cdots, 1{,}048{,}575\}$

$P_0 \in \{4, 5, \cdots, 11\}$

$P_1 \in \{1, 2, \cdots, 63\}$

$P_2 \in \{1, 2, \cdots, 63\}$

$K \in \{1, 2\}$:

K=1 when using the normal input mode without the 2x multiplier

K=2 when using the normal input mode with the 2x multiplier or when using the 19.44 MHz input mode

f_{IF}:

$$\left(\frac{3350}{N+\frac{FRAC}{MOD}}\right)MHz \le f_{IF} \le \left(\frac{4050}{N+\frac{FRAC}{MOD}}\right)MHz$$

$$13.2\,MHz \le f_{IF} \le 30\,MHz\big|_{K=1}$$

$$13.2\,MHz \le f_{IF} \le 55\,MHz\big|_{K=2\ or\ DCXO\ bypassed}$$

$$\frac{f_{REF_A}}{N_A+\left(\frac{1}{2}+\frac{FRAC_A}{2(MOD_A)}\right)} = \frac{f_{REF_B}}{N_B+\left(\frac{1}{2}+\frac{FRAC_B}{2(MOD_B)}\right)}$$

Assuming that the DCXO is not bypassed, the user must carefully consider the operating frequency of the externally connected crystal resonator. Because the DCXO is only capable of pulling the crystal over a 50 ppm range, the output frequency of the DCXO is essentially identical to the crystal frequency. The user must choose a crystal based on the desired value of f_{IF} such that: $f_{IF} = K(f_{CRYSTAL})$.

The denominator of EQ 1 is the input division factor, which has an integer part ($N_{A,B}$) due to an integer divider and an optional fractional part associated with the input SDM ($½ + FRAC_{A,B}/(2\times MOD_{A,B})$).

NOTE: When bypassing the SDM the device forces the fractional part to zero (equivalent to $FRAC_{A,B} = -MOD_{A,B}$).

The numerator of the f_{OUT1} equation contains the feedback division factor, which has an integer part (N) due to an integer divider along with an optional fractional part (FRAC/MOD) associated with the feedback SDM.

EQ 1 and EQ 2 and the constraints placed on their variables, leads to the conclusion that f_{REF} and f_{OUT1} must be rationally related. That is, the ratio f_{OUT1}/f_{REF} must be expressible as a ratio of integers. Thus, it is not possible to configure the device for a frequency ratio of $1/\sqrt{2}$ because the denominator is an irrational number, which violates the constraints on EQ 1 and EQ 2.

HOW TO CALCULATE DIVIDER VALUES

This section provides a 5-step procedure for calculating the divider values given a specific f_{OUT1}/f_{REF} ratio. The methodology is described in general terms, but a specific example is provided for clarity. The example assumes the use of the frequency control pins with A3:0 = 0010 and Y3:0 = 0100 (see Table 11 and Table 12). The example parameters are as follows:

$$f_{REF} = 622.08\left(\frac{239}{237}\right)MHz$$

$$f_{OUT1} = 625\left(\frac{66}{64}\right)MHz$$

$$f_{IF} = 26\ MHz$$

STEP 1: Ensure that f_{OUT1} and f_{REF} are rationally related.

As shown below, f_{OUT1}/f_{REF} is expressible as a ratio of two integers, so f_{OUT1} and f_{REF} are rationally related.

$$\frac{f_{OUT1}}{f_{REF}} = \frac{625\left(\frac{66}{64}\right)}{622.08\left(\frac{239}{237}\right)} = \frac{625(66)(237)(100)}{62208(239)(64)} = \frac{977{,}625{,}000}{951{,}553{,}568}$$

STEP 2: Determine the output divide factor (ODF).

Note that the VCO frequency (f_{VCO}) spans 3350 MHz to 4050 MHz. The ratio, f_{VCO}/f_{OUT1}, indicates the required ODF. Given the specified value of f_{OUT1} (~644.53 MHz) and the range of f_{VCO}, the ODF spans a range of 5.2 to 6.3. The ODF must be an integer, which means that ODF = 6 (as this is the only integer between 5.2 and 6.3).

STEP 3: Determine suitable values for P_0 and P_1.

The ODF is the product of the two output dividers, so ODF = P_0P_1. It has already been determined that ODF = 6 for the given example. Therefore, we have $P_0P_1 = 6$ with the constraints that P_0 and P_1 are both integers and that $4 \le P_0 \le 11$ (see the Output/Input Frequency Relationship section). These constraints lead to the singular solution: $P_0 = 6$ and $P_1 = 1$.

Although this particular example yields a singular solution for the output divider values with $f_{OUT1} \approx 644.53$ MHz, some f_{OUT1} frequencies result in multiple ODFs rather than just one. For example, if $f_{OUT1} = 100$ MHz the ODF ranges from 34 to 40. This leads to an assortment of possible values for P_0 and P_1 as shown in Table 16.

The P_0 and P_1 combinations listed in Table 16 are all equally valid. However, note that they yield only three valid ODF values (35, 36, 40) from the original range of 34-40.

Table 16: Combinations of P_0 and P_1

P_0	P_1	ODF
4	9	36
4	10	40
5	7	35
5	8	40
6	6	36
7	5	35
8	5	40
9	4	36
10	4	40

STEP 4: Determine the feedback divider values for the output PLL.

Repeat this step for each ODF when multiple ODFs exist (for example, 35, 36 and 40 in the case of Table 16).

To calculate the feedback divider values for a given ODF use the following equation:

$$\left(\frac{f_{OUT1}}{f_{IF}}\right) \times ODF = \frac{X}{Y}$$

Notice that the left-hand side contains variables with known quantities. Furthermore, the values are necessarily rational, so the left-hand side is expressible as a ratio of two integers, X and Y.

Example: $$\frac{\left(625\left[\frac{66}{64}\right]\right)(6)}{26} = \frac{625(66)(6)}{26(64)} = \frac{247{,}500}{1664} = \frac{X}{Y}$$

In the context of the AD9551, X/Y is always an improper fraction. Therefore, it is expressible as the sum of an integer, N, and the proper fraction, R/Y (R and Y are integers).

$$\frac{X}{Y} = N + \frac{R}{Y}$$

Example: $$\frac{247{,}500}{1664} = N + \frac{R}{Y}$$

Therefore, the example yields N = 148, Y = 1664 and R = 1228. To arrive at this result, use long division to convert the improper fraction, X/Y, to an integer (N) and proper fraction (R/Y). Note that dividing Y into X by means of long division yields an integer, N and remainder, R. The proper fraction has numerator, R (the remainder), and denominator, Y (the divisor), as shown below:

$$\begin{array}{r} N \\ Y\overline{)\,X} \\ -NY \\ \hline R \end{array} \quad \Rightarrow \quad \frac{X}{Y} = N + \frac{R}{Y}$$

It is imperative to use long division to obtain the correct results. Avoid the use of a calculator or math program, as these do not always yield correct results due to internal rounding and/or truncation. Some calculators or math programs may be up to the task if they can handle very large integer operations, but such are not common.

In the example, N = 148 and R/Y = 1228/1664, which reduces to R/Y = 307/416. These values of N, R and Y constitute the respective feedback divider values:

N = 148 FRAC = 307 MOD = 416

The only caveat is that N and MOD must meet the constraints given in the Output/Input Frequency Relationship section.

In the example, FRAC is non-zero, so the division value is an integer plus the fractional component, FRAC/MOD. This implies that the feedback SDM is necessary as part of the

feedback divider. If FRAC=0, then the feedback division factor is an integer and the SDM is not required (it may be bypassed).

Although the feedback divider values obtained in this way provide the proper feedback divide ratio to synthesize the exact output frequency, they may not yield optimal jitter performance at the final output. One reason for this is that the value of MOD defines the period of the SDM, which has a direct impact on the spurious output of the SDM. Specifically, the SDM spectrum will have MOD evenly spaced spurs between DC and f_{IF}. Thus, the spectral separation (Δf) of the spurs associated with the feedback SDM is:

$$\Delta f = \frac{f_{IF}}{MOD}$$

Since the SDM is in the feedback path of the output PLL, these spurs appear in the output signal as spurious components offset by Δf from f_{OUT1}. Hence, a small MOD value produces relatively large spurs with relatively large frequency offsets from f_{OUT1}, while a large MOD value produces smaller spurs but more closely spaced to f_{OUT1}. Clearly, the value of MOD has a direct impact on the spurious content (i.e. jitter) at OUT1.

Generally, the largest possible MOD value yields the smallest spurs. Thus, it is desirable to scale MOD and FRAC by the integer part of 2^{20} divided by the value of MOD obtained above. In the example, the value of MOD is 416, yielding a scale factor of 2520 (the integer part of $2^{20}/416$). A scale factor of 2520 leads to FRAC = 307×2520 = 773,640 and MOD = 416×2520 = 1,048,320.

However, these FRAC and MOD values are different from those that appear in Table 12 (Y3:0=0100). The reason is that a scale factor of 1120 (instead of 2520) was found to yield the most acceptable overall performance. A scale factor of 1120 results in the Table 12 values: FRAC = 343,840 and MOD = 465,920.

STEP 5: Determine the values of the REFA (or REFB) input dividers.

To calculate the feedback divider values use the following equation:

$$\frac{f_{REF}}{f_{IF}} = \frac{X}{Y}$$

Notice that the left-hand side contains variables with known quantities. Furthermore, the values are necessarily rational, so the left-hand side is expressible as a ratio of two integers, X and Y.

Example: $$\frac{622.08\left(\frac{239}{237}\right)}{26} = \frac{62208(239)}{100(26)(237)} = \frac{14{,}867{,}712}{616{,}200} = \frac{X}{Y}$$

As in STEP 4, use long division to convert the fraction, X/Y, to an integer, N, and proper fraction, R/Y (R and Y are integers). The same caution given in STEP 4 applies here regarding the need to use long division rather than a calculator or math program.

Given the example of X = 14,867,712 and Y = 616,200, long division yields: N = 24 and R/Y = 78,912/616,200, which reduces to R/Y = 3,288/25,675. The only caveats are that N must meet the constraints for $N_{A,B}$ given in the Output/Input Frequency Relationship section and that $Y < 2^{19}$ (524,288).

Now use R and Y to compute: Q = 2R – Y

Using R = 3,288 and Y = 25,675, from the above example yields:

$$Q = 2(3{,}288) - 25{,}675 = -19{,}099$$

These values of N, Q and Y constitute the respective input divider values:

$N_{A,B} = 24$ $FRAC_{A,B} = -19{,}099$ $MOD_{A,B} = 25{,}675$

In the example, $FRAC_{A,B}$ is non-zero, so the division value is an integer plus the fractional component, $FRAC_{A,B}/MOD_{A,B}$. This implies that the input SDM is necessary as part of the input divider. If $FRAC_{A,B} = 0$, then the input division factor is an integer and the SDM is not required (it may be bypassed).

The choice of $MOD_{A,B}$ affects the jitter performance of the input section in a manner similar to the feedback dividers. However, the spectral spacing of the spurs for the input SDMs is:

$$\Delta f_{A,B} = \frac{f_{REF_{A,B}}}{(MOD_{A,B})(2N_{A,B}+1)+FRAC_{A,B}}$$

The input SDMs are similar to the feedback SMD in that it is desirable to scale $MOD_{A,B}$ and $FRAC_{A,B}$ by the integer part of 2^{19} divided by the value of $MOD_{A,B}$ obtained above. In the example, the value of $MOD_{A,B}$ is 25,675, yielding a scale factor of 20 (the integer part of $2^{19}/25{,}675$). A scale factor of 20 leads to $FRAC_{A,B}$ = –19,099×20 = –381,980 and $MOD_{A,B}$ = 25,675×20 = 513,500.

However, these $FRAC_{A,B}$ and $MOD_{A,B}$ values are different than those that appear in Table 11 (A3:0=0010). The reason is that a scale factor of 6 (instead of 20) was found to yield the most acceptable overall performance. A scale factor of 6 results in the Table 11 values: $FRAC_{A,B}$ = –19,099×6 = –114,594 and $MOD_{A,B}$ = 25,675×6 = 154,050.

LOW DROP OUT REGULATORS

The AD9551 is powered from a single 3.3 V supply and contains on-chip LDO regulators for each function to eliminate the need for external LDOs. To ensure optimal performance each LDO output should have a 0.47µF capacitor connected

between its access pin and ground with the exception of the VCO LDO which requires a 0.1µF capacitor instead.

SERIAL CONTROL PORT

The AD9551 serial control port is a flexible, synchronous, serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9551 serial control port is configured for a single bidirectional I/O pin (SDIO only).

SERIAL CONTROL PORT PIN DESCRIPTIONS

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin and acts as input only or input/output. The AD9551 defaults to bidirectional pins for I/O.

$\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, SDIO is in a high impedance state. This pin is internally pulled up by a 100 kΩ resistor to 3.3 V. It should not be left floating. See the Operation of Serial Control Port section on the use of the $\overline{CS}$ in a communication cycle.

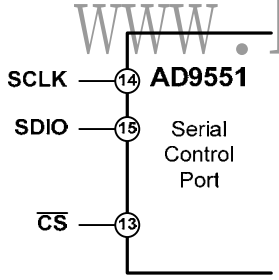


Figure 12. Serial Control Port

OPERATION OF SERIAL CONTROL PORT

Framing a Communication Cycle with $\overline{CS}$

A communication cycle (a write or a read operation) is gated by the $\overline{CS}$ line. $\overline{CS}$ must be brought low to initiate a communication cycle.

$\overline{CS}$ stall high is supported in modes where three or fewer bytes of data (plus instruction data) are transferred (W1:W0 must be set to 00, 01, or 10; see Table 17). In these modes, $\overline{CS}$ can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. $\overline{CS}$ can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer. During this period, the serial control port state machine enters a wait state until all data has been sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset by either completing the remaining transfer or by returning the $\overline{CS}$ low for at least one complete SCLK cycle (but fewer than eight SCLK cycles). A rising edge on the $\overline{CS}$ pin on a non-byte boundary terminates the serial transfer and flushes the buffer.

In the streaming mode (W1:W0 = 11), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). $\overline{CS}$ must be raised at the end of the last byte to be transferred, thereby ending the stream mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9551. The first writes a 16-bit instruction word into the AD9551, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9551 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation (I15 = 0), the second part is the transfer of data into the serial control port buffer of the AD9551. The length of the transfer (1, 2, 3 bytes, or streaming mode) is indicated by 2 bits (W1:W0) in the instruction byte. The length of the transfer indicated by (W1:W0) does not include the two-byte instruction. $\overline{CS}$ can be raised after each sequence of 8 bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is lowered. Stalling on non-byte boundaries resets the serial control port.

There are three types of registers on the AD9551: buffered, live, and read-only. Buffered (also referred to as mirrored) registers require an I/O update to transfer the new values from a temporary buffer on the chip to the actual register and are marked with an M in the column labeled Type of the register map. Toggling the IO_UPDATE pin or writing a 1 to the Register Update bit (Register 0005[0]) causes the update to occur. Because any number of bytes of data can be changed before issuing an update command, the update simultaneously enables all register changes since any previous update. Live registers do not require I/O update and update immediately after being written. Read-only registers ignore write commands and are marked RO in the Type column of the register map. The Type column of the register map may also have an AC, which indicates that the register is auto-clearing.

Read

If the instruction word is for a read operation (I15 = 1), the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1, 2, 3, 4 as determined by W1:W0. In this case, 4 is used for streaming mode where 4 or more words are transferred per read. The data readback is valid on the falling edge of SCLK.

The default mode of the AD9551 serial control port is bidirectional mode, and the data readback appears on the SDIO pin.

By default, a read request reads the register value that is currently in use by the AD9551. However, setting Register 0004[0] = 1 causes the buffered registers to be read instead. The buffered registers are the ones that take effect during the next I/O update.

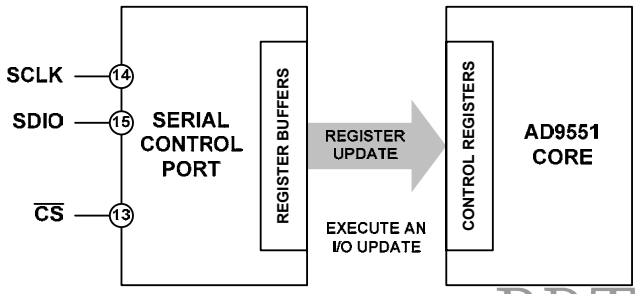


Figure 13: Relationship Between Serial Control Port Register Buffers and Control Registers of the AD9551

The AD9551 uses Register 0000 to Register 0509. Although the AD9551 serial control port allows both 8-bit and 16-bit instructions, the 8-bit instruction mode provides access to five address bits (A4 to A0) only, which restricts its use to the address space 0x00 to 0x01. The AD9551 defaults to 16-bit instruction mode on power-up, and the 8-bit instruction mode is not supported.

THE INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits, W1:W0, are the transfer length in bytes. The final 13 bits are the address (A12:A0) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data per Bits W1:W0, which is interpreted according to Table 17.

Bits [A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. The AD9551 uses all of the 13-bit address space. For multibyte transfers, this address is the starting byte address.

Table 17. Byte Transfer Count

W1	W0	Bytes to Transfer (Excluding the 2-Byte Instruction)
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

MSB/LSB FIRST TRANSFERS

The AD9551 instruction word and byte data may be MSB first or LSB first. The default for the AD9551 is MSB first. The LSB first mode can be set by writing a 1 to Register 0000[6] and requires that an I/O update be executed. Immediately after the LSB first bit is set, all serial control port operations are changed to LSB first order.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from high address to low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB First = 1 (LSB first), the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial control port internal byte address generator increments for each byte of the multibyte transfer cycle.

The AD9551 serial control port register address decrements from the register address just written toward 0000h for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the serial control port register address increments from the address just written toward 0x1FFF for multibyte I/O operations.

Unused addresses are not skipped during multibyte I/O operations. The user should write the default value to a reserved register and should only write zeros to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 18. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB														LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	W1	W0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

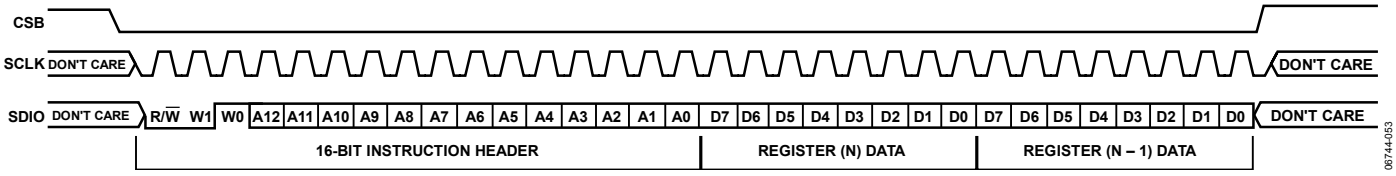


Figure 14. Serial Control Port Write—MSB First, 16-Bit Instruction, 2 Bytes Data

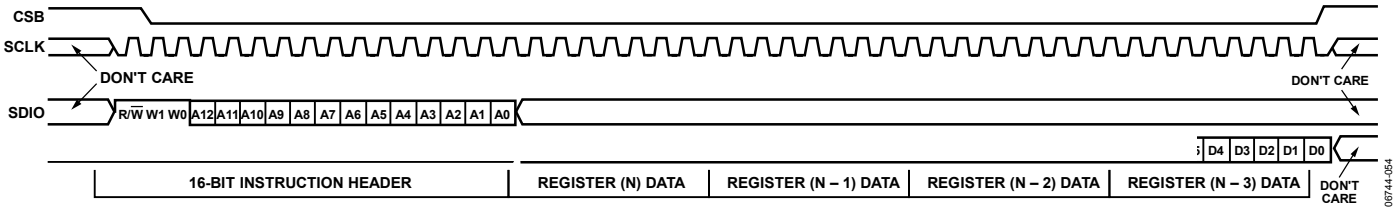


Figure 15. Serial Control Port Read—MSB First, 16-Bit Instruction, 4 Bytes Data

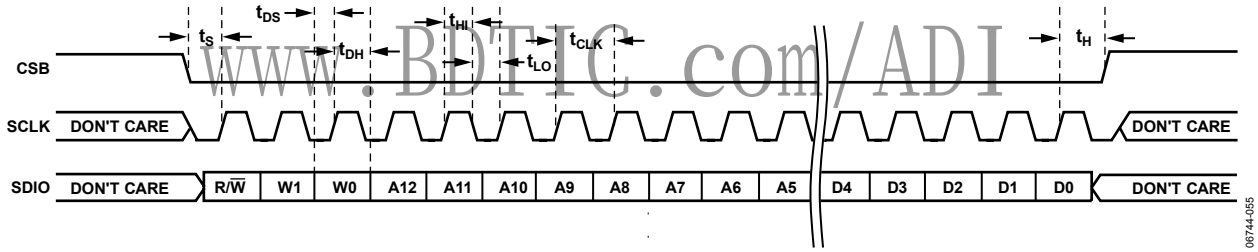


Figure 16. Serial Control Port Write: MSB First, 16-Bit Instruction, Timing Measurements

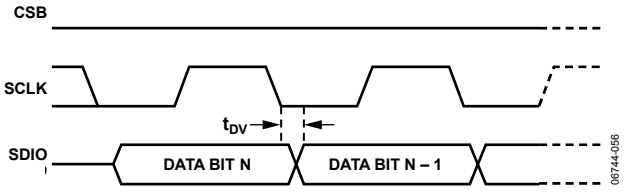


Figure 17. Timing Diagram for Serial Control Port Register Read

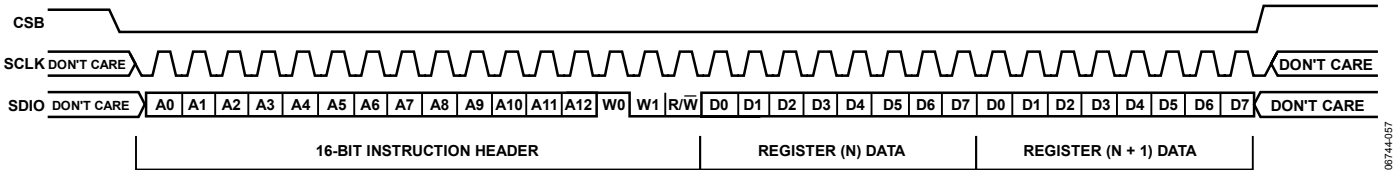


Figure 18. Serial Control Port Write—LSB First, 16-Bit Instruction, 2 Bytes Data

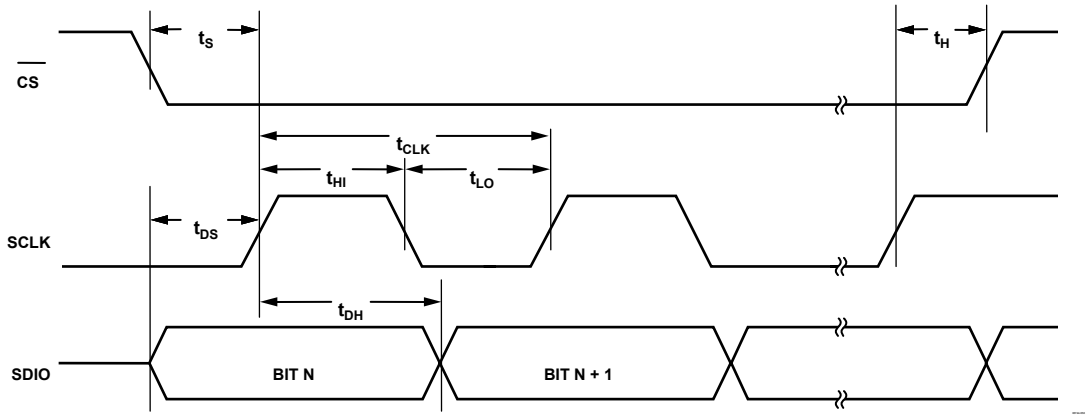


Figure 19. Serial Control Port Timing—Write

Table 19. Definitions of Terms Used in Serial Control Port Timing Diagrams

Parameter	Description
t_{CLK}	Period of SCLK
t_{DV}	Read data valid time (time from falling edge of SCLK to valid data on SDIO)
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_S	Setup time between $\overline{CS}$ and SCLK
t_H	Hold time between $\overline{CS}$ and SCLK
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state

REGISTER MAP

A bit labeled "autoclear" is active high. The control logic automatically returns it to a logic 0 state when the indicated task is completed.
A bit labeled "autoset" is active low. The control logic automatically returns it to a logic 1 state when the indicated task is completed.

Addr (hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default
00	Serial Port Config	0	LSB First	Device Reset (autoclear)	1	1	Device Reset	LSB First	0	18h
04	Read Back Control	unused							Read Back Control	00h
05	IO update	unused							I/O Update (autoclear)	00h
0A	Output PLL PFD and Charge Pump	Charge pump current <7:0> (3.5μA granularity, ~900μA full scale)								80h
0B	Output PLL PFD and Charge Pump	Enable SPI control of charge pump current	Enable SPI control of anti backlash period	CP mode <1:0>		Enable CP mode control	PFD feedback input edge control	PFD reference input edge control	Force VCO to midpoint frequency	30h
0C	Output PLL PFD and Charge Pump	ignored	CP offset current polarity	CP offset current <1:0>		Enable CP offset current control	(reserved) Enable PFD up divide-by-2	(reserved) Enable PFD down divide-by-2	(reserved) Enable feedback divide-by-2	00h
0D	Output PLL PFD and Charge Pump	Anti backlash control <1:0>		unused					Output PLL lock detector power down	00h
0E	VCO Control	Calibrate VCO (autoclear)	Enable Automatic Level Control	Automatic Level Control Threshold <2:0>			Enable SPI control of VCO calibration	Boost VCO supply	Enable SPI control of VCO band setting	70h
0F	VCO Control	VCO bias control <5:0>						unused		80h
10	VCO Control	VCO band control <6:0>							unused	80h
11	Output PLL Control	N<7:0> (Output SDM integer part)								00h
12	Output PLL Control	MOD<19:12> (Output SDM modulus)								80h
13	Output PLL Control	MOD<11:4> (Output SDM modulus)								00h
14	Output PLL Control	MOD<3:0> (Output SDM modulus)				Enable SPI Control of Output Frequency	Bypass output SDM	Output SDM disable	Output PLL Reset	00h
15	Output PLL Control	FRAC<19:12> (Output SDM fractional part)								20h
16	Output PLL Control	FRAC<11:4> (Output SDM fractional part)								00h
17	Output PLL Control	FRAC<3:0> (Output SDM fractional part)				Enable Output PLL Locked pin as test port	Test mux control <1:0>		P1 divider bit <5>	01h
18	Output PLL Control	P1 divider bits <4:0>					P0 divider bits <2:0>			00h
19	Output PLL Control	Enable SPI control of OUT1 dividers	Enable SPI control of OUT2 divider	P2 divider bit <5:0>						20h
1A	Input Receiver & Bandgap	Receiver RESET (active low) (autoset)	Bandgap voltage adjust <4:0> (00000=maximum, 11111=minimum)					Receiver power down enable	Enable SPI control of bandgap voltage	80h
1B	DCXO Control	Enable SPI control of DCXO	Enable SPI control of DCXO	DCXO tuning capacitor control <5:0>						00h

Addr (hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default
		tuning cap.	varactor							
1C	DCXO Control	DCXO varactor control <12:5>								00h
1D	DCXO Control	DCXO varactor control <4:0>					Enable frequency doubler	DCXO bypass	ignored	00h
1E	REFA Frequency	Enable SPI control of REFA SDM	REFA SDM bypass	REFA SDM enable	REFA enable	unused	REF SDM PRBS disable	19.44 MHz Input Mode Divider Select		30h
1F	REFA Frequency	FRACA<19:12> (REFA SDM fractional part)								40h
20	REFA Frequency	FRACA<11:4> (REFA SDM fractional part)								00h
21	REFA Frequency	FRACA<3:0> (REFA SDM fractional part)				unused				00h
22	REFA Frequency	NA<5:0> (REFA SDM integer part)					unused			10h
23	REFA Frequency	Must be 0	MODA<18:12> (REFA SDM modulus)							80h
24	REFA Frequency	MODA<11:4> (REFA SDM modulus)								00h
25	REFA Frequency	MODA<3:0> (REFA SDM modulus)				unused				00h
26	REFB Frequency	Enable SPI control of REFB SDM	REFB SDM bypass	REFB SDM enable	REFB enable	unused				30h
27	REFB Frequency	FRACB<19:12> (REFB SDM fractional part)								40h
28	REFB Frequency	FRACB<11:4> (REFB SDM fractional part)								00h
29	REFB Frequency	FRACB<3:0> (REFB SDM fractional part)				unused				00h
2A	REFB Frequency	NB<5:0> (REFB SDM integer part)					unused			10h
2B	REFB Frequency	Must be 0	MODB<18:12> (REFB SDM modulus)							80h
2C	REFB Frequency	MODB<11:4> (REFB SDM modulus)								00h
2D	REFB Frequency	MODB<3:0> (REFB SDM modulus)				unused				00h
2E	REFA Delay	Enable SPI control of REFA delay	REFA delay control <8:2>							40h
2F	REFA Delay	REFA delay control <1:0>		unused						00h
30	REFB Delay	Enable SPI control of REFB delay	REFB delay control <8:2>							40h
31	REFB Delay	REFB delay control <1:0>		unused						00h
32	OUT1 Driver Control	OUT1 drive strength	OUT1 power down	OUT1 mode control <2:0>			OUT1 CMOS polarity <1:0>		Enable SPI control of OUT1 driver control	A8h
33	Misc.	Input PLL bandwidth <1:0>		Input PLL gain <1:0>		Crystal bypass	unused			00h
34	OUT2 Driver Control	OUT2 drive strength	OUT2 power down	OUT2 mode control <2:0>			OUT2 CMOS polarity <1:0>		Enable SPI control of OUT2 driver control	A8h

REGISTER MAP DESCRIPTION

Control bit functions are active high unless stated otherwise. Register address values are always hexadecimal unless otherwise indicated.

SERIAL PORT CONTROL (REG 00 – 05)

Table 20:

Address	Bit(s)	Bit Name	Description
00	<7>	ususued	Forced to logic 0 internally, which enables 3-wire mode, only
	<6>	LSB First	Bit order for SPI port: 0 (default) = most significant bit and byte first 1 = least significant bit and byte first
	<5>	Soft Reset	Software initiated reset (register values set to default). This is an auto-clearing bit.
	<4>	unused	Forced to logic 1 internally, which enables 16-bit mode (the only mode supported by the device)
	<3:0>	unused	Mirrored version of the contents of <7:4> (that is, <3:0>=<4:7>).
04	<7:1>	unused	
	<0>	Read Back Control	For buffered registers, serial port read-back reads from actual (active) registers instead of the buffer: 0 (default) = reads values currently applied to the device's internal logic 1 = reads buffered values that take effect on next assertion of I/O update
05	<7:1>	unused	
	<0>	I/O Update	Writing a 1 to this bit transfers the data in the serial I/O buffer registers to the device's internal control registers. This is an auto-clearing bit.

OUTPUT PLL CHARGE PUMP & PFD CONTROL (REG 0A – 0D)

Table 21:

Address	Bit(s)	Bit Name	Description
0A	<7:0>	Output PLL PFD and CP Control	These bits set the magnitude of the output PLL charge pump current. The granularity is ~3.5 µA with a full-scale magnitude of ~900 µA. Register 0A is ineffective unless Register 0B<7>=1. Default is 0x80, or 450 µA.
0B	<7>	Enable SPI control of charge pump current	Controls functionality of Register 0A: 0 (default) = the device automatically controls the charge pump current 1 = charge pump current defined by Register 0A
	<6>	Enable SPI control of anti-backlash period	Controls functionality of Register 0D<7:6>: 0 (default) = the device automatically controls the anti-backlash period 1 = anti-backlash period defined by Register 0D<7:6>
	<5:4>	CP mode	Controls the mode of the output PLL charge pump: 00 = tri-state 01 = pump up 10 = pump down 11 (default) = normal
	<3>	Enable CP mode control	Controls functionality of <5:4>: 0 (default) = the device automatically controls the charge pump mode 1 = charge pump mode defined by <5:4>
	<2>	PFD feedback input edge control	Selects the polarity of the active edge of the output PLL's feedback input:: 0 (default) = positive edge 1 = negative edge
	<1>	PFD reference input edge control	Selects the polarity of the active edge of the output PLL's reference input: 0 (default) = positive edge 1 = negative edge
	<0>	Force VCO to	Select VCO control voltage functionality:

Address	Bit(s)	Bit Name	Description
		midpoint frequency	0 (default) = normal VCO operation 1 = force VCO control voltage to mid-scale
0C	<7>	unused	
	<6>	CP offset current polarity	Selects the polarity of the output PLL's charge pump offset current: 0 (default) = pump up 1 = pump down This bit is ineffective unless <3>=1.
	<5:4>	CP offset current	Controls the magnitude of the output PLL's charge pump offset current as a fraction of the value in Register 0A. Ineffective unless <3>=1: 00 (default) = 1/2 01 = 1/4 10 = 1/8 11 = 1/16
	<3>	Enable CP offset current control	Controls functionality of <6:4>: 0 (default) = the device automatically controls charge pump offset current 1 = charge pump offset current defined by <6:4>
	<2>	reserved	Enables PFD up divide-by-2 (reserved for test)
	<1>	reserved	Enables PFD down divide-by-2 (reserved for test)
	<0>	reserved	Enables feedback divide-by-2 (reserved for test)
0D	<7:6>	Anti-backlash control	Controls the PFD anti-backlash period of the output PLL: 00 (default) = minimum 01 = low 10 = high 11 = maximum These bits are ineffective unless Register 0B<6>=1.
	<5:1>	unused	
	<0>	Output PLL lock detector power down	Controls power down of the output PLL's lock detector: 0 (default) = lock detector active 1 = lock detector powered down

VCO CONTROL (REG 0E – 10)

Table 22:

Address	Bit(s)	Bit Name	Description
0E	<7>	Calibrate VCO	Initiates VCO calibration (this is an auto-clearing bit). This bit is ineffective unless <2>=1.
	<6>	Enable automatic level control	Controls functionality of Register 0F<7:2>: 0 = VCO threshold defined by Register 0F<7:2> 1 (default) = the device automatically controls the VCO threshold level
	<5:3>		Controls the VCO threshold detector level from minimum (000) to maximum (111), default is 110.
	<2>	Enable SPI control of VCO calibration	Enables functionality of <7>: 0 (default) = the device performs VCO calibration automatically 1 = bit <7> controls VCO calibration
	<1>	Boost VCO supply	Selects VCO supply voltage: 0 (default) = normal supply voltage 1 = increase supply voltage by 100 mV
	<0>	Enable SPI control of VCO band setting	Controls VCO band setting functionality: 0 (default) = the device automatically selects the VCO band 1 = VCO band defined by Register 10<7:1>
0F	<7:2>	VCO level control	Controls the VCO amplitude from minimum (00 0000) to maximum (11 1111), default is 10 0000.
	<1:0>	unused	

Address	Bit(s)	Bit Name	Description
10	<7:1>	VCO band control	Controls the VCO frequency band from a minimum (000 0000) to maximum (111 1111), default is 100 0000.
	<0>	unused	

OUTPUT PLL CONTROL (REG 11 – 19)

Table 23:

Address	Bit(s)	Bit Name	Description
11	<7:0>	N	8-bit integer divide value for the output SDM. Default is 0x00. NOTE: Operational limitations impose a lower bound of 64 (0x40) on N.
12	<7:0>	MOD	Bits <19:12> of the 20-bit modulus of the output SDM.
13	<7:0>	MOD	Bits <11:4> of the 20-bit modulus of the output SDM.
14	<7:4>	MOD	Bits <3:0> of the 20-bit modulus of the output SDM. Default is MOD = 1000 0000 0000 0000 0000 (524,288).
	<3>	Enable SPI control of output frequency	Controls output frequency functionality: 0 (default) = output frequency defined by pins C3:0 1 = contents of Registers 11 – 14 define output frequency via N, MOD and FRAC.
	<2>	Bypass output SDM	Controls bypassing of the output SDM: 0 (default) = allow integer-plus-fractional division 1 = allow only integer division
	<1>	Output SDM disable	Controls the output SDM internal clocks: 0 (default) = normal operation (SDM clocks active) 1 = SDM disables (SDM clocks stopped)
	<0>	Output PLL reset	Controls initialization of the output PLL: 0 (default) = normal operation 1 = resets the counters and logic associated with the output PLL, but does not affect the output dividers.
15	<7:0>	FRAC	Bits <19:12> of the 20-bit fractional part of the output SDM.
16	<7:0>	FRAC	Bits <11:4> of the 20-bit fractional part of the output SDM.
17	<7:4>	FRAC	Bits <3:0> of the 20-bit fractional part of the output SDM. Default is FRAC = 0010 0000 0000 0000 0000 (131,072).
	<3>	Enable Output PLL Locked pin as test port	Controls the Output PLL Locked pin functionality: 0 (default) = Output PLL Locked pin indicates status of PLL lock detector 1 = Output PLL Locked pin indicates the signal defined by <2:1>
	<2:1>	Test mux control	Selects test mux output: 00 (default) = front end test clock 01 = PFD up divide-by-2 10 = PFD down divide-by-2 11 = PLL feedback divide-by-2 These bits are ineffective unless <3>=1.
	<0>	P1	Bit <5> of the 6-bit P1 divider for OUT1.
18	<7:3>	P1	Bits <4:0> of the 6-bit P1 divider for OUT1 (1 ≤ P1 ≤ 63). Do not program 000000. Default is P1 = 32. The P1 bits are ineffective unless Register 19<7>=1.
	<2:0>	P0	Bits <2:0> of the 3-bit P0 divider for OUT1. The P0 divide value is as follows: 000 (default) = 4 001 = 5 010 = 6 011 = 7 100 = 8 101 = 9 110 = 10 111 = 11

Address	Bit(s)	Bit Name	Description
			The P0 bits are ineffective unless Register 19<7>=1.
19	<7>	Enable SPI control of OUT1 dividers	Controls functionality of OUT1 dividers: 0 (default) = OUT1 dividers defined by pins Y3:0 1 = contents of Register 17 and 18 define OUT1 dividers (P0 and P1)
	<6>	Enable SPI control of OUT2 divider	Controls functionality of OUT2 divider: 0 (default) = OUT2 divider defined by pins Y3:0 (P2=1) 1 = contents of <5:0> define P2
	<5:0>	P2	Bits <5:0> of the 6-bit P2 divider for OUT2 (1 ≤ P2 ≤ 63). Do not program 000000. Default is P2 = 32. The P2 bits are ineffective unless Register 19<6>=1.

INPUT RECEIVERS CONTROL (REG 1A)

Table 24:

Address	Bit(s)	Bit Name	Description
1A	<7>	Receiver reset	Input receiver reset control (this is an auto-clearing bit): 0 = reset input receiver logic 1 (default) = normal operation
	<6:2>	Bandgap voltage adjust	Controls the bandgap voltage setting from minimum (0 0000) to maximum (1 1111). Default is 0 0000.
	<1>	Receiver power down enable	Controls the option to power down the REFA and/or REFB receiver via Registers 1E<4> and 26<4>: 0 (default) = option disabled 1 = option enabled
	<0>	Enable SPI control of bandgap voltage	Enables functionality of <6:2>: 0 (default) = the device selects receiver bandgap voltage automatically 1 = bits <6:2> define the receiver bandgap voltage

DCXO CONTROL (REG 1B – 1D)

Table 25:

Address	Bit(s)	Bit Name	Description
1B	<7>	Enable SPI control of DCXO tuning capacitance	Enables functionality of <5:0>: 0 (default) = the device selects DCXO tuning capacitance automatically 1 = tuning capacitance defined by <5:0>
	<6>	Enable SPI control of DCXO varactor	Enables functionality of <5:0>: 0 (default) = the device selects DCXO varactor automatically 1 = varactor defined by Register 1C<7:0> and 1D<7:3>
	<5:0>	DCXO tuning capacitor control	Higher binary values correspond to smaller total capacitance resulting in a higher operating frequency. Default is 00 0000.
1C	<7:0>	DCXO varactor control	Bits <12:5> of the 13-bit varactor control word.
1D	<7:3>	DCXO varactor control	Bits <4:0> of the 13-bit varactor control word. The default varactor control word is 0 0000 0000 0000.
	<2>	Enable frequency doubler	Select/bypass the DCXO frequency doubler: 0 (default) = bypassed 1 = selected
	<1>	DCXO bypass	Select/bypass the DCXO: 0 (default) = selected 1 = bypassed
	<0>	unused	

REFA FREQUENCY CONTROL (REG 1E – 25)

Table 26:

Address	Bit(s)	Bit Name	Description
1E	<7>	Enable SPI control of REFA SDM	Controls REFA frequency division functionality: 0 (default) = REFA frequency division defined by pins A3:0 1 = contents of Registers 1F – 25 define REFA frequency division via NA, MODA and FRACA.
	<6>	REFA SDM bypass	Controls bypassing of the REFA SDM: 0 (default) = allow integer-plus-fractional division 1 = allow only integer division
	<5>	REFA SDM enable	Controls REFA SDM enable and hold functionality: 0 = reset REFA SDM and stop its clocks 1 (default) = REFA SDM enabled
	<4>	REFA enable	Controls REFA enable and power down functionality: 0 = power down REFA input receiver (ineffective unless Register 1A<1>=1) 1 (default) = normal operation
	<3>	unused	
	<2>	REF SDM PRBS disable	Controls the PRBS generator for both the REFA and REFB SDMs: 0 (default) = PRBS enabled 1 = PRBS disabled
	<1:0>	19.44 MHz Input Mode Divider Select	Selects the divider value when the 19.44 MHz input mode is in effect: 00 (default) = 1 01 = 1 10 = 2 11 = 4 These bits are ineffective unless pins A3:0=1111 or B3:0=1111.
1F	<7:0>	FRACA	Bits <19:12> of the 20-bit fractional part of the REFA SDM.
20	<7:0>	FRACA	Bits <11:4> of the 20-bit fractional part of the REFA SDM.
21	<7:4>	FRACA	Bits <3:0> of the 20-bit fractional part of the REFA SDM. Default is FRACA = 0100 0000 0000 0000 0000 (262,144). NOTE: FRACA assumes twos-complement format.
	<3:0>	unused	
22	<7:2>	NA	6-bit integer divide value for the REFA SDM. Default divide value is 8.
	<1:0>	unused	
23	<7>	unused	This bit must be programmed to 0 (even though the default value is 1).
	<6:0>	MODA	Bits <18:12> of the 19-bit modulus of the REFA SDM.
24	<7:0>	MODA	Bits <11:4> of the 19-bit modulus of the REFA SDM.
25	<7:4>	MODA	Bits <3:0> of the 19-bit modulus of the REFA SDM. Default is MODA = 000 0000 0000 0000 0000.
	<3:0>	unused	

REFB FREQUENCY CONTROL (REG 26 – 2D)

Table 27:

Address	Bit(s)	Bit Name	Description
26	<7>	Enable SPI control of REFB SDM	Controls REFB frequency division functionality: 0 (default) = REFB frequency division defined by pins B3:0 1 = contents of Registers 1F – 25 define REFB frequency division via NB, MODB and FRACB.
	<6>	REFB SDM bypass	Controls bypassing of the REFB SDM: 0 (default) = allow integer-plus-fractional division 1 = allow only integer division
	<5>	REFB SDM enable	Controls REFB SDM enable and hold functionality: 0 = reset REFB SDM and stop its clocks 1 (default) = REFB SDM enabled

Address	Bit(s)	Bit Name	Description
	<4>	REFB enable	Controls REFB enable and power down functionality: 0 = power down REFB input receiver (ineffective unless Register 1A<1>=1) 1 (default) = normal operation
	<3:0>	unused	
27	<7:0>	FRACB	Bits <19:12> of the 20-bit fractional part of the REFB SDM.
28	<7:0>	FRACB	Bits <11:4> of the 20-bit fractional part of the REFB SDM.
29	<7:4>	FRACB	Bits <3:0> of the 20-bit fractional part of the REFB SDM. Default is FRACB = 0100 0000 0000 0000 0000 (262,144). NOTE: FRACB assumes twos-complement format.
	<3:0>	unused	
2A	<7:2>	NB	6-bit integer divide value for the REFB SDM. Default divide value is 8.
	<1:0>	unused	
2B	<7>	unused	This bit must be programmed to 0 (even though the default value is 1).
	<6:0>	MODB	Bits <18:12> of the 19-bit modulus of the REFB SDM.
2C	<7:0>	MODB	Bits <11:4> of the 19-bit modulus of the REFB SDM.
2D	<7:4>	MODB	Bits <3:0> of the 19-bit modulus of the REFB SDM. Default is MODB = 000 0000 0000 0000 0000.
	<3:0>	unused	

REFA DELAY CONTROL (REG 2E – 2F)

Table 28:

Address	Bit(s)	Bit Name	Description
2E	<7>	Enable SPI control of REFA delay	Controls REFA delay functionality: 0 (default) = the device selects REFA delay automatically 1 = REFA delay defined by Registers 2E<6:0> and 2F<7:6>
	<6:0>	REFA delay control	Bits <8:2> of the 9-bit REFA delay word
2F	<7:6>	REFA delay control	Bits <1:0> of the 9-bit REFA delay word Default is 1 0000 0000. Delay granularity is ~150 ps.
	<5:0>	unused	

REFB DELAY CONTROL (REG 30 – 31)

Table 29:

Address	Bit(s)	Bit Name	Description
30	<7>	Enable SPI control of REFB delay	Controls REFB delay functionality: 0 (default) = the device selects REFB delay automatically 1 = REFB delay defined by Registers 30<6:0> and 31<7:6>
	<6:0>	REFB delay control	Bits <8:2> of the 9-bit REFB delay word
31	<7:6>	REFB delay control	Bits <1:0> of the 9-bit REFB delay word Default is 1 0000 0000. Delay granularity is ~150 ps.
	<5:0>	unused	

OUT1 DRIVER CONTROL (REG 32)

Table 30:

Address	Bit(s)	Bit Name	Description
32	<7>	OUT1 drive strength	Controls the output drive capability of the OUT1 driver: 0 = weak 1 (default) = strong
	<6>	OUT1 power down	Controls power down functionality of the OUT1 driver: 0 (default) = OUT1 active

Address	Bit(s)	Bit Name	Description
			1 = OUT1 powered down
	<5:3>	OUT1 mode control	OUT1 driver mode selection: 000 = CMOS – both pins active 001 = CMOS – positive pin active, negative pin tri-state 010 = CMOS – positive pin tri-state, negative pin active 011 = CMOS – both pins tri-state 100 = LVDS 101 (default) = LVPECL 110 = not used 111 = not used
	<2:1>	OUT1 CMOS polarity	Selects the polarity of the OUT1 pins in CMOS mode: 00 (default) = positive pin logic is true=1, false=0 / negative pin logic is true=0, false=1 01 = positive pin logic is true=1, false=0 / negative pin logic is true=1, false=0 10 = positive pin logic is true=0, false=1 / negative pin logic is true=0, false=1 11 = positive pin logic is true=0, false=1 / negative pin logic is true=1, false=0 These bits are ineffective unless <5:3> selects CMOS mode.
	<0>	Enable SPI control of OUT1 drive control	Controls OUT1 driver functionality: 0 (default) = OUT1 is LVDS or LVPECL per the OUTSEL pin 1 = OUT1 functionality defined by <7:1>

INPUT PLL CONTROL (REG 33)

Table 31:

Address	Bit(s)	Bit Name	Description
33	<7:6>	Input PLL bandwidth	Controls the configuration of the input PLL as given in Table 14
	<5:4>	Input PLL gain	Controls the gain of the input PLL
	<3>	Crystal bypass	
	<2:0>	unused	

OUT2 DRIVER CONTROL (REG 34)

Table 32:

Address	Bit(s)	Bit Name	Description
34	<7>	OUT2 drive strength	Controls the output drive capability of the OUT2 driver: 0 = weak 1 (default) = strong
	<6>	OUT2 power down	Controls power down functionality of the OUT2 driver: 0 (default) = OUT2 active 1 = OUT2 powered down
	<5:3>	OUT2 mode control	OUT2 driver mode selection: 000 = CMOS – both pins active 001 = CMOS – positive pin active, negative pin tri-state 010 = CMOS – positive pin tri-state, negative pin active 011 = CMOS – both pins tri-state 100 = LVDS 101 (default) = LVPECL 110 = not used 111 = not used
	<2:1>	OUT2 CMOS polarity	Selects the polarity of the OUT2 pins in CMOS mode: 00 (default) = positive pin logic is true=1, false=0 / negative pin logic is true=0, false=1 01 = positive pin logic is true=1, false=0 / negative pin logic is true=1, false=0

Address	Bit(s)	Bit Name	Description
			10 = positive pin logic is true=0, false=1 / negative pin logic is true=0, false=1 11 = positive pin logic is true=0, false=1 / negative pin logic is true=1, false=0 These bits are ineffective unless <5:3> selects CMOS mode.
	<0>	Enable SPI control of OUT2 drive control	Controls OUT2 driver functionality: 0 (default) = OUT2 is LVDS or LVPECL per the OUTSEL pin 1 = OUT2 functionality defined by <7:1>

OUTLINE DIMENSIONS

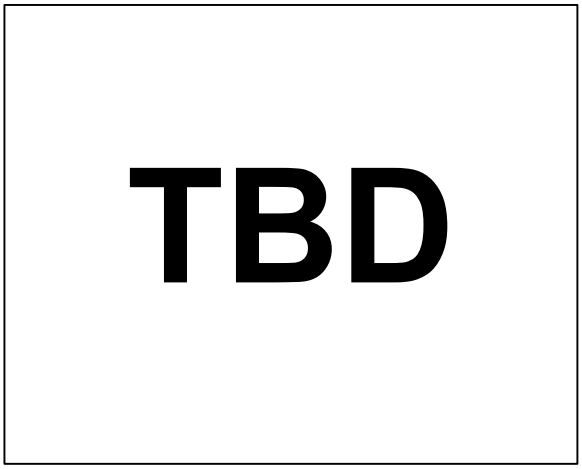


Figure 20: Outline Dimensions

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
		6x6 mm LFCSP Evaluation Board	

PR07805-0-9/08(PrJ)