16-Bit, 10 MHz Bandwidth, 30 MSPS to 160 MSPS Continuous Time Sigma-Delta ADC

Preliminary Technical Data

AD9261

FEATURES

SNR: 82.5 dB (84.5 dBFS)to 10 MHz input
SFDR: 87 dBc to 10 MHz input
Noise figure: 15dB
Input impedance: 1 kΩ
Power: 375 mW
1.8 V analog supply operation
1.8 V to 3.3 V output supply
Selectable bandwidth
2.5 MHz/5 MHz/10 MHz
Output data rate: 30 MSPS to 160 MSPS
Integrated decimation filters
Integrated sample rate converter
On-chip PLL clock multiplier
On-chip voltage reference
Offset binary, Gray code or twos complement data format
Serial control interface (SPI)

APPLICATIONS

Data Acquisition
Automated Test Equipment
Instrumentation
Medical Imaging

FUNCTIONAL BLOCK DIAGRAM

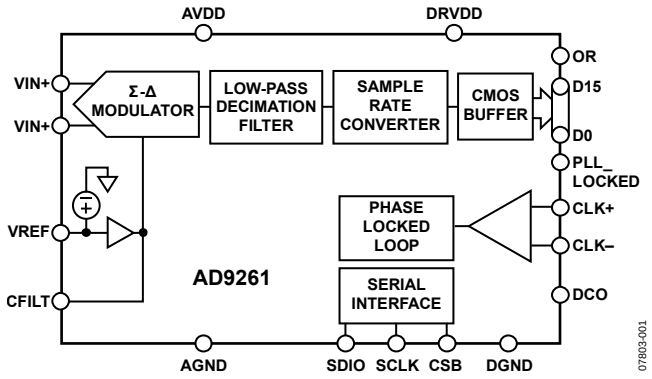

Figure 1.

GENERAL DESCRIPTION

The AD9261 is a 16-bit analog-to-digital converter (ADC) based on a continuous time sigma-delta (Σ-Δ) architecture that achieves 86 dB of dynamic range over a 10 MHz input bandwidth. The integrated features and characteristics unique to the continuous time Σ-Δ architecture significantly simplify its use and minimize the need for external components.

The AD9261 has a resistive input impedance that significantly relaxes the requirements of the driver amplifier. In addition, a 32× oversampled 5th-order continuous time loop filter significantly attenuates out of band signals and aliases, reducing the need for external filters at the input.

An external clock input or the integrated integer-N PLL provides the 640 MHz internal clock needed for the oversampled continuous time Σ-Δ modulator. On-chip decimation filters and sample rate converters reduce the modulator data rate from 640 MSPS to a user-defined output data rate between 30 MSPS to 160 MSPS, enabling a more efficient and direct interface.

The digital output data is presented in offset binary, Gray code, or twos complement format. A data clock output (DCO) is provided to ensure proper timing with the receiving logic.

The AD9261 operates on a 1.8 V analog supply and a 1.8 V to 3.3 V digital supply, consuming 375 mW. The AD9261 is available in a 48-lead LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Continuous time Σ-Δ architecture efficiently achieves high dynamic range and wide bandwidth.
2. Passive input structure reduces or eliminates the requirements for a driver amplifier.
3. An oversampling ratio of 32× and high order loop filter provide excellent alias rejection reducing or eliminating the need for antialiasing filters.
4. An integrated decimation filter, sample rate converter, PLL clock multiplier, and voltage reference provide ease of use.
5. Operates from a single 1.8 V analog power supply and 1.8 V to 3.3 V output supply.
6. A standard serial port interface (SPI) supports various product features and functions.

Rev. PrA

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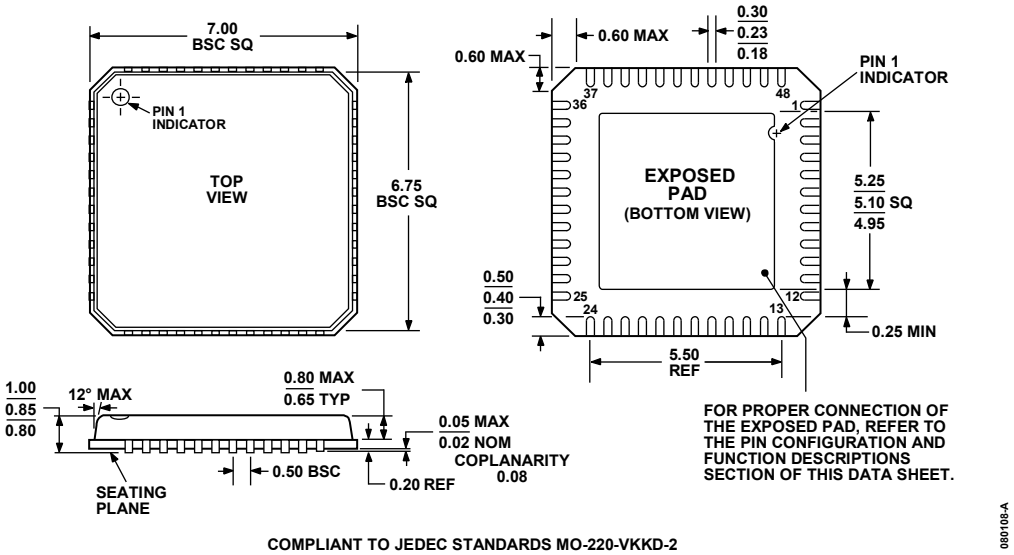
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 2. 48-Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad (CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9261BCPZ-10[1, 2]	–40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-48-1
AD9261-10EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] It is required that the exposed paddle be soldered to the AGND plane to achieve the best electrical and thermal performance.

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