3.3 V Upstream Cable Line Driver

AD8324

FEATURES

Supports DOCSIS 2.0 and Euro-DOCSIS standards for reverse path transmission systems
Gain programmable in 1 dB steps over a 59 dB range
Low distortion at 61 dBmV output:
–59 dBc SFDR at 21 MHz
–54 dBc SFDR at 65 MHz
Output noise level @ minimum gain 1.3 nV/√Hz
Maintains 75 Ω output impedance in TX-enable and Transmit-disable condition
Upper bandwidth: 100 MHz (full gain range)
3.3 V supply operation
Supports SPI® interfaces

APPLICATIONS

DOCSIS 2.0 and Euro-DOCSIS cable modems
CATV set-top boxes
CATV telephony modems
Coaxial and twisted pair line drivers

GENERAL DESCRIPTION

The AD8324[1] is a low cost amplifier designed for coaxial line driving. The features and specifications make the AD8324 ideally suited for DOCSIS 2.0 and Euro-DOCSIS applications. The gain of the AD8324 is digitally controlled. An 8-bit serial word determines the desired output gain over a 59 dB range, resulting in gain changes of 1 dB/LSB.

The AD8324 accepts a differential or single-ended input signal. The output is specified for driving a 75 Ω load through a 1:1 transformer.

Distortion performance of –54 dBc is achieved with an output level up to 61 dBmV at 65 MHz bandwidth.

This device has a sleep mode function that reduces the quiescent current to 30 μA and a full power-down function that reduces power-down current to 2.5 mA.

The AD8324 is packaged in a low cost 20-lead LFCSP package and a 20-lead QSOP package. The AD8324 operates from a single 3.3 V supply.

FUNCTIONAL BLOCK DIAGRAM

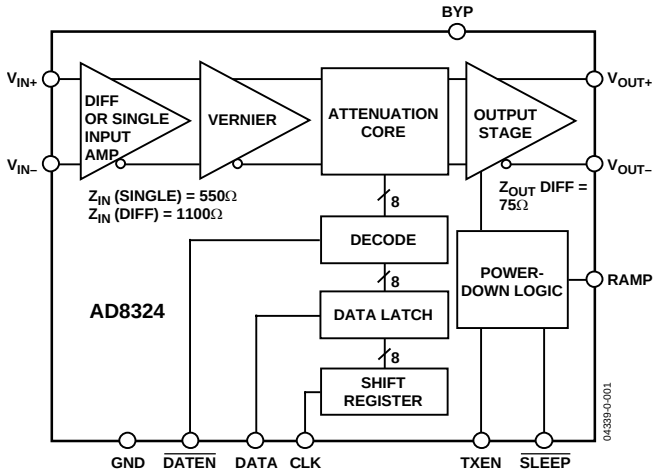

Figure 1. Functional Block Diagram

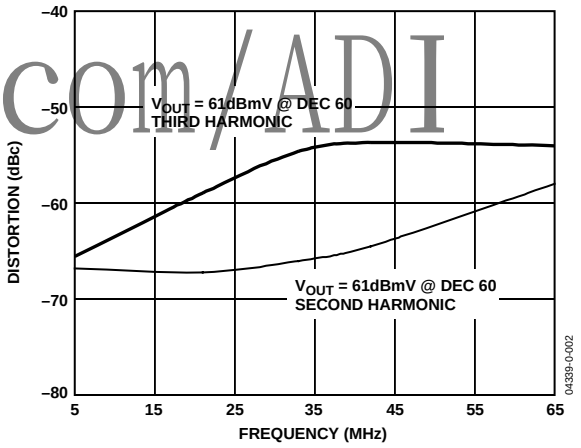

Figure 2. Worst Harmonic Distortion vs. Frequency

[1] Patent pending.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{CC} = 3.3 V, R_L = R_{IN} = 75 Ω, V_{IN} (Differential) = 27.5 dBmV, unless otherwise noted. The AD8324 is characterized using a 1:1 transformer[1] at the device output.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Specified AC Voltage	Output = 61 dBmV, Max Gain		27.5		dBmV
Input Resistance	Single-Ended Input		550		Ω
	Differential Input		1100		Ω
Input Capacitance			2		pF
GAIN CONTROL INTERFACE					
Voltage Gain Range		58	59.0	60	dB
Max Gain	Gain Code = 60 Dec	32.5	33.5	34.5	dB
Min Gain	Gain Code = 1 Dec	−26.5	−25.5	−24.5	dB
Output Step Size[2]		0.6	1.0	1.4	dB/LSB
Output Step Size Temperature Coefficient	T_A = −40°C to +85°C		±0.004		dB/°C
OUTPUT CHARACTERISTICS					
Bandwidth (−3 dB)	All Gain Codes (1–60 Decimal Codes)		100		MHz
Bandwidth Roll-Off	f = 65 MHz		1.7		dB
1 dB Compression Point[3]	Max Gain, f = 10 MHz, Output Referred	19.6	21		dBm
	Min Gain, f = 10 MHz, Input Referred	2.1	3.7		dBm
Output Noise[2]					
Max Gain	f = 10 MHz		157	166	nV/√Hz
Min Gain	f = 10 MHz		1.3	1.5	nV/√Hz
Transmit Disable	f = 10 MHz		1.1	1.2	nV/√Hz
Noise Figure[2]					
Max Gain	f = 10 MHz		15.5	16.0	dB
Differential Output Impedance	TX Enable and TX Disable		75 ± 30%[4]		Ω
OVERALL PERFORMANCE					
Second-Order Harmonic Distortion[5, 3]					
	f = 33 MHz, V_{OUT} = 61 dBmV @ Max Gain		−66	−60	dBc
	f = 65 MHz, V_{OUT} = 61 dBmV @ Max Gain		−58	−53	dBc
Third-Order Harmonic Distortion[5, 3]	f = 21 MHz, V_{OUT} = 61 dBmV @ Max Gain		−59	−57.5	dBc
	f = 65 MHz, V_{OUT} = 61 dBmV @ Max Gain		−54	−52.5	dBc
ACPR[2, 6]			−61	−58	dBc
Isolation (Transmit Disable)[2]	Max Gain, f = 65 MHz		−75	−70	dB
POWER CONTROL					
TX Enable Settling Time	Max Gain, V_{IN} = 0		2.5		µs
TX Disable Settling Time	Max Gain, V_{IN} = 0		3.8		µs
Output Switching Transients[3]	Equivalent Output = 31 dBmV		2.5	6	mV p-p
	Equivalent Output = 61 dBmV		27	71	mV p-p
Output Settling					
Due to Gain Change	Min to Max Gain		60		ns
Due to Input Step Change	Max Gain, V_{IN} = 27.5 dBmV		30		ns
POWER SUPPLY					
Operating Range		3.13	3.3	3.47	V
Quiescent Current	Max Gain	195	207	235	mA
	Min Gain	25	39	50	mA
	Transmit Disable (TXEN = 0)	1	2.5	4	mA
	$\overline{SLEEP}$ Mode (Power-Down)		30	500	µA
OPERATING TEMPERATURE RANGE	LFCSP	−40		+85	°C
	QSOP	−25		+70	°C

[1] TOKO 458PT-1556 used for above specifications. Typical insertion loss of 0.5 dB @ 10 MHz.
[2] Guaranteed by design and characterization to ±6 sigma for T_A = 25°C.
[3] Guaranteed by design and characterization to ±3 sigma for T_A = 25°C.
[4] Measured through a 1:1 transformer.
[5] Specification is worst case over all gain codes.
[6] V_{IN} = 27.5 dBmV, QPSK modulation, 160 kSPS symbol rate.

LOGIC INPUTS (TTL/CMOS COMPATIBLE LOGIC)

$\overline{\text{DATEN}}$, CLK, SDATA, TXEN, $\overline{\text{SLEEP}}$, V_{CC} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
Logic 1 Voltage	2.1		3.3	V
Logic 0 Voltage	0		0.8	V
Logic 1 Current (V_{INH} = 3.3 V), CLK, SDATA, $\overline{\text{DATEN}}$	0		20	nA
Logic 0 Current (V_{INL} = 0 V), CLK, SDATA, $\overline{\text{DATEN}}$	−600		−100	nA
Logic 1 Current (V_{INH} = 3.3 V), TXEN	50		190	µA
Logic 0 Current (V_{INL} = 0 V), TXEN	−250		−30	µA
Logic 1 Current (V_{INH} = 3.3 V), $\overline{\text{SLEEP}}$	50		190	µA
Logic 0 Current (V_{INL} = 0 V), $\overline{\text{SLEEP}}$	−250		−30	µA

TIMING REQUIREMENTS

V_{CC} = 3.3 V, $t_R = t_F$ = 4 ns, f_{CLK} = 8 MHz, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
Clock Pulse Width (t_{WH})	16.0			ns
Clock Period (t_C)	32.0			ns
Setup Time SDATA vs. Clock (t_{DS})	5.0			ns
Setup Time $\overline{\text{DATEN}}$ vs. Clock (t_{ES})	15.0			ns
Hold Time SDATA vs. Clock (t_{DH})	5.0			ns
Hold Time $\overline{\text{DATEN}}$ vs. Clock (t_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, $\overline{\text{DATEN}}$, Clock (t_R, t_F)			10	ns

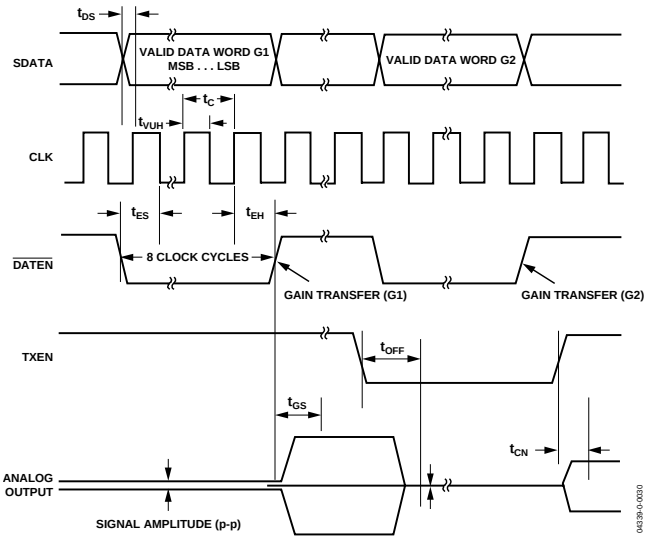


Figure 3. Serial Interface Timing

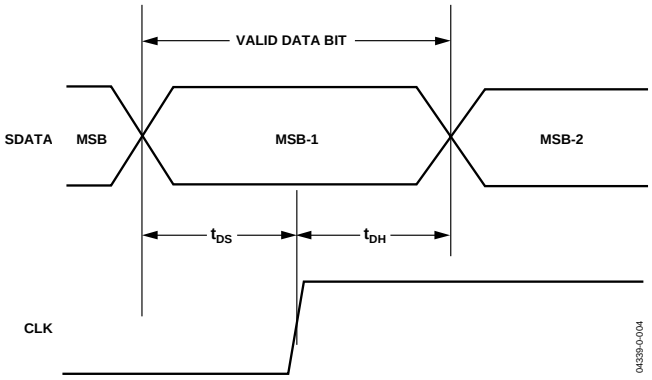


Figure 4. SDATA Timng

ABSOLUTE MAXIMUM RATINGS

Table 4. AD8324 Stress Ratings

Parameter	Rating
Supply Voltage V_{CC}	3.63 V
Input Voltage	
VIN+, VIN–	1.5 V p-p
$\overline{\text{DATEN}}$, SDATA, CLK, $\overline{\text{SLEEP}}$, TXEN	–0.5 V to +3.63 V
Internal Power Dissipation	
QSOP, LFCSP	776 mW
Operating Temperature Range	
LFCSP	–40°C to +85°C
QSOP	–25°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 5. Thermal Resistance Ratings

Model	θ_{JA}	Unit
AD8324JRQ	83.2[1]	°C/W
AD8324ACP	30.4[2]	°C/W

[1] Thermal resistance measured on SEMI standard 4-layer board.
[2] Thermal resistance measured on SEMI standard 4-layer board, paddle soldered to board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS

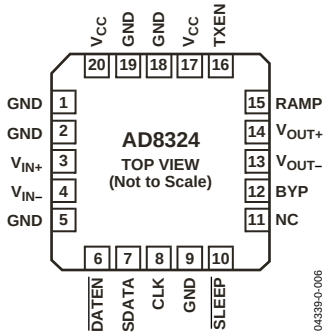


Figure 5. 20-Lead LFCSP

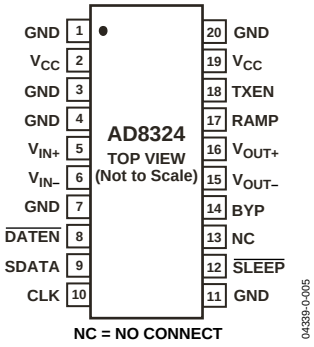


Figure 6. 20-Lead QSOP

Table 6. Pin Function Descriptions

Pin No. 20-Lead LFCSP	Pin No. 20-Lead QSOP	Mnemonic	Description
1, 2, 5, 9, 18, 19	1, 3, 4, 7, 11, 20	GND	Common External Ground Reference.
17, 20	2, 19	V_{CC}	Common Positive External Supply Voltage.
3	5	V_{IN+}	Noninverting Input. DC-biased to approximately $V_{CC}/2$. Should be ac-coupled with a 0.1 µF capacitor.
4	6	V_{IN-}	Inverting Input. DC-biased to approximately $V_{CC}/2$. Should be ac-coupled with a 0.1 µF capacitor.
6	8	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0-to-1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A 1-to-0 transition inhibits the data latch (holds the previous and simultaneously enables the register for serial data load).
7	9	SDATA	Serial Data Input. This digital input allows an 8-bit serial (gain) word to be loaded into the internal register with the MSB (most significant bit) first.
8	10	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave shift register. Logic 0-to-1 transition latches the data bit, and a 1-to-0 transfers the data bit to the slave. This requires the input serial data-word to be valid at or before this clock transition.
10	12	$\overline{\text{SLEEP}}$	Low Power Sleep Mode. In the sleep mode, the AD8324's supply current is reduced to 30 µA. A Logic 0 powers down the part (high Z_{OUT} state), and a Logic 1 powers up the part.
12	14	BYP	Internal Bypass. This pin must be externally decoupled (0.1 µF capacitor).
13	15	V_{OUT-}	Negative Output Signal. Must be biased to V_{CC}. See Figure 23.
14	16	V_{OUT+}	Positive Output Signal. Must be biased to V_{CC}. See Figure 23.
15	17	RAMP	External RAMP Capacitor (Optional).
16	18	TXEN	Logic 0 disables forward transmission. Logic 1 enables forward transmission.

TYPICAL PERFORMANCE CHARACTERISTICS

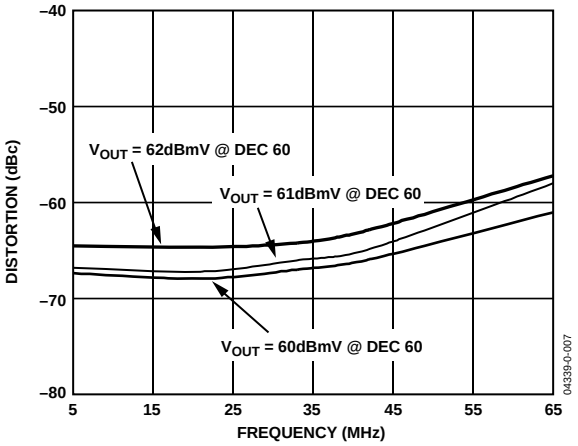


Figure 7. Second-Order Harmonic Distortion vs. Frequency for Various Output Powers

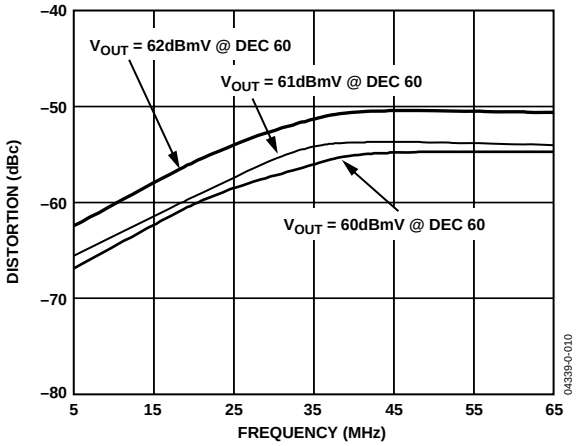


Figure 10. Third-Order Harmonic Distortion vs. Frequency for Various Output Powers

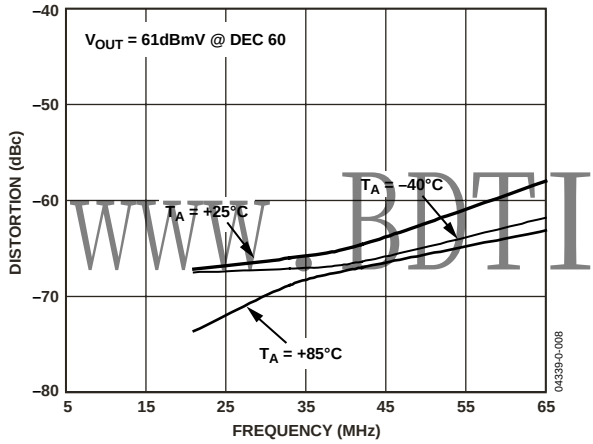


Figure 8. LFSCP Second-Order Harmonic Distortion vs. Frequency vs. Temperature

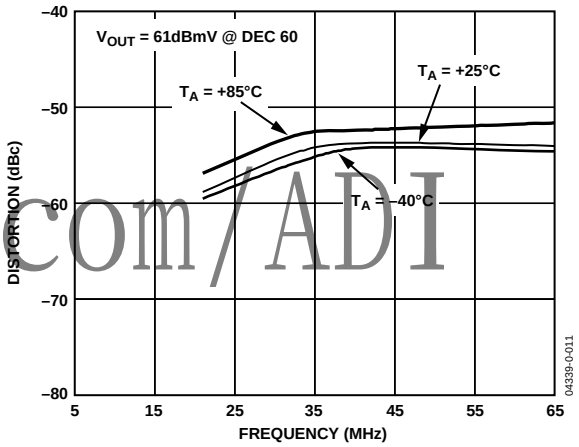


Figure 11. LFCSP Third-Order Harmonic Distortion vs. Frequency vs. Temperature

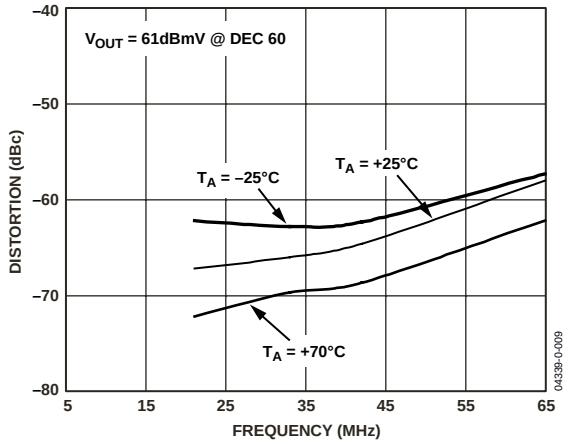


Figure 9. QSOP Second-Order Harmonic Distortion vs. Frequency vs. Temperature

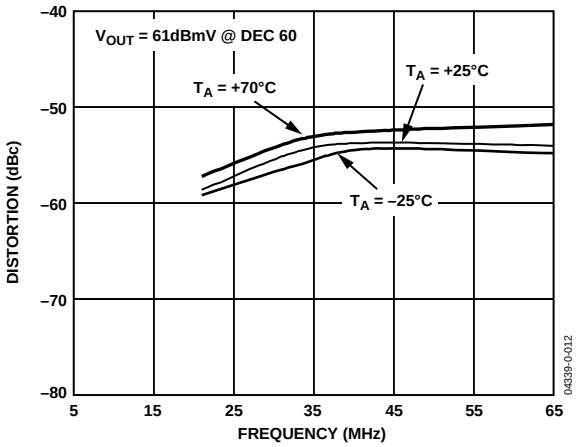


Figure 12. QSOP Third-Order Harmonic Distortion vs. Frequency vs. Temperature

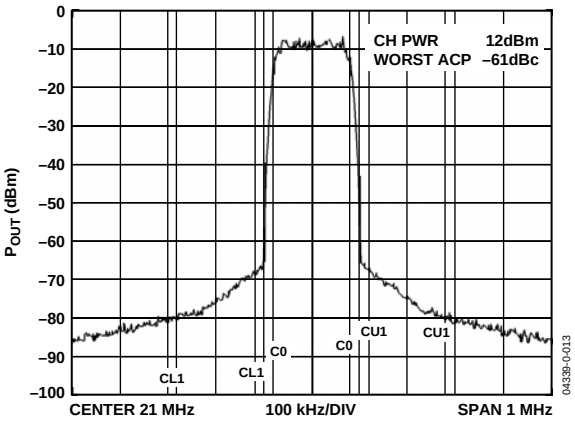


Figure 13. Adjacent Channel Power

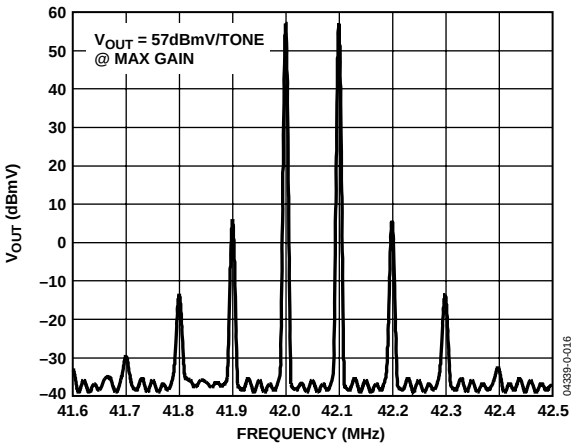


Figure 16. Two-Tone Intermodulation Distortion

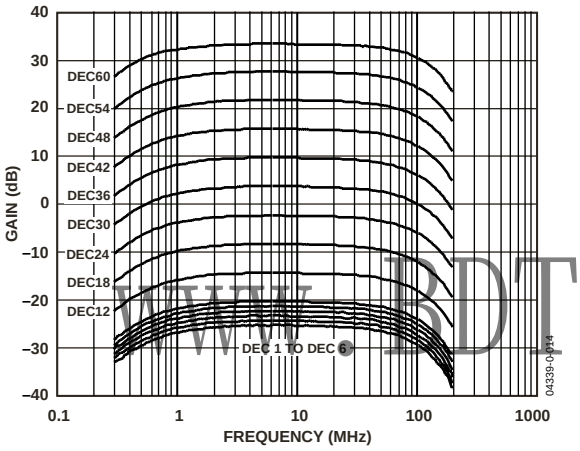


Figure 14. AC Response

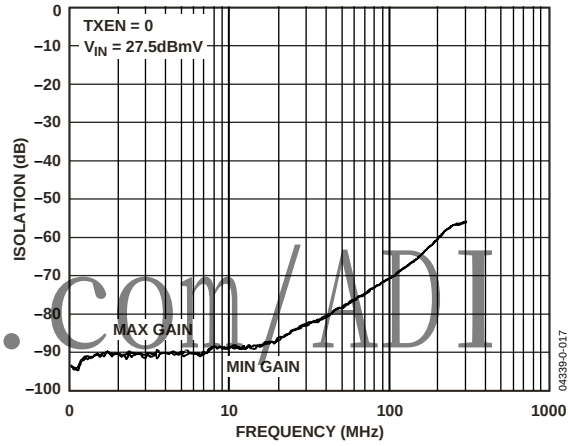


Figure 17. Isolation in Transmit Disable Mode vs. Frequency

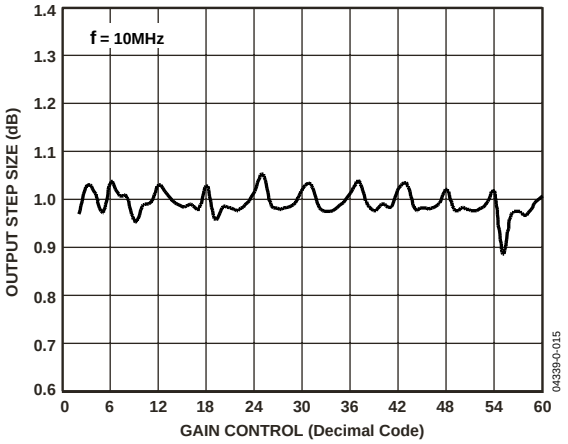


Figure 15. Output Step Size vs. Gain Control

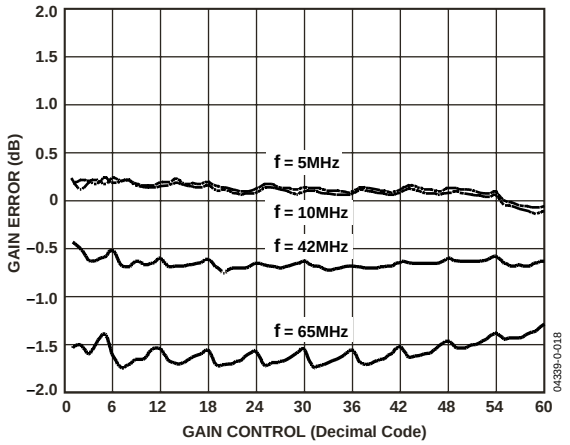


Figure 18. Gain Error vs. Gain Control

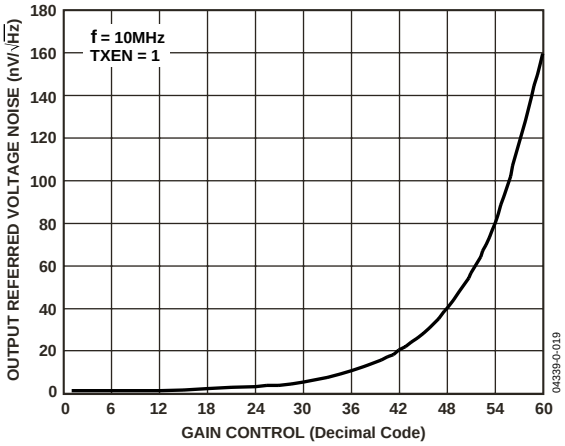


Figure 19. Output Referred Voltage Noise vs. Gain Control

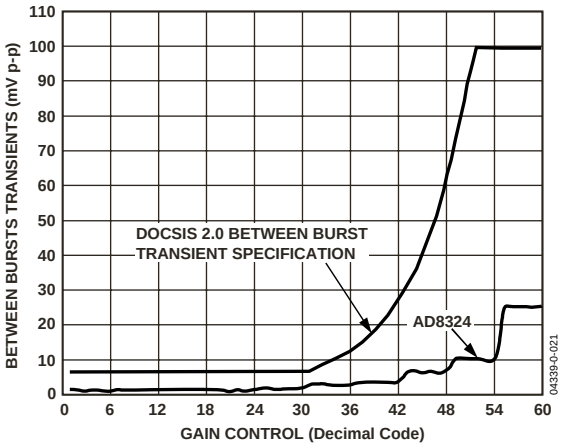


Figure 21. Between Burst Transient vs. Gain Control

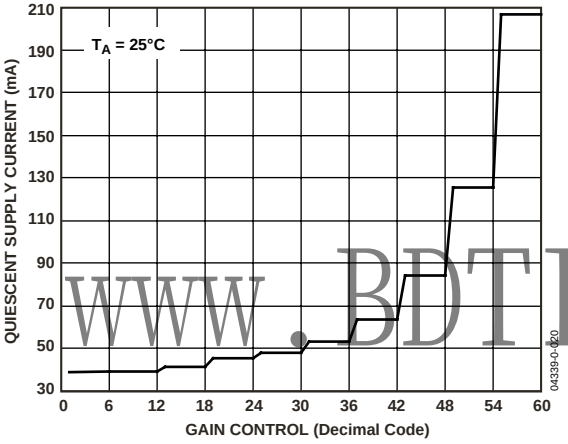


Figure 20. Supply Current vs. Gain Control

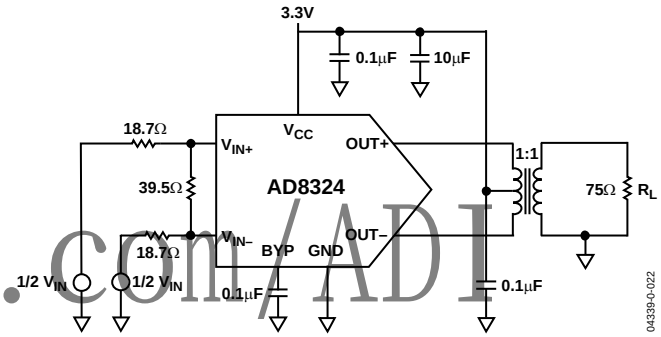


Figure 22. Typical Characterization Circuit

APPLICATIONS

GENERAL APPLICATIONS

The AD8324 is primarily intended for use as the upstream power amplifier (PA) in DOCSIS (data over cable service interface specification) certified cable modems and CATV set-top boxes. The upstream signal is either a QPSK or QAM signal generated by a DSP, a dedicated QPSK/QAM modulator, or a DAC. In all cases, the signal must be low-pass filtered before being applied to the PA in order to filter out-of-band noise and higher order harmonics from the amplified signal.

Due to the varying distances between the cable modem and the head-end, the upstream PA must be capable of varying the output power by applying gain or attenuation. The ability to vary the output power of the AD8324 ensures that the signal from the cable modem will have the proper level once it arrives at the head-end. The upstream signal path commonly includes a diplexer and cable splitters. The AD8324 has been designed to overcome losses associated with these passive components in the upstream cable path.

CIRCUIT DESCRIPTION

The AD8324 is composed of three analog functions in the transmit-enable mode. The input amplifier (preamp) can be used in a single-ended or differential configuration. If the input is used in the differential configuration, the input signals should be 180 degrees out of phase and of equal amplitude. A vernier is used in the input stage for controlling the fine 1 dB gain steps. This stage then drives a DAC, which provides the bulk of the AD8324's attenuation. The signals in the preamp and DAC blocks are differential to improve the PSRR and linearity. A differential current is fed from the DAC into the output stage. The output stage maintains 75 Ω differential output impedance in all power modes.

GAIN PROGRAMMING FOR THE AD8324

The AD8324 features a serial peripheral interface (SPI) for programming the gain code settings. The SPI interface consists of three digital data lines: CLK, $\overline{\text{DATEN}}$, and SDATA. The $\overline{\text{DATEN}}$ pin should be held low while the AD8324 is being programmed. The SDATA pin accepts the serial data stream for programming the AD8324 gain code. The CLK pin accepts the clock signal to latch in the data from the SDATA line.

The AD8324 utilizes a 6-bit shift register for clocking in the data. The shift register is designed to be programmed MSB first. The timing interface for programming the AD8324 can be seen in Table 2, Table 3, Figure 3, and Figure 4. While the $\overline{\text{DATEN}}$ pin is held low, the serial bits on the SDATA line are shifted into the register on the rising edge of the CLK pin.

For existing software that uses 8-bits to program the cable driver, the 2 MSBs will be ignored. This allows the AD8324 to be compatible with some existing system designs.

The AD8324 recognizes gain codes 1 through 60 (all gain codes are in decimal, unless otherwise noted). When the AD8324 is programmed with 61 to 63, it will internally default to max gain (gain code 60). If the programmed gain code is above 63, the AD8324 will recognize only the 6 LSBs. For example, gain code 75 (01001011 binary) will be interpreted as gain code 11 (001011 binary) since the 2 MSBs are ignored.

The programming range of the AD8324 is from –25.5 dB (gain code 1) to +33.5 dB (gain code 60). The 60 dB gain range is linear with a 1 dB change in a 1 LSB change in gain code. Figure 15 illustrates the gain step size of the AD8324 versus gain code. The AD8324 was characterized with a differential input signal and a TOKO 458PT-1457 1:1 transformer at the output.

INPUT BIAS, IMPEDANCE, AND TERMINATION

The V_{IN+} and V_{IN-} inputs have a dc bias level of $V_{CC}/2$; therefore the input signal should be ac-coupled as seen in the typical application circuit (Figure 23). The differential input impedance of the AD8324 is approximately 1.1 kΩ, while the single-ended input is 550 Ω. The high input impedance of the AD8324 allows flexibility in termination and properly matching filter networks. The AD8324 will exhibit optimum performance when driven with a pure differential signal.

OUTPUT BIAS, IMPEDANCE, AND TERMINATION.

The output stage of the AD8324 requires a bias of 3.3 V. The 3.3 V power supply should be connected to the center tap of the output transformer. Also, the V_{CC} that is being applied to the center tap of the transformer should be decoupled as seen in the typical application circuit (Figure 23).

The output impedance of the AD8324 is 75 Ω, regardless of whether the amplifier is in transmit enable, transmit disable, or sleep mode. This, when combined with a 1:1 voltage ratio transformer, eliminates the need for external back termination resistors. If the output signal is being evaluated using standard 50 Ω test equipment, a minimum loss 75 Ω to 50 Ω pad must be used to provide the test circuit with the proper impedance match. The AD8324 evaluation board provides a convenient means to implement a matching attenuator. Soldering a 43.3 Ω resistor in the R15 placeholder and an 86.6 Ω resistor in the R16 place-holder will allow testing on a 50 Ω system. When using a matching attenuator, it should be noted that there will be 5.7 dB of power loss (7.5 dB voltage) through the network.

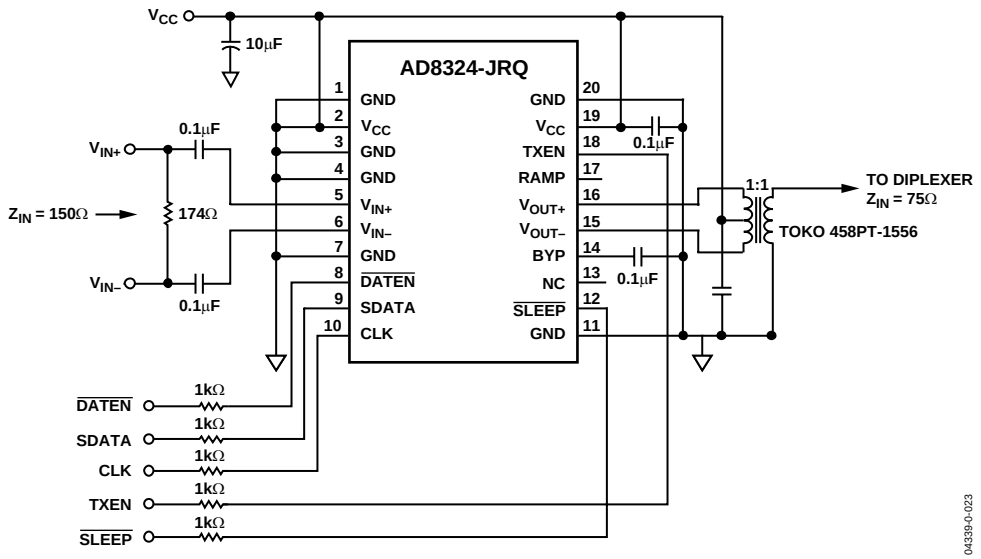


Figure 23. Typical Application Circuit

Table 7. Adjacent Channel Power

	Adjacent Channel Symbol Rate (kSym/s)					
Channel Symbol Rate (kSym/s)	**160**	**320**	**640**	**1280**	**2560**	**5120**
160	–63	–64	–68	–71	–72	–66
320	–63	–64	–66	–70	–72	–67
640	–64	–64	–65	–67	–71	–67
1280	–67	–65	–65	–66	–68	–67
2560	–70	–67	–66	–66	–67	–65
5120	–72	–70	–67	–67	–64	–64

POWER SUPPLY

The 3.3 V supply should be delivered to each of the V_{CC} pins via a low impedance power bus. This ensures that each pin is at the same potential. The power bus should be decoupled to ground using a 10 µF tantalum capacitor located close to the AD8324. In addition to the 10 µF capacitor, V_{CC} pins should be decoupled to ground with ceramic chip capacitors located close to the pins. The bypass pin, labeled BYP, should also be decoupled. The PCB should have a low impedance ground plane covering all unused portions of the board, except in areas of the board where input and output traces are in close proximity to the AD8324 and the output transformer. All AD8324 ground pins must be connected to the ground plane to ensure proper grounding of all internal nodes.

SIGNAL INTEGRITY LAYOUT CONSIDERATIONS

Careful attention to printed circuit board layout details will prevent problems due to board parasitics. Proper RF design techniques are mandatory. The differential input and output traces should be kept as short as possible. Keeping the traces short will minimize parasitic capacitance and inductance, which is most critical between the outputs of the AD8324 and the 1:1 output transformer. It is also critical that all differential signal paths be symmetrical in length and width. In addition, the input and output traces should be adequately spaced to minimize coupling (crosstalk) through the board. Following these guide-lines will optimize the overall performance of the AD8324 in all applications.

INITIAL POWER-UP

When the supply voltage is first applied to the AD8324, the gain of the amplifier is initially set to gain code 1. As power is first applied to the amplifier, the TXEN pin should be held low (Logic 0) to prevent forward signal transmission. After power has been applied to the amplifier, the gain can be set to the desired level by following the procedure provided in the Gain Programming for the AD8324 section. The TXEN pin can then be brought from Logic 0 to Logic 1, enabling forward signal transmission at the desired gain level.

RAMP PIN AND BYP PIN FEATURES

The RAMP pin (Pin 15) is used to control the length of the burst on and off transients. By default, leaving the RAMP pin unconnected will result in a transient that is fully compliant with DOCSIS 2.0 Section 6.2.21.2, Spurious Emissions During Burst On/Off Transients. DOCSIS requires that all between burst transients must be dissipated no faster than 2 µs. Adding capacitance to the RAMP pin will slow the dissipation even more.

The BYP pin is used to decouple the output stage to ground. Typically, for normal DOCSIS operation, the BYP pin should be decoupled to ground with a 0.1 µF capacitor. However, in applications that may require transient on/off times faster than 2 µs, smaller capacitors may be used, but it should be noted that the BYP pin should always be decoupled to ground.

POWER SAVING FEATURES

The AD8324 incorporates three distinct methods of reducing power consumption: transmit disable and sleep modes for between-burst and shutdown modes, as well as gain dependent quiescent current for transmit enable mode.

The asynchronous TXEN pin is used to place the AD8324 into between-burst mode. In this reduced current state, the 75 Ω output impedance is maintained. Applying Logic 0 to the TXEN pin deactivates the on-chip amplifier, providing a 98.8% reduction in consumed power. For 3.3 V operation, the supply current is typically reduced from 207 mA to 2.5 mA. In this mode of operation, between-burst noise is minimized and high input to output isolation is achieved. In addition to the TXEN pin, the AD8324 also incorporates an asynchronous $\overline{\text{SLEEP}}$ pin, which may be used to further reduce the supply current to approximately 30 µA. Applying Logic 0 to the $\overline{\text{SLEEP}}$ pin places the amplifier into $\overline{\text{SLEEP}}$ mode. Transitioning into or out of $\overline{\text{SLEEP}}$ mode may result in a transient voltage at the output of the amplifier.

In addition to the sleep and transmit disable functions, the AD8324 provides yet another means of reducing system power consumption. While in the transmit enable state, the AD8324 incorporates supply current scaling, which allows for lower power consumption at lower gain codes. Figure 20 shows the typical relationship between supply current and gain code.

DISTORTION, ADJACENT CHANNEL POWER, AND DOCSIS

To deliver the DOCSIS required 58 dBmV of QPSK signal and 55 dBmV of 16 QAM signal, the PA is required to deliver up to 61 dBmV. This added power is required to compensate for losses associated with the diplex filter or other passive components that may be included in the upstream path of cable modems or set-top boxes. It should be noted that the AD8324 was characterized with a differential input signal. Figures 7 to 10 show the AD8324 second and third harmonic distortion performance versus the fundamental frequency for various output power levels. These figures are useful for determining the in-band harmonic levels from 5 MHz to 65 MHz. Harmonics higher in frequency (above 42 MHz for DOCSIS and above 65 MHz for Euro-DOCSIS) will be sharply attenuated by the low-pass filter function of the diplexer.

Another measure of signal integrity is adjacent channel power, commonly referred to as ACP. DOCSIS 2.0, section 6.2.21.1.1 states, "Spurious emissions from a transmitted carrier may occur in an adjacent channel that could be occupied by a carrier of the same or different symbol rates." Figure 13 shows the typical ACP for a 61 dBmV (approximately 12 dBm) QPSK signal taken at the output of the AD8324 evaluation board. The transmit channel width and adjacent channel width in Figure 13 correspond to the symbol rates of 160 kSym/s. Table 7 shows the ACP results for the AD8324 driving a QPSK, 61 dBmV signal for all conditions in DOCSIS Table 6-9, Adjacent Channel Spurious Emissions.

UTILIZING DIPLEX FILTERS

The AD8324 was designed to drive 61 dBmV without any external filtering and still meet DOCSIS spurious emissions and distortion requirements. However, in most upstream CATV applications, a diplex filter is used to separate the upstream and downstream signal paths from one another. The diplex filter does have insertion loss that the upstream driver needs to overcome, but it also provides a low-pass filter. The addition of this low-pass filter to the signal chain can greatly attenuate second harmonic products of channels above 21 MHz and third harmonic products of channels at or above 14 MHz up for diplexers with a 42 MHz upstream cutoff. Similar performance gains can be achieved using European-specified diplexers to filter second harmonics for channels above 33 MHz and third harmonics for channels above 22 MHz (65 MHz upstream cutoff). This filtering allows the AD8324 to drive up to 63 dBmV of QPSK (this level can vary by application and modulation type).

NOISE AND DOCSIS

At minimum gain, the AD8324 output noise spectral density is 1.3 nV/√Hz measured at 10 MHz. DOCSIS Table 6-10, Spurious Emissions in 5 MHz to 42 MHz, specifies the output noise for various symbol rates. The calculated noise power in dBmV for 160 kSym/s is

$$20 \times \log\left[\sqrt{(1.3\ nV/\sqrt{Hz})^2 \times 160\ kHz}\right] + 60 = -65.7\ dBmV$$

Comparing the computed noise power of –65.7 dBmV to the +8 dBmV signal yields –73.7 dBc, which meets the required level set forth in DOCSIS Table 6-10. As the AD8324 gain is increased above this minimum value, the output signal increases at a faster rate than the noise, resulting in a signal-to-noise ratio that improves with gain. In transmit disable mode, the output noise spectral density is 1.1 nV/√Hz, which results in –67 dBmV when computed over 160 kSym/s. The noise power was measured directly at the AD8324AR-EVAL's output.

EVALUATION BOARD FEATURES AND OPERATION

The AD8324 evaluation board and control software can be used to control the AD8324 upstream cable driver via the parallel port of a personal computer. A standard printer cable connected to the parallel port of the PC is used to feed all the necessary data to the AD8324 using the Windows® based control software. This package provides a means of controlling the gain and the power mode of the AD8324. With this evaluation kit, the AD8324 can be evaluated in either a single-ended or differential input configuration. A schematic of the evaluation board is provided in Figure 29.

DIFFERENTIAL SIGNAL SOURCE

Typical applications for the AD8324 use a differential input signal from a modulator or a DAC. Refer to Table 8 for common values of R4, or calculate other input configurations using the equation in Figure 24. This circuit configuration will give optimal distortion results due to the symmetric input signals. It should be noted that this is the configuration that was used to characterize the AD8324.

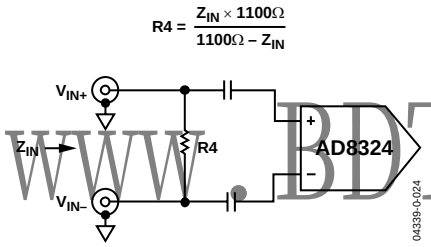


Figure 24. Differential Circuit

DIFFERENTIAL SIGNAL FROM SINGLE-ENDED SOURCE

The default configuration of the evaluation board implements a differential signal drive from a single-ended signal source. This configuration uses a 1:1 balun transformer to approximate a differential signal. Because of the non-ideal nature of real transformers, the differential signal is not purely equal and opposite in amplitude. Although this circuit slightly sacrifices even order harmonic distortion due to asymmetry, it does provide a convenient way to evaluate the AD8324 with a single-ended source. The AD8324 evaluation board is populated with a TOKO 617DB-A0070 1:1 for this purpose (T1).

Table 8 provides typical R4 values for common input configurations. R16 must be removed, and R2 and R3 should be shorted. Other input impedances may be calculated using the equation in Figure 25. Refer to Figure 29 for an evaluation board schematic. To use the transformer for converting a single ended source into a differential signal, the input signal must be applied to V_{IN+}.

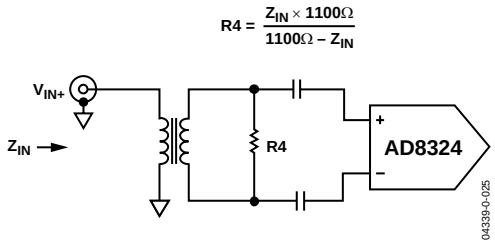


Figure 25. Single-to-Differential Circuit

SINGLE-ENDED SOURCE

Although the AD8324 was designed to have optimal DOCSIS performance when used with a differential input signal, the AD8324 may also be used as a single-ended receiver, or as an IF digitally controlled amplifier. However, as with the single-ended to differential configuration noted previously, even order harmonic distortion will be slightly degraded.

When operating the AD8324 in a single-ended input mode, terminate the part as illustrated in Figure 26. On the AD8324 evaluation boards, this termination method requires the removal and shorting of R2 and R3, the removal of R4, as well as the addition of 86.6 Ω at R1 and 40.2 Ω at R17 for 75 Ω termination. Table 8 shows the correct values for R11 and R12 for some common input configurations. Other input impedance configurations may be accommodated using the equations in Figure 26.

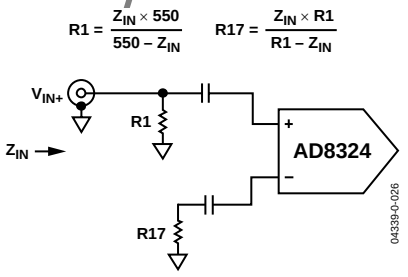


Figure 26. Single-Ended Circuit

Table 8. Common Matching Resistors

Differential Input Termination			
Z_{IN} (Ω)	**R2/R3 (Ω)**	**R4 (Ω)**	**R1/R17 (Ω)**
50	Open	52.3	Open/Open
75	Open	80.6	Open/Open
100	Open	110	Open/Open
150	Open	174	Open/Open
Single-Ended Input Termination			
Z_{IN} (Ω)	**R2/R3 (Ω)**	**R4 (Ω)**	**R1/R17 (Ω)**
50	0/0	Open	54.9/26.1
75	0/0	Open	86.6/40.2

OVERSHOOT ON PC PRINTER PORTS

The data lines on some PC parallel printer ports have excessive overshoot, which may cause communications problems when presented to the CLK pin of the AD8324. The evaluation board was designed to accommodate a series resistor and shunt capacitor (R9 and C5 in Figure 29) to filter the CLK signal if required. For parallel ports with logic levels above 3.3 V, R9 and C5 may be used as an attenuator.

INSTALLING VISUAL BASIC CONTROL SOFTWARE

Install the CabDrive_24 software by running the setup.exe file on disk one of the AD8324 evaluation software. Follow the on-screen directions and insert disk two when prompted. Choose the installation directory and then select the icon in the upper left to complete the installation.

RUNNING AD8324 SOFTWARE

To load the control software, go to START, PROGRAMS, CABDRIVE_24 or select the AD8324.exe file from the installed directory. Once loaded, select the proper parallel port to communicate with the AD8324 (Figure 27).

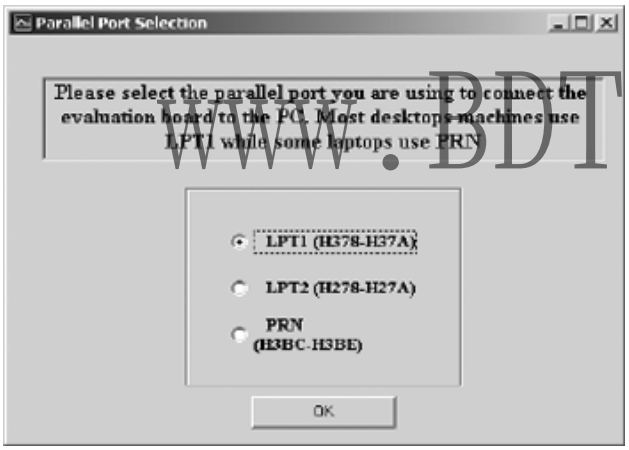


Figure 27. Parallel Port Selection

CONTROLLING GAIN/ATTENUATION OF THE AD8324

The slide bar controls the gain/attenuation of the AD8324, which is displayed in dB and in V/V. The gain scales 1 dB per LSB. The gain code from the position of the slide bar is displayed in decimal, binary, and hexadecimal (Figure 28).

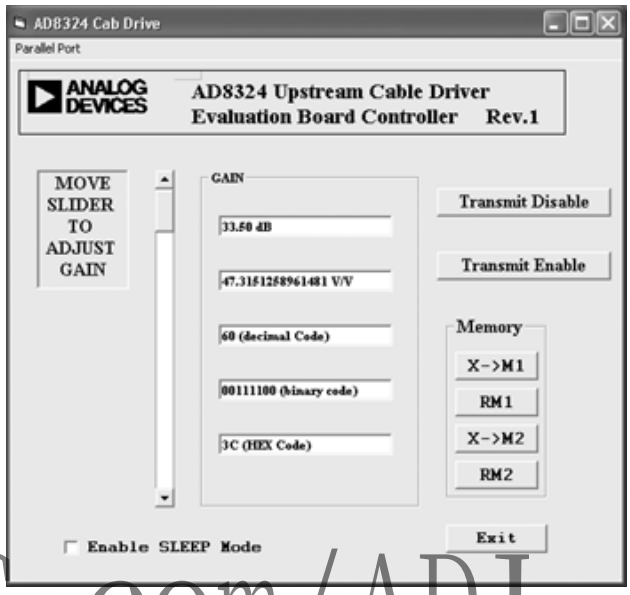


Figure 28. Control Software Interface

TRANSMIT ENABLE AND SLEEP MODE

The Transmit Enable and Transmit Disable buttons select the mode of operation of the AD8324 by asserting logic levels on the asynchronous TXEN pin. The Transmit Disable button applies Logic 0 to the TXEN pin, disabling forward transmission. The Transmit Enable button applies Logic 1 to the TXEN pin, enabling the AD8324 for forward transmission. Checking the Enable $\overline{\text{SLEEP}}$ Mode checkbox applies Logic 0 to the asynchronous $\overline{\text{SLEEP}}$ pin, setting the AD8324 for $\overline{\text{SLEEP}}$ mode.

MEMORY FUNCTIONS

The Memory section of the software provides a way to alternate between two gain settings. The X–>M1 button stores the current value of the gain slide bar into memory, while the RM1 button recalls the stored value, returning the gain slide bar to the stored level. The same applies to the X–>M2 and RM2 buttons.

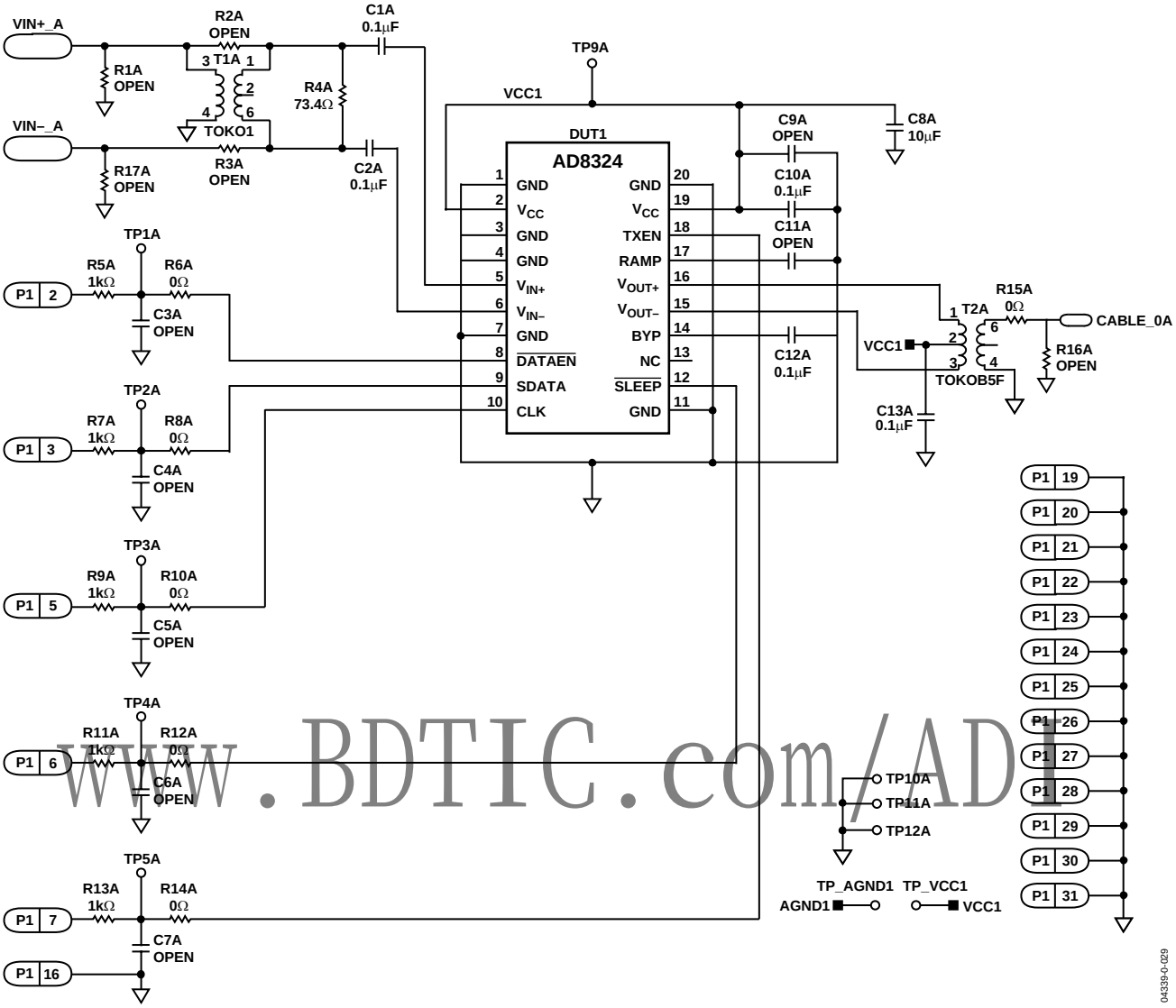
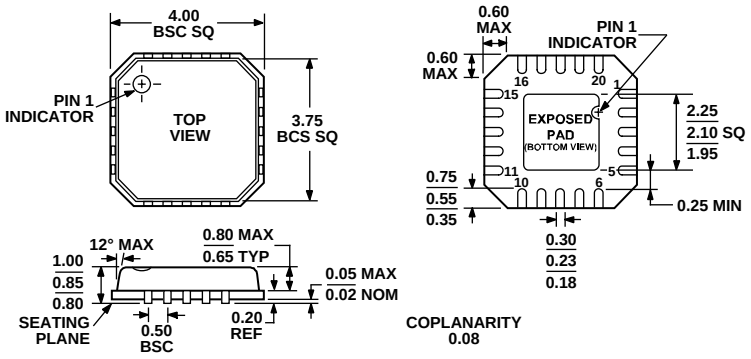


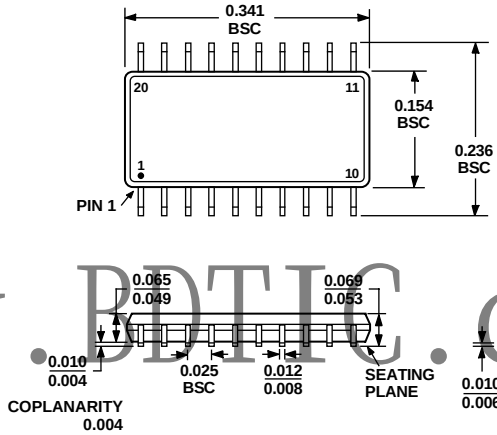
Figure 29. AD8324 Evaluation Board Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 30. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad (CP-20-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137-AD

Figure 31. 20-Lead Shrink Small Outline Package [QSOP] (RQ-20)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8324JRQ	–25°C to +70°C	20-Lead QSOP	RQ-20
AD8324JRQ-REEL	–25°C to +70°C	20-Lead QSOP	RQ-20
AD8324JRQ-REEL7	–25°C to +70°C	20-Lead QSOP	RQ-20
AD8324JRQZ[1]	–25°C to +70°C	20-Lead QSOP	RQ-20
AD8324JRQZ-REEL[1]	–25°C to +70°C	20-Lead QSOP	RQ-20
AD8324JRQZ-REEL7[1]	–25°C to +70°C	20-Lead QSOP	RQ-20
AD8324ACP	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8324ACP-REEL7	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8324ACPZ[1]	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8324ACPZ-REEL7[1]	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8324JRQ-EVAL		Evaluation Board	
AD8324ACP-EVAL		Evaluation Board	

[1] Z = Pb-free part.

C04339–0–7/05(A)