0.1 GHz to 2.5 GHz 70 dB Logarithmic Detector/Controller

AD8313

FEATURES

Wide bandwidth: 0.1 GHz to 2.5 GHz min
High dynamic range: 70 dB to ±3.0 dB
High accuracy: ±1.0 dB over 65 dB range (@ 1.9 GHz)
Fast response: 40 ns full-scale typical
Controller mode with error output
Scaling stable over supply and temperature
Wide supply range: 2.7 V to 5.5 V
Low power: 40 mW at 3 V
Power-down feature: 60 mW at 3 V
Complete and easy to use

APPLICATIONS

RF transmitter power amplifier setpoint control and level monitoring
Logarithmic amplifier for RSSI measurement cellular base stations, radio link, radar

FUNCTIONAL BLOCK DIAGRAM

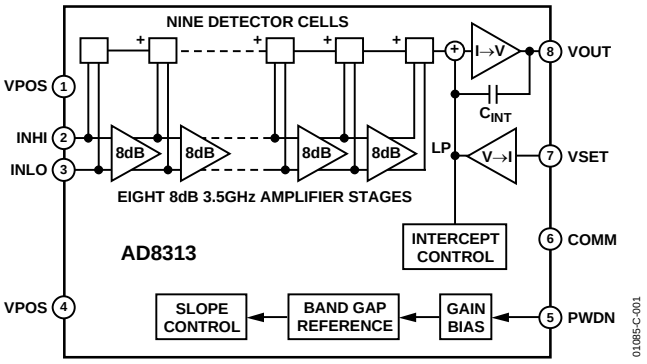

Figure 1.

GENERAL DESCRIPTION

The AD8313 is a complete multistage demodulating logarithmic amplifier that can accurately convert an RF signal at its differential input to an equivalent decibel-scaled value at its dc output. The AD8313 maintains a high degree of log conformance for signal frequencies from 0.1 GHz to 2.5 GHz and is useful over the range of 10 MHz to 3.5 GHz. The nominal input dynamic range is −65 dBm to 0 dBm (re: 50 Ω), and the sensitivity can be increased by 6 dB or more with a narrow-band input impedance matching network or a balun. Application is straightforward, requiring only a single supply of 2.7 V to 5.5 V and the addition of a suitable input and supply decoupling. Operating on a 3 V supply, its 13.7 mA consumption (for T_A = 25°C) is only 41 mW. A power-down feature is provided; the input is taken high to initiate a low current (20 μA) sleep mode, with a threshold at half the supply voltage.

The AD8313 uses a cascade of eight amplifier/limiter cells, each having a nominal gain of 8 dB and a −3 dB bandwidth of 3.5 GHz. This produces a total midband gain of 64 dB. At each amplifier output, a detector (rectifier) cell is used to convert the RF signal to baseband form; a ninth detector cell is placed directly at the input of the AD8313. The current-mode outputs of these cells are summed to generate a piecewise linear approximation to the logarithmic function. They are converted to a low impedance voltage-mode output by a transresistance stage, which also acts as a low-pass filter.

When used as a log amplifier, scaling is determined by a separate feedback interface (a transconductance stage) that sets the slope to approximately 18 mV/dB; used as a controller, this stage accepts the setpoint input. The logarithmic intercept is positioned to nearly −100 dBm, and the output runs from about 0.45 V dc at −73 dBm input to 1.75 V dc at 0 dBm input. The scale and intercept are supply- and temperature-stable.

The AD8313 is fabricated on Analog Devices' advanced 25 GHz silicon bipolar IC process and is available in an 8-lead MSOP package. The operating temperature range is −40°C to +85°C. An evaluation board is available.

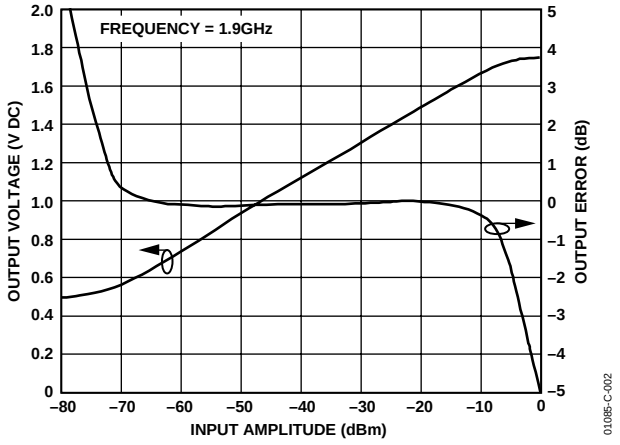

Figure 2. Typical Logarithmic Response and Error vs. Input Amplitude

Rev. D

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2/03—Data Sheet changed from Rev. B to Rev. C
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8/99—Data Sheet changed from Rev. A to Rev. B

5/99—Data Sheet changed from Rev. 0 to Rev. A

8/98—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 5 V[1], R_L 10 kΩ, unless otherwise noted.

Table 1.

Parameter	Conditions	Min[2]	Typ	Max[2]	Unit
SIGNAL INPUT INTERFACE					
Specified Frequency Range		0.1		2.5	GHz
DC Common-Mode Voltage			V_{POS} – 0.75		V
Input Bias Currents			10		μA
Input Impedance	f_{RF} < 100 MHz[3]		900||1.1		Ω||pF[4]
LOG (RSSI) MODE	Sinusoidal, input termination configuration shown in Figure 29				
100 MHz[5]	Nominal conditions				
±3 dB Dynamic Range[6]		53.5	65		dB
Range Center			–31.5		dBm
±1 dB Dynamic Range			56		dB
Slope		17	19	21	mV/dB
Intercept		–96	–88	–80	dBm
	2.7 V ≤ V_S ≤ 5.5 V, –40°C ≤ T ≤ +85°C				
±3 dB Dynamic Range		51	64		dB
Range Center			–31		dBm
±1 dB Dynamic Range			55		dB
Slope		16	19	22	mV/dB
Intercept		–99	–89	–75	dBm
Temperature Sensitivity	P_{IN} = –10 dBm		–0.022		dB/°C
900 MHz[5]	Nominal conditions				
±3 dB Dynamic Range		60	69		dB
Range Center			–32.5		dBm
±1 dB Dynamic Range			62		dB
Slope		15.5	18	20.5	mV/dB
Intercept		–105	–93	–81	dBm
	2.7 V ≤ V_S ≤ 5.5 V, –40°C ≤ T ≤ +85°C				
±3 dB Dynamic Range		55.5	68.5		dB
Range Center			–32.75		dBm
±1 dB Dynamic Range			61		dB
Slope		15	18	21	mV/dB
Intercept		–110	–95	–80	dBm
Temperature Sensitivity	P_{IN} = –10 dBm		–0.019		dB/°C
1.9 GHz[7]	Nominal conditions				
±3 dB Dynamic Range		52	73		dB
Range Center			–36.5		dBm
±1 dB Dynamic Range			62		dB
Slope		15	17.5	20.5	mV/dB
Intercept		–115	–100	–85	dBm
	2.7 V ≤ V_S ≤ 5.5 V, –40°C ≤ T ≤ +85°C				
±3 dB Dynamic Range		50	73		dB
Range Center			–36.5		dBm
±1 dB Dynamic Range			60		dB
Slope		14	17.5	21.5	mV/dB
Intercept		–125	–101	–78	dBm
Temperature Sensitivity	P_{IN} = –10 dBm		–0.019		dB/°C

Parameter	Conditions	Min[2]	Typ	Max[2]	Unit
2.5 GHz[7]	Nominal conditions				
±3 dB Dynamic Range		48	66		dB
Range Center			–34		dBm
±1 dB Dynamic Range			46		dB
Slope		16	20	25	mV/dB
Intercept		–111	–92	–72	dBm
	2.7 V ≤ V_S ≤ 5.5 V, –40°C ≤ T ≤ +85°C				
±3 dB Dynamic Range		47	68		dB
Range Center			–34.5		dBm
±1 dB Dynamic Range			46		dB
Slope		14.5	20	25	mV/dB
Intercept		–128	–92	–56	dBm
Temperature Sensitivity	P_{IN} =–10 dBm		–0.040		dB/°C
3.5 GHz[5]	Nominal conditions				
±3 dB Dynamic Range			43		dB
±1 dB Dynamic Range			35		dB
Slope			24		mV/dB
Intercept			–65		dBm
CONTROL MODE					
Controller Sensitivity	f = 900 MHz		23		V/dB
Low Frequency Gain	VSET to VOUT[8]		84		dB
Open-Loop Corner Frequency	VSET to VOUT[8]		700		Hz
Open-Loop Slew Rate	f = 900 MHz		2.5		V/µs
VSET Delay Time			150		ns
VOUT INTERFACE					
Current Drive Capability					
Source Current			400		µA
Sink Current			10		mA
Minimum Output Voltage	Open-loop		50		mV
Maximum Output Voltage	Open-loop		V_{POS} – 0.1		V
Output Noise Spectral Density	P_{IN} = –60 dBm, f_{SPOT} = 100 Hz		2.0		µV/√Hz
	P_{IN} = –60 dBm, f_{SPOT} = 10 MHz		1.3		µV/√Hz
Small Signal Response Time	P_{IN} = –60 dBm to –57 dBm, 10% to 90%		40	60	ns
Large Signal Response Time	P_{IN} = No signal to 0 dBm; settled to 0.5 dB		110	160	ns
VSET INTERFACE					
Input Voltage Range		0		V_{POS}	V
Input Impedance			18||1		kΩ||pF
POWER-DOWN INTERFACE					
PWDN Threshold			V_{POS}/2		V
Power-Up Response Time	Time delay following high to low transition until device meets full specifications.		1.8		µs
PWDN Input Bias Current	PWDN = 0 V		5		µA
	PWDN = V_S		<1		µA
POWER SUPPLY					
Operating Range		2.7		5.5	V
Powered-Up Current			13.7	15.5	mA
	4.5 V ≤V_S ≤ 5.5 V, –40°C ≤ T ≤ +85°C			18.5	mA
	2.7 V ≤V_S ≤ 3.3 V, –40°C ≤ T ≤ +85°C			18.5	mA
Powered-Down Current	4.5 V ≤V_S ≤ 5.5 V, –40°C ≤ T ≤ +85°C		50	150	µA
	2.7 V ≤V_S ≤ 3.3 V, –40°C ≤ T ≤ +85°C		20	50	µA

[1] Except where otherwise noted; performance at V_S = 3 V is equivalent to 5 V operation.
[2] Minimum and maximum specified limits on parameters that are guaranteed but not tested are 6 sigma values.
[3] Input impedance shown over frequency range in Figure 26.
[4] Double vertical bars (||) denote "in parallel with."
[5] Linear regression calculation for error curve taken from –40 dBm to –10 dBm for all parameters.
[6] Dynamic range refers to range over which the linearity error remains within the stated bound.
[7] Linear regression calculation for error curve taken from –60 dBm to –5 dBm for 3 dB dynamic range. All other regressions taken from –40 dBm to –10 dBm.
[8] AC response shown in Figure 12.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Supply Voltage V_S	5.5 V
VOUT, VSET, PWDN	0 V, VPOS
Input Power Differential (re: 50 Ω, 5.5 V)	25 dBm
Input Power Single-Ended (re: 50 Ω, 5.5 V)	19 dBm
Internal Power Dissipation	200 mW
θ_{JA}	200°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTION

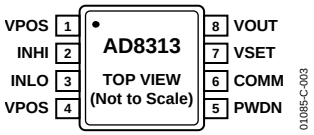

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	VPOS	Positive Supply Voltage (VPOS), 2.7 V to 5.5 V.
2	INHI	Noninverting Input. This input should be ac-coupled.
3	INLO	Inverting Input. This input should be ac-coupled.
5	PWDN	Connect Pin to Ground for Normal Operating Mode. Connect this pin to the supply for power-down mode.
6	COMM	Device Common.
7	VSET	Setpoint Input for Operation in Controller Mode. To operate in RSSI mode, short VSET and VOUT.
8	VOUT	Logarithmic/Error Output.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5 V, R_L input match shown in Figure 29, unless otherwise noted.

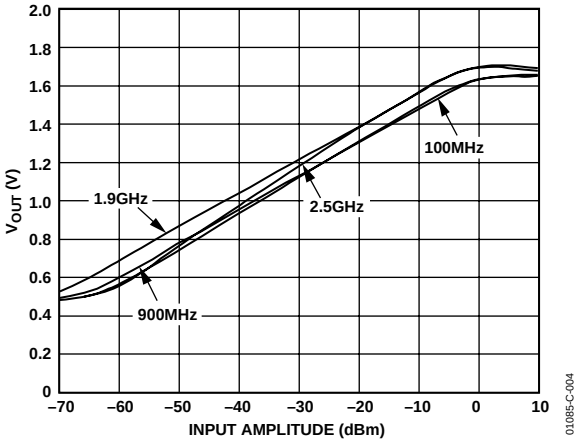

Figure 4. V_{OUT} vs. Input Amplitude

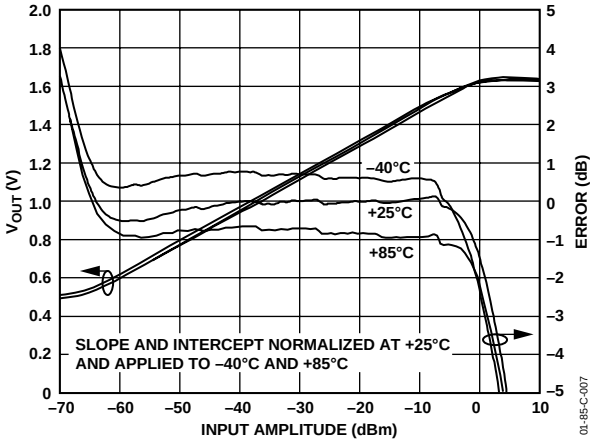

Figure 7. V_{OUT} and Log Conformance vs. Input Amplitude at 900 MHz for Multiple Temperatures

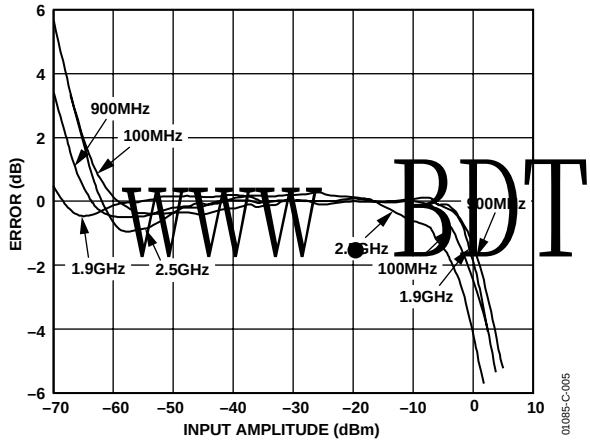

Figure 5. Log Conformance vs. Input Amplitude

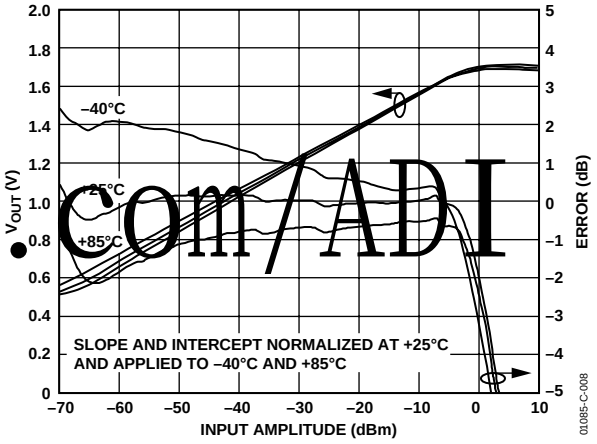

Figure 8. V_{OUT} and Log Conformance vs. Input Amplitude at 1.9 GHz for Multiple Temperatures

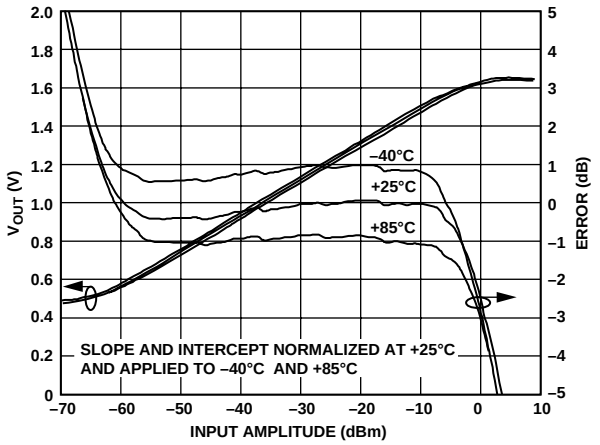

Figure 6. V_{OUT} and Log Conformance vs. Input Amplitude at 100 MHz for Multiple Temperatures

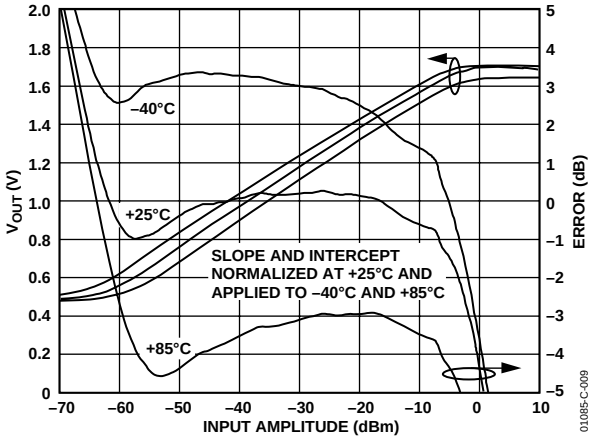

Figure 9. V_{OUT} and Log Conformance vs. Input Amplitude at 2.5 GHz for Multiple Temperatures

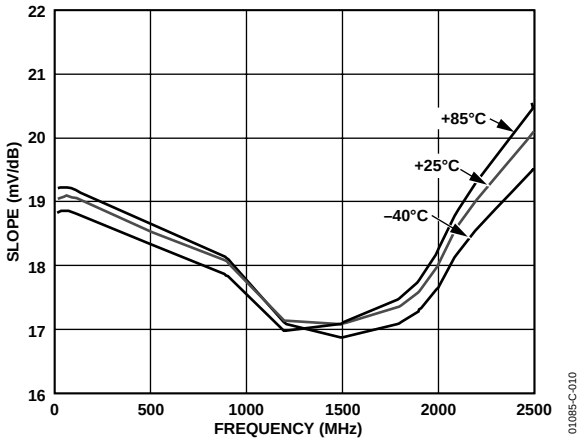

Figure 10. V_{OUT} Slope vs. Frequency for Multiple Temperatures

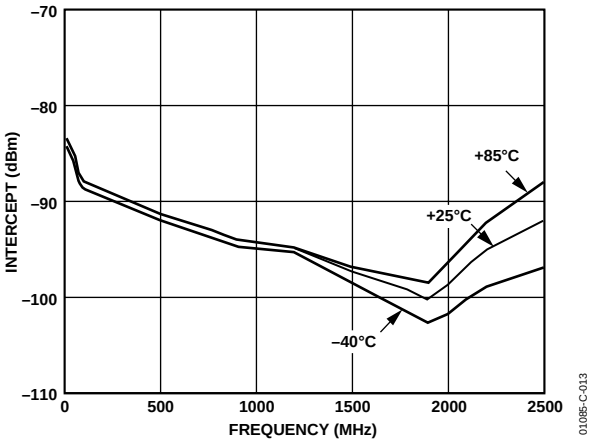

Figure 13. V_{OUT} Intercept vs. Frequency for Multiple Temperatures

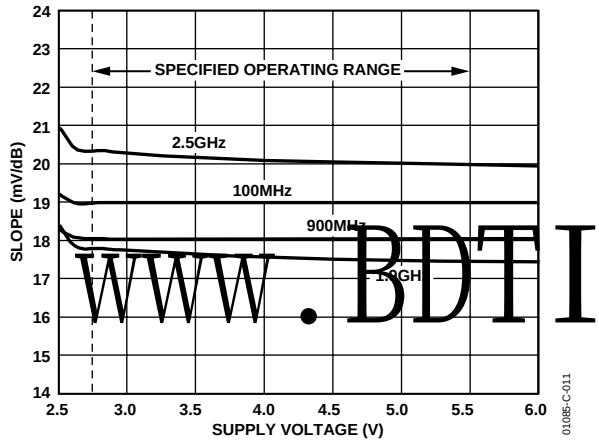

Figure 11. V_{OUT} Slope vs. Supply Voltage

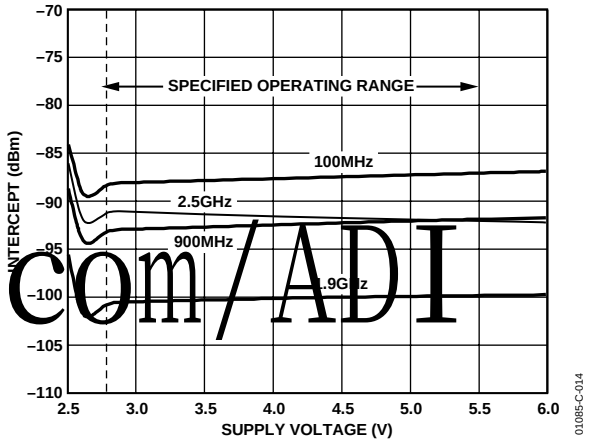

Figure 14. V_{OUT} Intercept vs. Supply Voltage

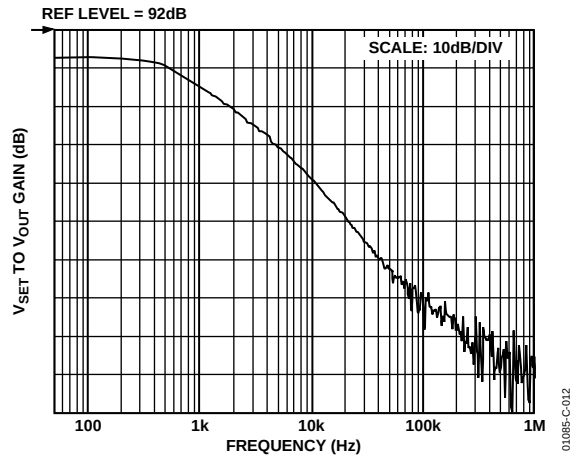

Figure 12. AC Response from V_{SET} to V_{OUT}

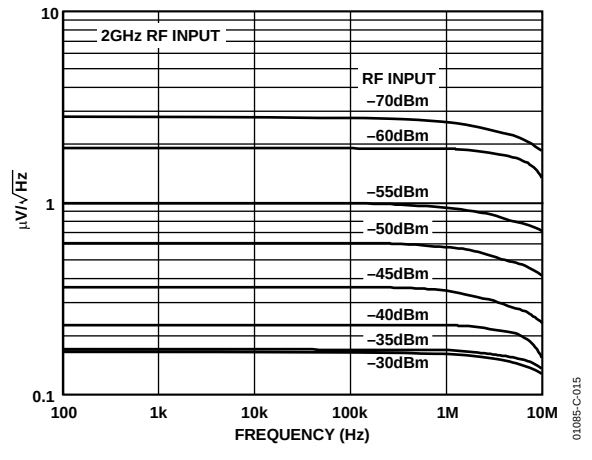

Figure 15. V_{OUT} Noise Spectral Density

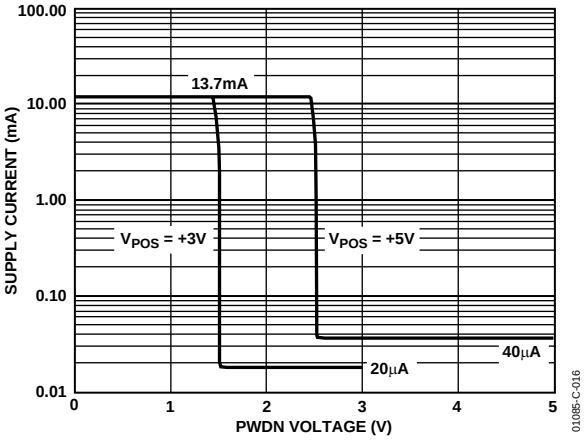

Figure 16. Typical Supply Current vs. PWDN Voltage

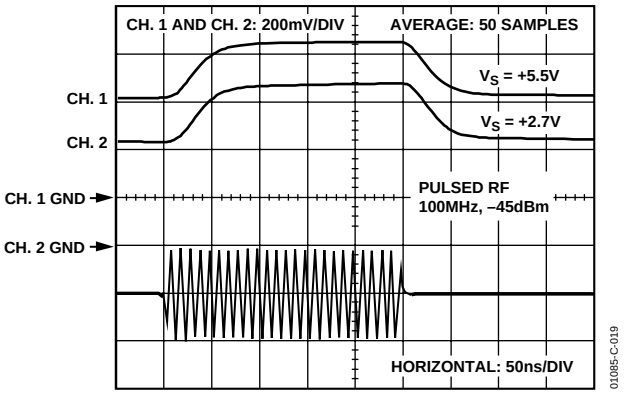

Figure 18. Response Time, No Signal to –45 dBm

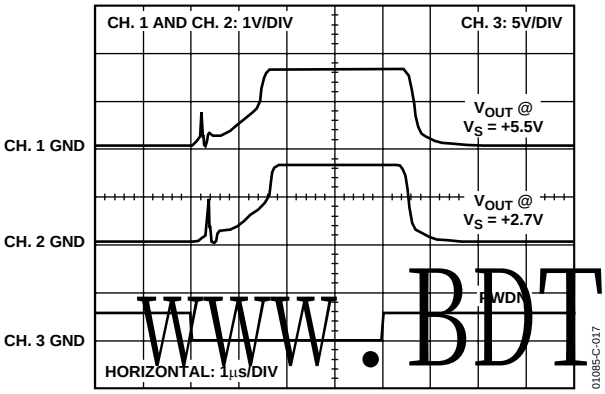

Figure 17. PWDN Response Time

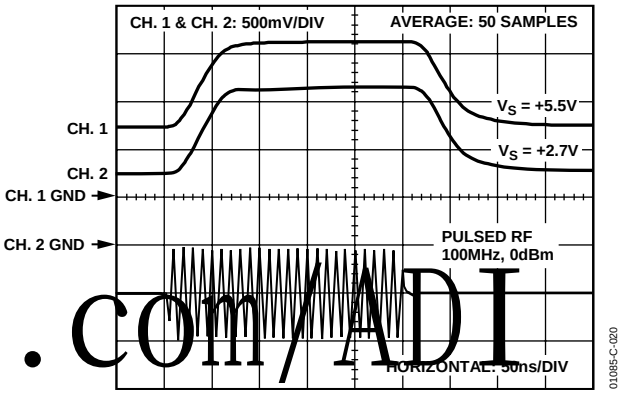

Figure 19. Response Time, No Signal to 0 dBm

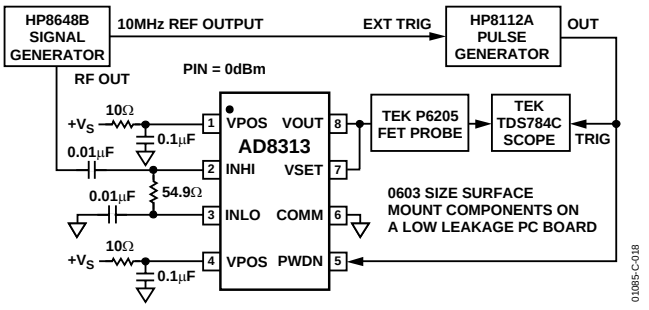

Figure 20. Test Setup for PWDN Response Time

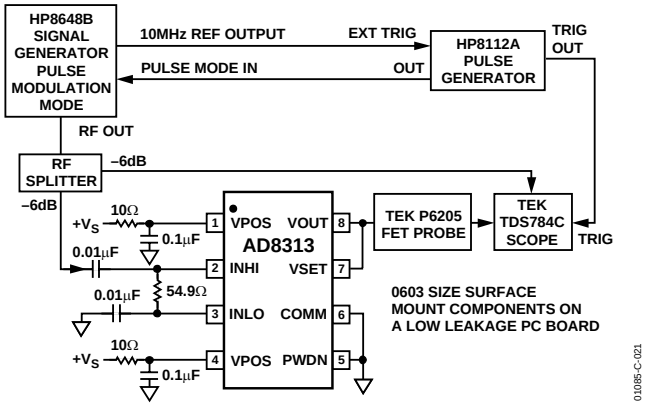

Figure 21. Test Setup for RSSI Mode Pulse Response

CIRCUIT DESCRIPTION

The AD8313 is an 8-stage logarithmic amplifier, specifically designed for use in RF measurement and power amplifier control applications at frequencies up to 2.5 GHz. A block diagram is shown in Figure 22. For a detailed description of log amp theory and design principles, refer to the AD8307 data sheet.

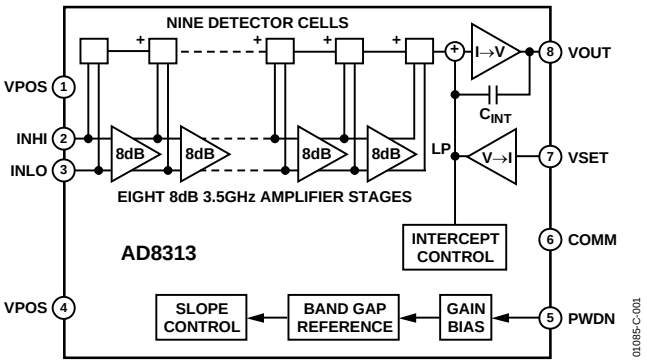

Figure 22. Block Diagram

A fully differential design is used. Inputs INHI and INLO (Pins 2 and 3) are internally biased to approximately 0.75 V below the supply voltage, and present a low frequency impedance of nominally 900 Ω in parallel with 1.1 pF. The noise spectral density referred to the input is 0.6 nV/√Hz, equivalent to a voltage of 35 V rms in a 3.5 GHz bandwidth, or a noise power of −76 dBm re: 50 Ω. This sets the lower limit to the dynamic range; the Applications section shows how to increase the sensitivity by using a matching network or input transformer. However, the low end accuracy of the AD8313 is enhanced by specially shaping the demodulation transfer characteristic to partially compensate for errors due to internal noise.

Each of the eight cascaded stages has a nominal voltage gain of 8 dB and a bandwidth of 3.5 GHz. Each stage is supported by precision biasing cells that determine this gain and stabilize it against supply and temperature variations. Since these stages are direct-coupled and the dc gain is high, an offset compensation loop is included. The first four stages and the biasing system are powered from Pin 4, while the later stages and the output interfaces are powered from Pin 1. The biasing is controlled by a logic interface PWDN (Pin 5); this is grounded for normal operation, but may be taken high (to V_S) to disable the chip. The threshold is at $V_{POS}/2$ and the biasing functions are enabled and disabled within 1.8 µs.

Each amplifier stage has a detector cell associated with its output. These nonlinear cells perform an absolute value (full-wave rectification) function on the differential voltages along this backbone in a transconductance fashion; their outputs are in current-mode form and are thus easily summed. A ninth detector cell is added at the input of the AD8313. Since the midrange response of each of these nine detector stages is separated by 8 dB, the overall dynamic range is about 72 dB (Figure 23). The upper end of this range is determined by the capacity of the first detector cell, and occurs at approximately 0 dBm. The practical dynamic range is over 70 dB to the ±3 dB error points. However, some erosion of this range can occur at temperature and frequency extremes. Useful operation to over 3 GHz is possible, and the AD8313 remains serviceable at 10 MHz, needing only a small amount of additional ripple filtering.

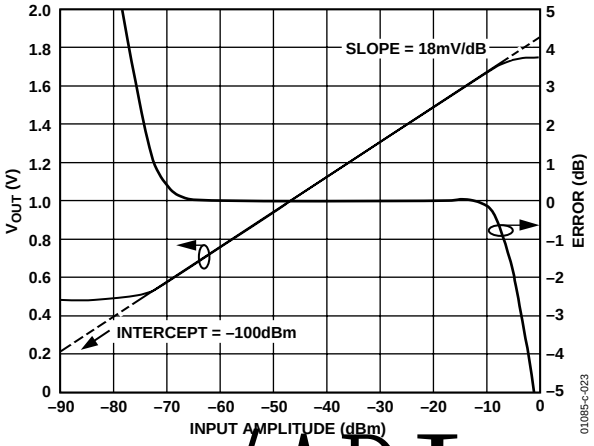

Figure 23. Typical VOUT Response and Error vs. Input Power at 1.9 GHz

The fluctuating current output generated by the detector cells, with a fundamental component at twice the signal frequency, is filtered first by a low-pass section inside each cell, and then by the output stage. The output stage converts these currents to a voltage, V_{OUT}, at VOUT (Pin 8), which can swing rail-to-rail. The filter exhibits a 2-pole response with a corner at approximately 12 MHz and full-scale rise time (10% to 90%) of 40 ns. The residual output ripple at an input frequency of 100 MHz has an amplitude of under 1 mV. The output can drive a small resistive load; it can source currents of up to 400 µA, and sink up to 10 mA. The output is stable with any capacitive load, though settling time could be impaired. The low frequency incremental output impedance is approximately 0.2 Ω.

In addition to its use as an RF power measurement device (that is, as a logarithmic amplifier), the AD8313 may also be used in controller applications by breaking the feedback path from VOUT to VSET (Pin 7), which determines the slope of the output (nominally 18 mV/dB). This pin becomes the setpoint input in controller modes. In this mode, the voltage V_{OUT} remains close to ground (typically under 50 mV) until the decibel equivalent of the voltage V_{SET} is reached at the input, when V_{OUT} makes a rapid transition to a voltage close to V_{POS} (see the Operating in Controller Mode section). The logarithmic intercept is nominally positioned at −100 dBm (re: 50 Ω); this is effective in both the log amp mode and the controller mode.

With Pins 7 and 8 connected (log amp mode), the output can be stated as

$$V_{OUT} = V_{SLOPE}\,(P_{IN} + 100\ \text{dBm})$$

where P_{IN} is the input power stated in dBm when the source is directly terminated in 50 Ω. However, the input impedance of the AD8313 is much higher than 50 Ω, and the sensitivity of this device may be increased by about 12 dB by using some type of matching network (see below), which adds a voltage gain and lowers the intercept by the same amount. Dependence on the reference impedance can be avoided by restating the expression as

$$V_{OUT} = 20 \times V_{SLOPE} \times \log \times (V_{IN} / 2.2\ \mu\text{V})$$

where V_{IN} is the rms value of a sinusoidal input appearing across Pins 2 and 3; here, 2.2 μV corresponds to the intercept, expressed in voltage terms. For detailed information on the effect of signal waveform and metrics on the intercept positioning for a log amp, refer to the AD8307 data sheet.

With Pins 7 and 8 disconnected (controller mode), the output can be stated as

$$V_{OUT} \to V_S \quad \text{when} \quad V_{SLOPE} \log (P_{IN} / 100) > V_{SET}$$

$$V_{OUT} \to 0 \quad \text{when} \quad V_{SLOPE} \log (P_{IN} / 100) < V_{SET}$$

when the input is stated in terms of the power of a sinusoidal signal across a net termination impedance of 50 Ω. The transition zone between high and low states is very narrow since the output stage behaves essentially as a fast integrator. The above equations can be restated as

$$V_{OUT} \to V_S \quad \text{when} \quad V_{SLOPE} \log (V_{IN} / 2.2\ \mu\text{V}) > V_{SET}$$

$$V_{OUT} \to 0 \quad \text{when} \quad V_{SLOPE} \log (V_{IN} / 2.2\ \mu\text{V}) < V_{SET}$$

Another use of the separate VOUT and VSET pins is in raising the load-driving current capability by including an external NPN emitter follower. More complete information about usage in these modes is provided in the Applications section.

INTERFACES

This section describes the signal and control interfaces and their behavior. On-chip resistances and capacitances exhibit variations of up to ±20%. These resistances are sometimes temperature-dependent, and the capacitances may be voltage-dependent.

POWER-DOWN INTERFACE, PWDN

The power-down threshold is accurately centered at the midpoint of the supply as shown in Figure 24. If Pin 5 is left unconnected or tied to the supply voltage (recommended), the bias enable current is shut off, and the current drawn from the supply is predominately through a nominal 300 kΩ chain (20 μA at 3 V). When grounded, the bias system is turned on. The threshold level is accurately at $V_{POS}/2$. When operating in the device ON state, the input bias current at the PWDN pin is approximately 5 μA for V_{POS} = 3 V.

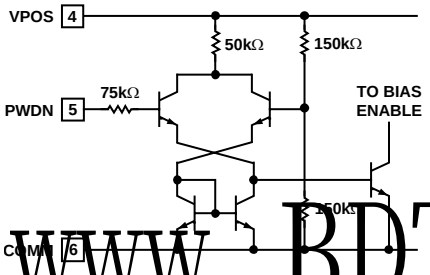

Figure 24. Power-Down Threshold Circuitry

SIGNAL INPUTS, INHI, INLO

The simplest low frequency ac model for this interface consists of just a 900 Ω resistance, R_{IN}, in shunt with a 1.1 pF input capacitance, C_{IN}, connected across INHI and INLO. Figure 25 shows these distributed in the context of a more complete schematic. The input bias voltage shown is for the enabled chip; when disabled, it rises by a few hundred millivolts. If the input is coupled via capacitors, this change may cause a low level signal transient to be introduced, having a time constant formed by these capacitors and R_{IN}. For this reason, large coupling capacitors should be well matched. This is not necessary when using the small capacitors found in many impedance transforming networks used at high frequencies.

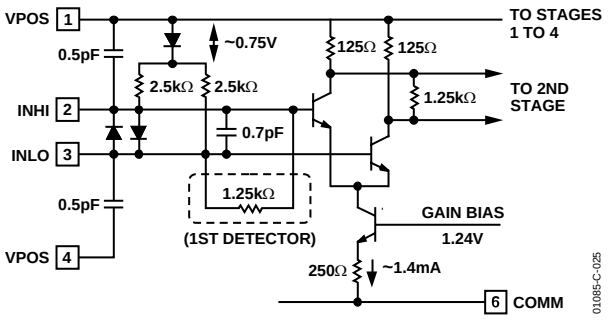

Figure 25. Input Interface Simplified Schematic

For high frequency use, Figure 26 shows the input impedance plotted on a Smith chart. This measured result of a typical device includes a 191 mil 50 Ω trace and a 680 pF capacitor to ground from the INLO pin.

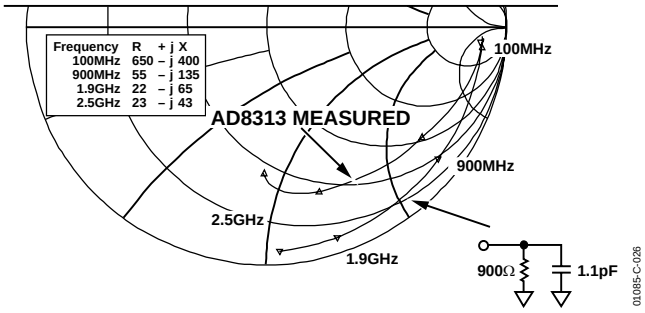

Figure 26. Typical Input Impedance

LOGARITHMIC/ERROR OUTPUT, VOUT

The rail-to-rail output interface is shown in Figure 27. V_{OUT} can run from within about 50 mV of ground, to within about 100 mV of the supply voltage, and is short-circuit safe to either supply. However, the sourcing load current, I_{SOURCE}, is limited to that which is provided by the PNP transistor, typically 400 μA. Larger load currents can be provided by adding an external NPN transistor (see the Applications section). The dc open-loop gain of this amplifier is high, and it may be regarded as an integrator having a capacitance of 2 pF (C_{INT}) driven by the current-mode signal generated by the summed outputs of the nine detector stages, which is scaled approximately 4.0 μA/dB.

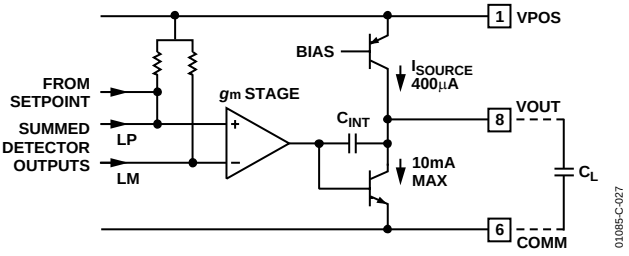

Figure 27. Output Interface Circuitry

Thus, for midscale RF input of about 3 mV, which is some 40 dB above the minimum detector output, this current is 160 μA, and the output changes by 8 V/μs. When VOUT is connected to VSET, the rise and fall times are approximately 40 ns (for $R_L \geq 10$ kΩ).

The nominal slew rate is 2.5 V/μs. The HF compensation technique results in stable operation with a large capacitive load, C_L, though the positive-going slew rate is then limited by I_{SOURCE}/C_L to 1 V/μs for C_L = 400 pF.

SETPOINT INTERFACE, VSET

The setpoint interface is shown in Figure 28. The voltage, V_{SET}, is divided by a factor of 3 in a resistive attenuator of 18 kΩ total resistance. The signal is converted to a current by the action of the op amp and the resistor R3 (1.5 kΩ), which balances the current generated by the summed output of the nine detector cells at the input to the previous cell. The logarithmic slope is nominally 3 µs × 4.0 µA/dB × 1.5 kΩ = 18 mV/dB.

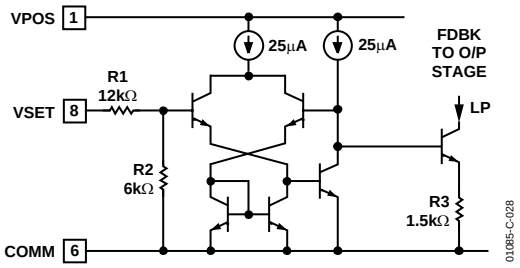

Figure 28. Setpoint Interface Circuitry

APPLICATIONS

BASIC CONNECTIONS FOR LOG (RSSI) MODE

Figure 29 shows the AD8313 connected in its basic measurement mode. A power supply between 2.7 V and 5.5 V is required. The power supply to each of the VPOS pins should be decoupled with a 0.1 μF surface-mount ceramic capacitor and a 10 Ω series resistor.

The PWDN pin is shown as grounded. The AD8313 may be disabled by a logic high at this pin. When disabled, the chip current is reduced to about 20 μA from its normal value of 13.7 mA. The logic threshold is at $V_{POS}/2$, and the enable function occurs in about 1.8 μs. However, that additional settling time is generally needed at low input levels. While the input in this case is terminated with a simple 50 Ω broadband resistive match, there are many ways in which the input termination can be accomplished. These are discussed in the Input Coupling section.

VSET is connected to VOUT to establish a feedback path that controls the overall scaling of the logarithmic amplifier. The load resistance, R_L, should not be lower than 5 kΩ so that the full-scale output of 1.75 V can be generated with the limited available current of 400 μA max.

As stated in the Absolute Maximum Ratings table, an externally applied overvoltage on the VOUT pin, which is outside the range 0 V to V_{POS}, is sufficient to cause permanent damage to the device. If overvoltages are expected on the VOUT pin, a series resistor, R_{PROT}, should be included as shown. A 500 Ω resistor is sufficient to protect against overvoltage up to ±5 V; 1000 Ω should be used if an overvoltage of up to ±15 V is expected. Since the output stage is meant to drive loads of no more than 400 μA, this resistor does not impact device performance for higher impedance drive applications (higher output current applications are discussed in the Increasing Output Current section).

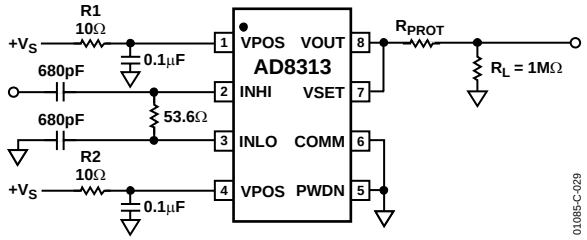

Figure 29. Basic Connections for Log (RSSI) Mode

OPERATING IN CONTROLLER MODE

Figure 30 shows the basic connections for operation in controller mode. The link between VOUT and VSET is broken and a setpoint is applied to VSET. Any difference between V_{SET} and the equivalent input power to the AD8313 drives V_{OUT} either to the supply rail or close to ground. If V_{SET} is greater than the equivalent input power, V_{OUT} is driven toward ground, and vice versa.

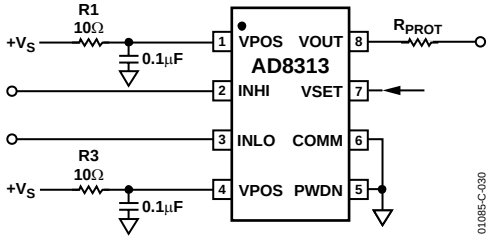

Figure 30. Basic Connections for Operation in the Controller Mode

This mode of operation is useful in applications where the output power of an RF power amplifier (PA) is to be controlled by an analog AGC loop (Figure 31). In this mode, a setpoint voltage, proportional in dB to the desired output power, is applied to the VSET pin. A sample of the output power from the PA, via a directional coupler or other means, is fed to the input of the AD8313.

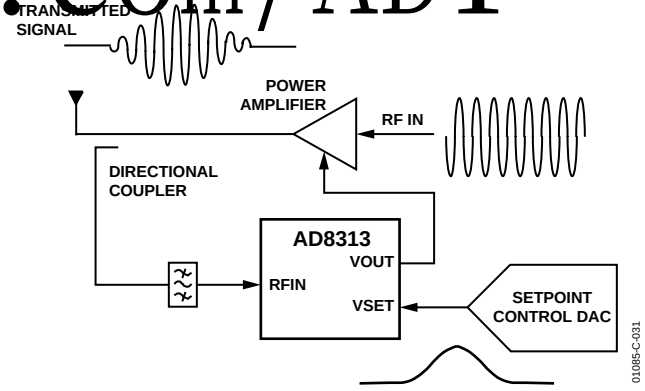

Figure 31. Setpoint Controller Operation

V_{OUT} is applied to the gain control terminal of the power amplifier. The gain control transfer function of the power amplifier should be an inverse relationship, that is, increasing voltage decreases gain.

A positive input step on V_{SET} (indicating a demand for increased power from the PA) drives V_{OUT} toward ground. This should be arranged to increase the gain of the PA. The loop settles when V_{OUT} settles to a voltage that sets the input power to the AD8313 to the dB equivalent of V_{SET}.

INPUT COUPLING

The signal can be coupled to the AD8313 in a variety of ways. In all cases, there must not be a dc path from the input pins to ground. Some of the possibilities include dual-input coupling capacitors, a flux-linked transformer, a printed circuit balun, direct drive from a directional coupler, or a narrow-band impedance matching network.

Figure 32 shows a simple broadband resistive match. A termination resistor of 53.6 Ω combines with the internal input impedance of the AD8313 to give an overall resistive input impedance of approximately 50 Ω. It is preferable to place the termination resistor directly across the input pins, INHI to INLO, where it lowers the possible deleterious effects of dc offset voltages on the low end of the dynamic range. At low frequencies, this may not be quite as beneficial, since it requires larger coupling capacitors. The two 680 pF input coupling capacitors set the high-pass corner frequency of the network at 9.4 MHz.

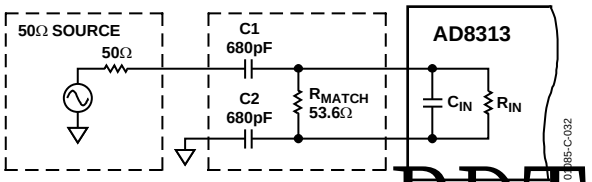

Figure 32. A Simple Broadband Resistive Input Termination

The high-pass corner frequency can be set higher according to the equation

$$f_{3dB} = \frac{1}{2 \times \pi \times C \times 50}$$

where:

$$C = \frac{C1 \times C2}{C1 \times C2}$$

In high frequency applications, the use of a transformer, balun, or matching network is advantageous. The impedance matching characteristics of these networks provide what is essentially a gain stage before the AD8313 that increases the device sensitivity. This gain effect is explored in the following matching example.

Figure 33 and Figure 34 show device performance under these three input conditions at 900 MHz and 1.9 GHz.

While the 900 MHz case clearly shows the effect of input matching by realigning the intercept as expected, little improvement is seen at 1.9 GHz. Clearly, if no improvement in sensitivity is required, a simple 50 Ω termination may be the best choice for a given design based on ease of use and cost of components.

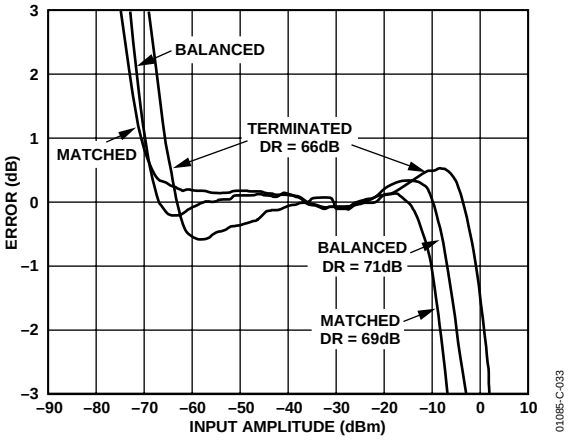

Figure 33. Comparison of Terminated, Matched, and Balanced Input Drive at 900 MHz

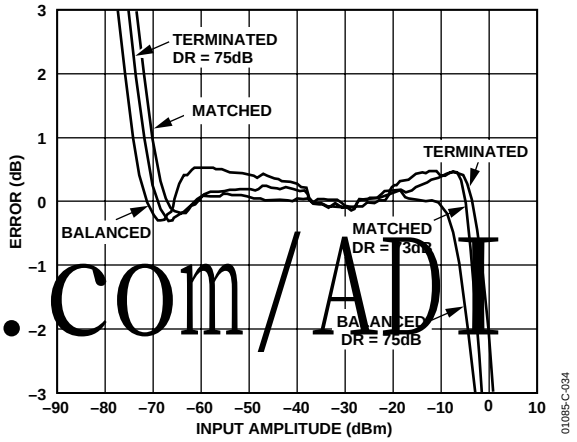

Figure 34. Comparison of Terminated, Matched, and Balanced Input Drive at 1.9 GHz

NARROW-BAND LC MATCHING EXAMPLE AT 100 MHz

While numerous software programs provide an easy way to calculate the values of matching components, a clear understanding of the calculations involved is valuable. A low frequency (100 MHz) value has been used for this example because of the deleterious board effects at higher frequencies. RF layout simulation software is useful when board design at higher frequencies is required.

A narrow-band LC match can be implemented either as a series-inductance/shunt-capacitance or as a series-capacitance/shunt-inductance. However, the concurrent requirement that the AD8313 inputs, INHI and INLO, be ac-coupled, makes a series-capacitance/shunt-inductance type match more appropriate (Figure 35).

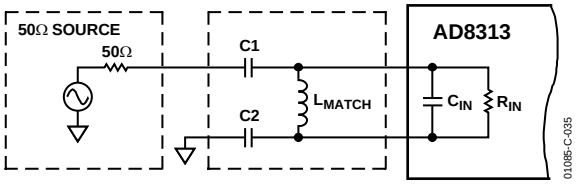

Figure 35. Narrow-Band Reactive Match

Typically, the AD8313 needs to be matched to 50 Ω. The input impedance of the AD8313 at 100 MHz can be read from the Smith chart (Figure 26) and corresponds to a resistive input impedance of 900 Ω in parallel with a capacitance of 1.1 pF.

To make the matching process simpler, the AD8313 input capacitance, C_{IN}, can be temporarily removed from the calculation by adding a virtual shunt inductor (L2), which resonates away C_{IN} (Figure 36). This inductor is factored back into the calculation later. This allows the main calculation to be based on a simple resistive-to-resistive match, that is, 50 Ω to 900 Ω.

The resonant frequency is defined by the equation

$$\omega = \frac{1}{\sqrt{L2 \times C_{IN}}}$$

therefore,

$$L2 = \frac{1}{\omega^2 C_{IN}} = 2.3\ \mu\text{H}$$

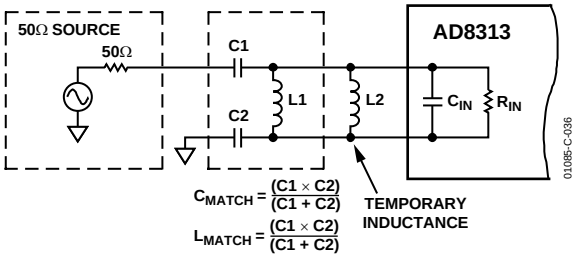

Figure 36. Input Matching Example

With C_{IN} and L2 temporarily out of the picture, the focus is now on matching a 50 Ω source resistance to a (purely resistive) load of 900 Ω and calculating values for C_{MATCH} and $L1$. When

$$R_S R_{IN} = \frac{L1}{C_{MATCH}}$$

the input looks purely resistive at a frequency given by

$$f_0 = \frac{1}{2\pi\sqrt{L1 \times C_{MATCH}}} = 100\ \text{MHz}$$

Solving for C_{MATCH} gives

$$C_{MATCH} = \frac{1}{\sqrt{R_S R_{IN}}} \times \frac{1}{2\pi f_0} = 7.5\ \text{pF}$$

Solving for $L1$ gives

$$L1 = \frac{\sqrt{R_S}\, R_{IN}}{2\pi f_0} = 337.6\ \text{nH}$$

Because $L1$ and $L2$ are parallel, they can be combined to give the final value for L_{MATCH}, that is,

$$L_{MATCH} = \frac{L1 \times L2}{L1 + L2} = 294\ \text{nH}$$

C1 and C2 can be chosen in a number of ways. First, C2 can be set to a large value, for example, 1000 pF, so that it appears as an RF short. C1 would then be set equal to the calculated value of C_{MATCH}. Alternatively, C1 and C2 can each be set to twice C_{MATCH} so that the total series capacitance is equal to C_{MATCH}. By making C1 and C2 slightly unequal (that is, select C2 to be about 10% less than C1) but keeping their series value the same, the amplitude of the signals on INHI and INLO can be equalized so that the AD8313 is driven in a more balanced manner. Any of the options detailed above can be used provided that the combined series value of C1 and C2, that is, C1 × C2/(C1 + C2) is equal to C_{MATCH}.

In all cases, the values of C_{MATCH} and L_{MATCH} must be chosen from standard values. At this point, these values need now be installed on the board and measured for performance at 100 MHz. Because of board and layout parasitics, the component values from the preceding example had to be tuned to the final values of C_{MATCH} = 8.9 pF and L_{MATCH} = 270 nH as shown in Table 4.

Assuming a lossless matching network and noting conservation of power, the impedance transformation from R_S to R_{IN} (50 Ω to 900 Ω) has an associated voltage gain given by

$$Gain_{\text{dB}} = 20 \times \log\sqrt{\frac{R_{IN}}{R_S}} = 12.6\ \text{dB}$$

Because the AD8313 input responds to *voltage* and not to true power, the voltage gain of the matching network increases the effective input low-end power sensitivity by this amount. Thus, in this case, the dynamic range is shifted downward, that is, the 12.6 dB voltage gain shifts the 0 dBm to −65 dBm input range downward to −12.6 dBm to −77.6 dBm. However, because of network losses, this gain is not be fully realized in practice. Refer to Figure 33 and Figure 34 for an example of practical attainable voltage gains.

Table 4 shows recommended values for the inductor and capacitors in Figure 35 for some selected RF frequencies in addition to the associated theoretical voltage gain. These values for a reactive match are optimal for the board layout detailed as Figure 45.

As previously discussed, a modification of the board layout produces networks that may not perform as specified. At 2.5 GHz, a shunt inductor is sufficient to achieve proper matching. Consequently, C1 and C2 are set sufficiently high that they appear as RF shorts.

Table 4. Recommended Values for C1, C2, and L_{MATCH} in Figure 35

Freq. (MHz)	C_{MATCH} (pF)	C1 (pF)	C2 (pF)	L_{MATCH} (nH)	Voltage Gain(dB)
100	8.9	22	15	270	12.6
			1000	270	
900	1.5	3	3	8.2	9.0
		1.5	1000	8.2	
1900	1.5	3	3	2.2	6.2
		1.5	1000	2.2	
2500	Large	390	390	2.2	3.2

Figure 37 shows the voltage response of the 100 MHz matching network. Note the high attenuation at lower frequencies typical of a high-pass network.

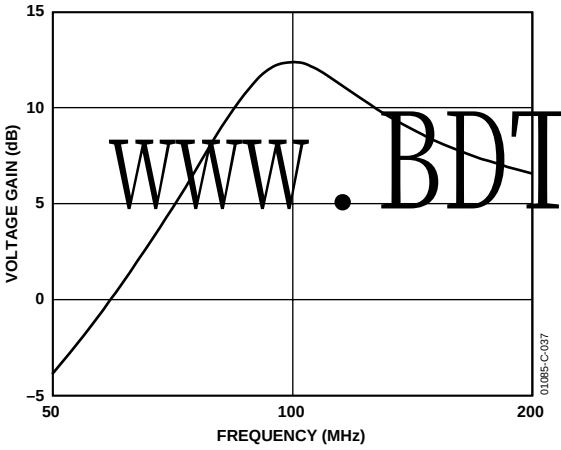

Figure 37. Voltage Response of 100 MHz Narrow-Band Matching Network

ADJUSTING THE LOG SLOPE

Figure 38 shows how the log slope can be adjusted to an exact value. The idea is simple: the output at the VOUT pin is attenuated by the variable resistor R2 working against the internal 18 kΩ of input resistance at the VSET pin. When R2 is 0, the attenuation it introduces is 0, and thus the slope is the basic 18 mV/dB. Note that this value varies with frequency, (Figure 10). When R2 is set to its maximum value of 10 kΩ, the attenuation from VOUT to VSET is the ratio 18/(18 + 10), and the slope is raised to (28/18) × 18 mV, or 28 mV/dB. At about the midpoint, the nominal scale is 23 mV/dB. Thus, a 70 dB input range changes the output by 70 × 23 mV, or 1.6 V.

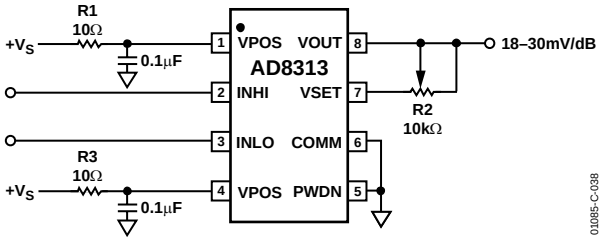

Figure 38. Adjusting the Log Slope

As stated, the unadjusted log slope varies with frequency from 17 mV/dB to 20 mV/dB, as shown in Figure 10. By placing a resistor between VOUT and VSET, the slope can be adjusted to a convenient 20 mV/dB as shown in Figure 39.

Table 5 shows the recommended values for this resistor, R_{EXT}. Also shown are values for R_{EXT}, which increase the slope to approximately 50 mV/dB. The corresponding voltage swings for a −65 dBm to 0 dBm input range are also shown in Table 6.

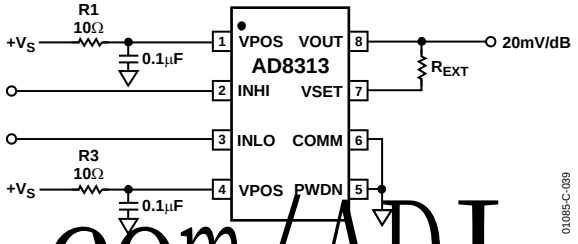

Figure 39. Adjusting the Log Slope to a Fixed Value

Table 5. Values for R_{EXT} in Figure 39

Frequency MHz	R_{EXT} kV	Slope mV/dB	V_{OUT} Swing for Pin −65 dBm to 0 dBm – V
100	0.953	20	0.44 to 1.74
900	2.00	20	0.58 to 1.88
1900	2.55	20	0.70 to 2.00
2500	0	20	0.54 to 1.84
100	29.4	50	1.10 to 4.35
900	32.4	50.4	1.46 to 4.74
1900	33.2	49.8	1.74 to 4.98
2500	26.7	49.7	1.34 to 4.57

The value for R_{EXT} is calculated by

$$R_{EXT} = \frac{(New\ Slope - Original\ Slope)}{Original\ Slope} \times 18\ \text{k}\Omega$$

The value for the *Original Slope*, at a particular frequency, can be read from Figure 10. The resulting output swing is calculated by simply inserting the New Slope value and the intercept at that frequency (Figure 10 and Figure 13) into the general equation for the AD8313's output voltage:

$$V_{OUT} = Slope(P_{IN} - Intercept)$$

INCREASING OUTPUT CURRENT

To drive a more substantial load, either a pull-up resistor or an emitter-follower can be used.

In Figure 40, a 1 kΩ pull-up resistor is added at the output, which provides the load current necessary to drive a 1 kΩ load to 1.7 V for V_S = 2.7 V. The pull-up resistor slightly lowers the intercept and the slope. As a result, the transfer function of the AD8313 is shifted upward (intercept shifts downward).

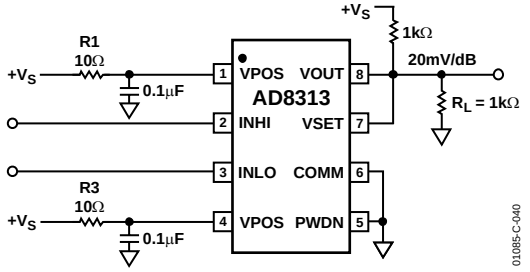

Figure 40. Increasing AD8313 Output Current Capability

In Figure 41, an emitter-follower provides the current gain, when a 100 Ω load can readily be driven to full-scale output. While a high ß transistor such as the BC848BLT1 (min ß = 200) is recommended, a 2 kΩ pull-up resistor between VOUT and $+V_S$ can provide additional base current to the transistor.

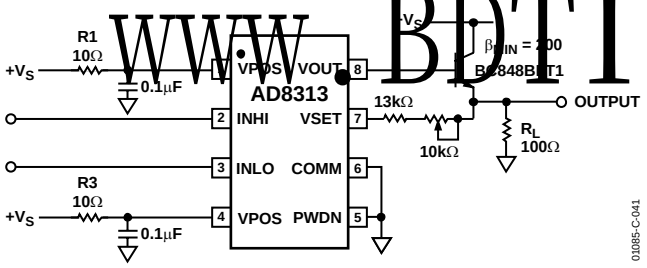

Figure 41. Output Current Drive Boost Connection

In addition to providing current gain, the resistor/potentiometer combination between VSET and the emitter of the transistor increases the log slope to as much as 45 mV/dB, at maximum resistance. This gives an output voltage of 4 V for a 0 dBm input. If no increase in the log slope is required, VSET can be connected directly to the emitter of the transistor.

EFFECT OF WAVEFORM TYPE ON INTERCEPT

Although specified for input levels in dBm (dB relative to 1 mW), the AD8313 responds to voltage and not to power. A direct consequence of this characteristic is that input signals of equal rms power but differing crest factors produce different results at the log amp's output.

Different signal waveforms vary the effective value of the log amp's intercept upward or downward. Graphically, this looks like a vertical shift in the log amp's transfer function. The device's logarithmic slope, however, is in principle not affected. For example, if the AD8313 is being fed alternately from a continuous wave and from a single CDMA channel of the same rms power, the AD8313 output voltage differs by the equivalent of 3.55 dB (64 mV) over the complete dynamic range of the device (the output for a CDMA input being lower).

Table 6 shows the correction factors that should be applied to measure the rms signal strength of a various signal types. A continuous wave input is used as a reference. To measure the rms power of a square wave, for example, the mV equivalent of the dB value given in the table (18 mV/dB × 3.01 dB) should be subtracted from the output voltage of the AD8313.

Table 6. Shift in AD8313 Output for Signals with Differing Crest Factors

Signal Type	Correction Factor (Add to Output Reading)
CW Sine Wave	0 dB
Square Wave or DC	−3.01 dB
Triangular Wave	+0.9 dB
GSM Channel (All Time Slots On)	+0.55 dB
CDMA Channel	+3.55 dB
PDC Channel (All Time Slots On)	+0.58 dB
Gaussian Noise	+2.51 dB

EVALUATION BOARD

SCHEMATIC AND LAYOUT

Figure 44 shows the schematic of the AD8313 evaluation board. Note that uninstalled components are indicated as *open*. This board contains the AD8313 as well as the AD8009 current-feedback operational amplifier.

This is a 4-layer board (top and bottom signal layers, ground, and power). The top layer silkscreen and layout are shown in Figure 42 and Figure 43. A detailed drawing of the recommended PCB footprint for the MSOP package and the pads for the matching components are shown in Figure 45.

The vacant portions of the signal and power layers are filled out with ground plane for general noise suppression. To ensure a low impedance connection between the planes, there are multiple through-hole connections to the RF ground plane. While the ground planes on the power and signal planes are used as general-purpose ground returns, any RF grounds related to the input matching network (for example, C2) are returned directly to the RF internal ground plane.

GENERAL OPERATION

The AD8313 should be powered by a single supply in the range of 2.7 V to 5.5 V. The power supply to each AD8313 VPOS pin is decoupled by a 10 Ω resistor and a 0.1 µF capacitor. The AD8009 can run on either single or dual supplies, +5 V to ±6 V. Both the positive and negative supply traces are decoupled using a 0.1 µF capacitor. Pads are provided for a series resistor or inductor to provide additional supply filtering.

The two signal inputs are ac-coupled using 680 pF high quality RF capacitors (C1, C2). A 53.6 Ω resistor across the differential signal inputs (INHI, INLO) combines with the internal 900 Ω input impedance to give a broadband input impedance of 50.6 Ω. This termination is not optimal from a noise perspective due to the Johnson noise of the 53.6 Ω resistor. Neither does it account for the AD8313's reactive input impedance nor for the decrease over frequency of the resistive component of the input impedance. However, it does allow evaluation of the AD8313 over its complete frequency range without having to design multiple matching networks.

For optimum performance, a narrow-band match can be implemented by replacing the 53.6 Ω resistor (labeled L/R) with an RF inductor and replacing the 680 pF capacitors with appropriate values. The Narrow-Band LC Matching Example at 100 MHz section includes a table of recommended values for selected frequencies and explains the method of calculation.

Switch 1 is used to select between power-up and power-down modes. Connecting the PWDN pin to ground enables normal operation of the AD8313. In the opposite position, the PWDN pin can be driven externally (SMA connector labeled ENBL) to either device state, or it can be allowed to float to a disabled device state.

The evaluation board comes with the AD8313 configured to operate in RSSI/measurement mode. This mode is set by the 0 Ω resistor (R11), which shorts the VOUT and VSET pins to each other. When using the AD8009, the AD8313 logarithmic output appears on the SMA connector labeled VOUT. Using only the AD8313, the log output can be measured at TP1 or the SMA connector labeled VSET.

USING THE AD8009 OPERATIONAL AMPLIFIER

The AD8313 can supply only 400 µA at VOUT. It is also sensitive to capacitive loading, which can cause inaccurate measurements, especially in applications where the AD8313 is used to measure the envelope of RF bursts.

The AD8009 alleviates both of these issues. It is an ultrahigh speed current feedback amplifier capable of delivering over 175 mA of load current, with a slew rate of 5,500 V/µs, which results in a rise time of 545 ps, making it ideal as a pulse amplifier.

The AD8009 is configured as a buffer amplifier with a gain of 1. Other gain options can be implemented by installing the appropriate resistors at R10 and R12.

Various output filtering and loading options are available using R5, R6, and C6. Note that some capacitive loads may cause the AD8009 to become unstable. It is recommended that a 42.2 Ω resistor be installed at R5 when driving a capacitive load. More details can be found in the AD8009 data sheet.

VARYING THE LOGARITHMIC SLOPE

The slope of the AD8313 can be increased from its nominal value of 18 mV/dB to a maximum of 40 mV/dB by removing R11, the 0 Ω resistor, which shorts VSET to VOUT. VSET and VOUT are now connected through the 20 kΩ potentiometer. The AD8009 must be configured for a gain of 1 to accurately vary the slope of the AD8313.

OPERATING IN CONTROLLER MODE

To put the AD8313 into controller mode, R7 and R11 should be removed, breaking the link between VOUT and VSET. The VSET pin can then be driven externally via the SMA connector labeled VSET.

RF BURST RESPONSE

The VOUT pin of the AD8313 is very sensitive to capacitive loading, as a result care must be taken when measuring the device's response to RF bursts. For best possible response time measurements it is recommended that the AD8009 be used to buffer the output from the AD8313. No connection should be made to TP1, the added load will effect the response time.

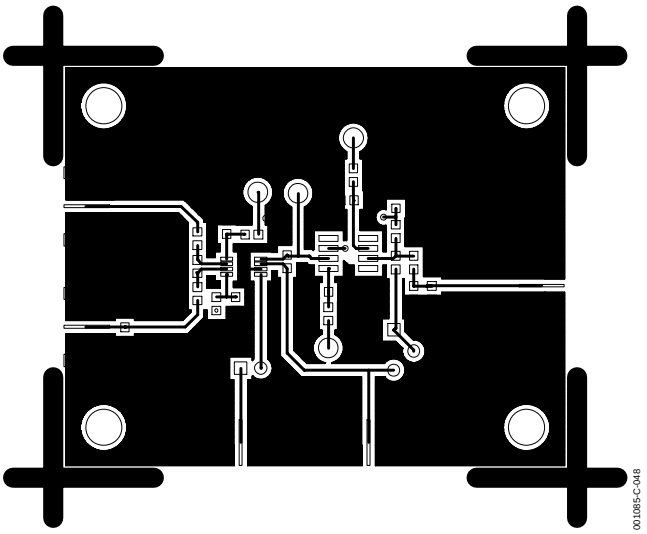

Figure 42. Layout of Signal Layer

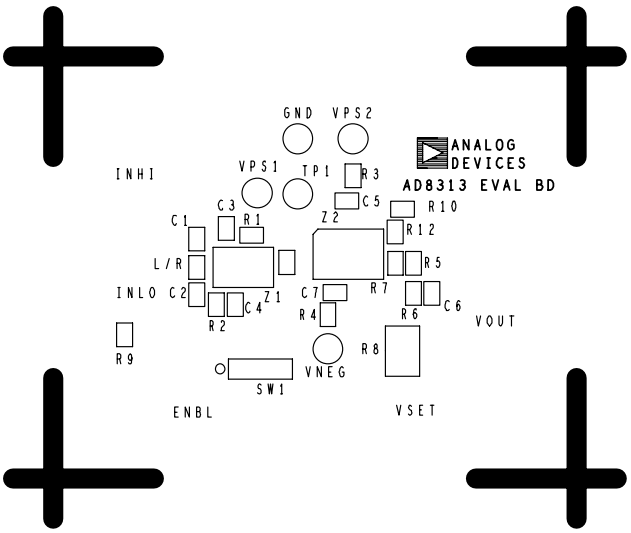

Figure 43. Signal Layer Silkscreen

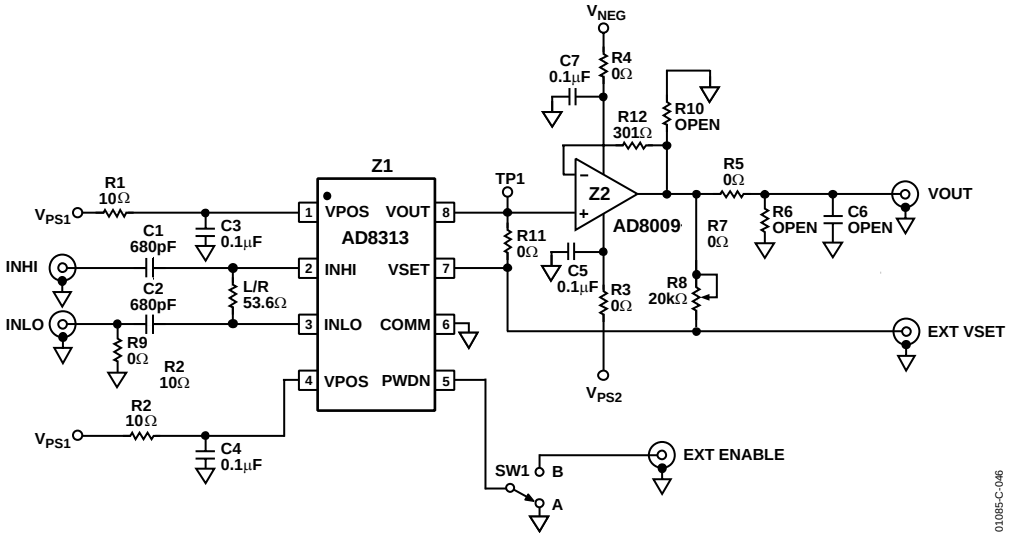

Figure 44. Evaluation Board Schematic

Table 7. Evaluation Board Configuration Options

Component	Function	Default
VPS1, VPS2, GND, VNEG	Supply Pins. VPS1 is the positive supply pin for the AD8313. VPS2 and VNEG are the positive and negative supply pins for the AD8009. If the AD8009 is being operated from a single supply, VNEG should be connected to GND. VPS1 and VPS2 are independent. GND is shared by both devices.	Not Applicable
Z1	AD8313 Logarithmic Amplifier. If the AD8313 is used in measurement mode, it is not necessary to power up the AD8009 op amp. The log output can be measured at TP1 or at the SMA connector labeled VSET.	Installed
Z1	AD8009 Operational Amplifier.	Installed
SW1	Device Enable. When in Position A, the PWDN pin is connected to ground and the AD8313 is in normal operating mode. In Position B, the PWDN pin is connected to an SMA connector labeled ENBL. A signal can be applied to this connector.	SW1 = A
R7, R8	Slope Adjust. The slope of the AD8313 can be increased from its nominal value of 18 mV/dB to a maximum of 40 mV/dB by removing R11, the 0 Ω resistor, which shorts VSET to VOUT, and installing a 0 Ω resistor at R7. The 20 kΩ potentiometer at R8 can then be used to change the slope. Operating in Controller Mode. To put the AD8313 into controller mode, R7 and R11 should be removed, breaking the link between VOUT and VSET. The VSET pin can then be driven externally via the SMA connector labeled VSET.	R7 = 0 Ω (Size 0603) R8 = installed
L/R, C1, C2, R9	Input Interface. The 52.3 Ω resistor in position L/R, along with C1 and C2, create a wideband 50 Ω input. Alternatively, the 52.3 Ω resistor can be replaced by an inductor to form an input matching network. See Input Coupling section for more details. Remove the 0 Ω resistor at R9 for differential drive applications.	L/R = 53.6 Ω (Size 0603) C1 = C2 = 680 pF (Size 0603) R9 = 0 Ω (Size 0603)
R10, R12	Op Amp Gain Adjust. The AD8009 is initially configured as a buffer; gain = 1. To increase the gain of the op amp, modify the resistor values R10 and R12.	R10 = open (Size 0603) R12 = 301 Ω (Size 0603)
R5, R6, C6	Op Amp Output Loading/Filtering. A variety of loading and filtering options are available for the AD8009. The robust output of the op amp is capable of driving low impedances such as 50 Ω or 75 Ω, configure R5 and R6 accordingly. See the AD8009 data sheet for more details.	R5 = 0 Ω (Size 0603) R6 = open (Size 0603) C6 = open (Size 0603)
R1, R2, R3, R4, C3, C4, C5, C7	Supply Decoupling.	R1 = R2 = 10 Ω (Size 0603) R3 = R4 = 0 Ω (Size 0603) C3 = C4 = 0.1 µF (Size 0603) C5 = C7 = 0.1 µF (Size 0603)

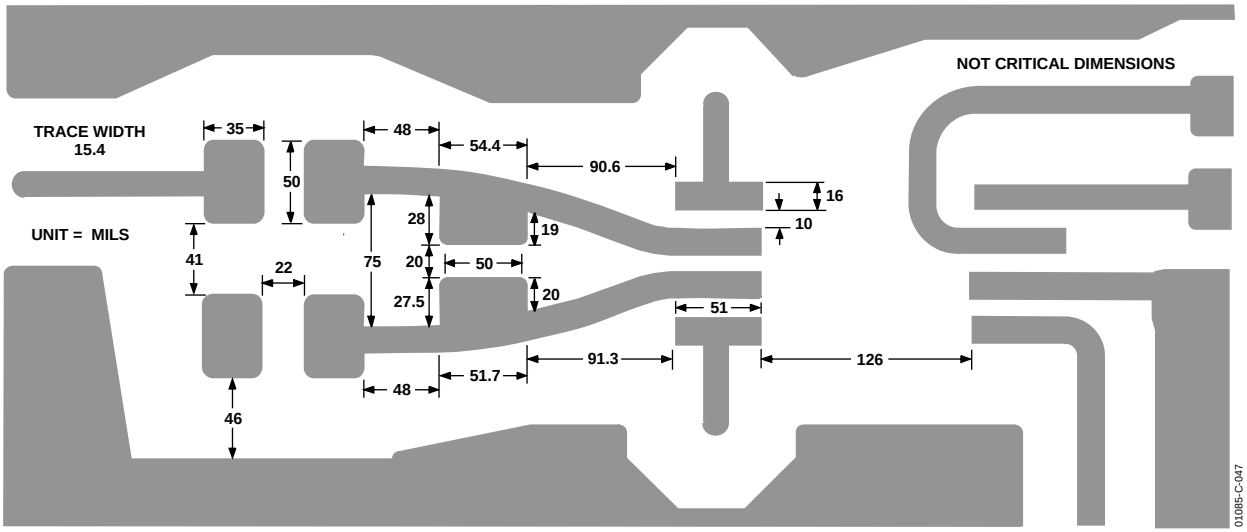

Figure 45. Detail of PCB Footprint for Package and Pads for Matching Network

OUTLINE DIMENSIONS

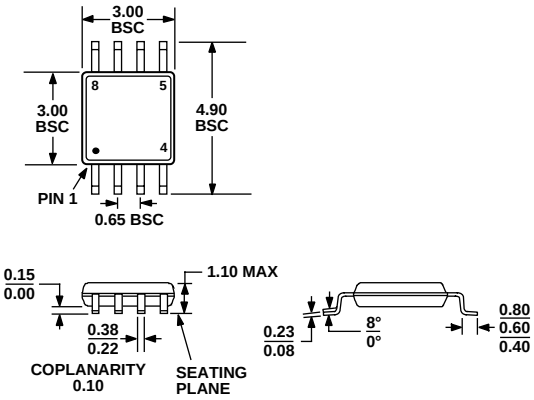

Figure 46 . 8-Lead MicroSOIC Package [MSOP]
(RM-08)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Option	Branding
AD8313ARM	−40°C to +85°C	8-Lead MSOP	RM-08	J1A
AD8313ARM-REEL	−40°C to +85°C	13" Tape and Reel	RM-08	J1A
AD8313ARM-REEL7	−40°C to +85°C	7" Tape and Reel	RM-08	J1A
AD8313ARMZ[1]	−40°C to +85°C	8-Lead MSOP		
AD8313ARMZ-REEL7[1]	−40°C to +85°C	7" Tape and Reel		
AD8313-EVAL		Evaluation Board		

[1] Z = Pb-free part.

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