Wide Supply Range, Rail-to-Rail Output Instrumentation Amplifier

Preliminary Technical Data

AD8226

FEATURES

- Gain set with 1 external resistor
  - Gain range: 1 to 1000
- Input voltage goes to ground
- Input overdrive protection
- Very wide power supply range
  - Dual supply: ±1.3 V to ±18 V
  - Single supply: 2.6 V to 36 V
- Bandwidth (G = 1): 800 kHz
- CMRR (G = 1): 78 dB minimum
- Input noise: 22 nV/rt(Hz)
- Typical supply current: 350 µA
- SOIC-8 and MSOP-8 packages

APPLICATIONS

- Industrial process controls
- Bridge amplifiers
- Medical instrumentation
- Portable data acquisition
- Multichannel systems

PIN CONFIGURATION

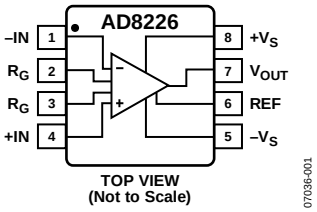

Figure 1.

GENERAL DESCRIPTION

The AD8226 is a low cost instrumentation amplifier that requires only one external resistor to set any gain between 1 and 1000.

The AD8226 is designed to work with a very wide range of voltages. It can operate on supplies ranging from ±1.2 V to ±18 V (2.4 V to 36 V single supply). The AD8226 comes with rail-to-rail output and a wide input range that includes the ability to go slightly below the negative supply. In addition, the AD8226 inputs can withstand voltages beyond the rail.

The AD8226 is perfect for multichannel, space-constrained applications. Being a low power and low cost amplifier allows multiple channels to be used.

The AD8226 has three grades. The A grade is the lower cost version and is specified for temperatures from −40°C to +85°C. The B grade is the higher performance version and is specified from −40°C to +85°C. The C grade version is the higher temperature version and is specified from −40°C to +105°C. All models are operational from −40°C to +125°C; behavior at these temperatures is shown in the typical performance curves. The AD8226 is available in MSOP and SOIC packages.

Table 1. Instrumentation Amplifiers by Category

General Purpose	Zero Drift	Military Grade	Low Power	High Speed PGA
AD8220[1]	AD8231[1]	AD620	AD627[1]	AD8250
AD8221	AD8290	AD621	AD623[1]	AD8251
AD8222	AD8293[1]	AD524	AD8226[1]	AD8253
AD8224[1]	AD8553[1]	AD526		
AD8228	AD8556[1]	AD624		
	AD8557[1]			

[1] Rail-to-rail output.

Rev. PrA

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SPECIFICATIONS

$+V_S$ = +15 V, $-V_S$ = −15 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	A, C Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
COMMON-MODE REJECTION RATIO (CMRR)								
CMRR DC to 60 Hz	V_{CM} = −10 V to +10 V							
G = 1		76			86			dB
G = 10		90			100			dB
G = 100		105			105			dB
G = 1000		105			105			dB
NOISE	*Total Noise*: $e_N = \sqrt{e_{NI}^2 + (e_{NO}/G^2)}$							
Voltage Noise, 1 kHz								
Input Voltage Noise, e_{NI}	V_{IN+}, V_{IN-}, V_{REF} = 0		22			22		nV/√Hz
Output Voltage Noise, e_{NO}			120			120		nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 1			3			3		μV p-p
G = 10			0.8			0.8		μV p-p
G = 100 to 1000			0.6			0.6		μV p-p
Current Noise	f = 1 kHz		100			100		fA/√Hz
	f = 0.1 Hz to 10 Hz		3			3		pA p-p
VOLTAGE OFFSET	*Total offset voltage :* $V_{OS} = V_{OSI} + (V_{OSO}/G)$							
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V			500			200	μV
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}							μV
Average temperature coefficient	$T_A = T_{MIN}$ to T_{MAX}							
Output Offset, V_{OSO}	V_S = ±5 V to ±15 V			1500			750	μV
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}							mV
Average temperature coefficient	$T_A = T_{MIN}$ to T_{MAX}		2	15		2	7	μV/°C
Offset RTI vs. Supply (PSR)	V_S = ±5 V to ±15 V							
G = 1		80			90			dB
G = 10		100			105			dB
G = 100		105			105			dB
G = 1000		105			105			dB
INPUT CURRENT								
Input Bias Current		10	20	30	10	20	30	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	5		40	5		40	nA
Average temperature coefficient	$T_A = T_{MIN}$ to T_{MAX}		100			100		pA/°C
Input Offset Current				3			2	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}			5			5	nA
Average temperature coefficient	$T_A = T_{MIN}$ to T_{MAX}		5			5		pA/°C
REFERENCE INPUT								
R_{IN}			100			100		kΩ
I_{IN}			7			7		μA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%

Parameter	Conditions	A, C Grade Min	A, C Grade Typ	A, C Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			1000			1000		kHz
G = 10			150			150		kHz
G = 100			15			15		kHz
G =1000			1.5			1.5		kHz
Settling Time 0.01%	10 V step							
G = 1			22			22		µs
G = 10			22			22		µs
G = 100			50			50		µs
G = 1000			600			600		µs
Slew Rate	G = 1		0.5			0.5		V/µs
	G = 5 to 100		1			1		V/µs
GAIN	$G = 1 + (49.4k\Omega/R_G)$							
Gain Range		1		1000	1		1000	V/V
Gain Error	V_{OUT} ±10 V							
G = 1				0.07			0.02	%
G = 10				0.3			0.1	%
G = 100				0.3			0.1	%
G = 1000				0.3			0.1	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 1	R_L = 10 kΩ							ppm
G = 100	R_L = 10 kΩ							ppm
G = 1000	R_L = 10 kΩ							ppm
G = 1-100	R_L = 2kΩ							ppm
Gain vs. Temperature								
G = 1	$T_A = T_{MIN}$ to T_{MAX}		2	10		2	5	ppm/°C
G > 1[1]	$T_A = T_{MIN}$ to T_{MAX}			−50			−50	ppm/°C
INPUT	V_S = ± 1.35 V to 36 V							
Input Impedance								
Differential			2||2			2||2		GΩ||pF
Common Mode			2||2			2||2		GΩ||pF
Input Operating Voltage Range[2]	T_A = 25°C	$-V_S - 0.1$		$+V_S - 0.7$	$-V_S - 0.1$		$+V_S - 0.7$	V
	T_A = −40°C	$-V_S - 0.15$		$+V_S - 0.9$	$-V_S - 0.15$		$+V_S - 0.9$	V
	T_A = 105°C	$-V_S - 0.05$		$+V_S - 0.6$	$-V_S - 0.05$		$+V_S - 0.6$	V
Input Overvoltage Range	$T_A = T_{MIN}$ to T_{MAX}	$+V_S$ −40		$-V_S$ +40	$+V_S$ −40		$-V_S$ +40	V
OUTPUT	V_S = ± 1.35 V to 36 V							
Output Swing	R_L = 10 kΩ to ground	$-V_S + 0.2$		$+V_S - 0.2$	$-V_S + 0.2$		$-V_S + 0.2$	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	$-V_S + 0.3$		$+V_S - 0.3$	$-V_S + 0.3$		$+V_S - 0.3$	V
Output Swing	R_L = 100 kΩ to ground	$-V_S + 0.1$		$+V_S - 0.1$	$-V_S + 0.1$		$-V_S + 0.1$	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	$-V_S + 0.1$		$+V_S - 0.1$	$-V_S + 0.1$		$-V_S + 0.1$	V
Short-Circuit Current			13				13	mA
POWER SUPPLY								
Operating Range	Dual supply operation	±1.3		±18	±1.3		±18	V
Quiescent Current			350	400		350	400	µA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}							µA
TEMPERATURE RANGE								
Specified Performance: T_{MIN} to T_{MAX}	A and B grades	−40		+85	−40		+85	°C
	C grade	−40		+105				
Operational		−40		+125	−40		+125	°C

[1] Does not include the effects of external resistor R_G
[2] Input voltage range of the AD8226 input stage. Input range depends on common mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section in the Theory of Operation for more information.

$+V_S$ = 2.7 V, $-V_S$ = 0 V, V_{REF} = 0 V, T_A = 25°C, G = 1, R_L = 10 kΩ, unless otherwise noted.

Table 3.

Parameter	Conditions	A,C Grade Min	A,C Grade Typ	A,C Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)								
CMRR DC to 60 Hz	V_{CM} = 0 V to 1.7 V							
G = 1		76			86			dB
G = 10		90			100			dB
G = 100		105			105			dB
G = 1000		105			105			dB
NOISE	*Total Noise*: $e_N = \sqrt{e_{NI}^2 + (e_{NO}/G^2)}$							
Voltage Noise, 1 kHz								
Input Voltage Noise, e_{NI}	V_{IN+}, V_{IN-}, V_{REF} = 0		22			22		nV/√Hz
Output Voltage Noise, e_{NO}			120			120		nV/√Hz
RTI	f = 0.1 Hz to 10 Hz							
G = 1			3			3		µV p-p
G = 10			0.8			0.8		µV p-p
G = 100 to 1000			0.6			0.6		µV p-p
Current Noise	f = 1 kHz		100			100		fA/√Hz
	f = 0.1 Hz to 10 Hz		3			3		pA p-p
VOLTAGE OFFSET	*Total offset voltage :* $V_{OS} = V_{OSI} + (V_{OSO}/G)$							
Input Offset, V_{OSI}	V_S = 0 V to 1.7 V			300			150	µV
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}							µV
Average TC	$T_A = T_{MIN}$ to T_{MAX}		0.1	4		0.1	2	µV/°C
Output Offset, V_{OSO}	V_S = 0 V to 1.7 V			1200			750	µV
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}							mV
Average TC	$T_A = T_{MIN}$ to T_{MAX}		2	15		2	7	µV/°C
Offset RTI vs. Supply (PSR)	V_S = 0 V to 1.7 V							
G = 1		80			90			dB
G = 10		100			105			dB
G = 100		105			105			dB
G = 1000		105			105			dB
INPUT CURRENT								
Input Bias Current		10	20	30	10	20	30	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	5		40	5		40	nA
Average TC	$T_A = T_{MIN}$ to T_{MAX}		100			100		pA/°C
Input Offset Current				3			2	nA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}			5			5	nA
Average TC	$T_A = T_{MIN}$ to T_{MAX}		5			5		pA/°C
REFERENCE INPUT								
R_{IN}			100			100		kΩ
I_{IN}			7			7		µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Reference Gain to Output			1			1		V/V
Reference Gain Error			0.01			0.01		%
DYNAMIC RESPONSE								
Small Signal –3 dB Bandwidth								
G = 1			1000			1000		kHz
G = 10			150			150		kHz
G = 100			15			15		kHz
G =1000			1.5			1.5		kHz

Parameter	Conditions	A,C Grade Min	A,C Grade Typ	A,C Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit
Settling Time 0.01%	2 V step							
G = 1			22			22		µs
G = 1 0			22			22		µs
G = 100			50			50		µs
G = 1000			600			600		µs
Slew Rate	G = 1		0.5			0.5		V/µs
	G = 5 to 100		1			1		V/µs
GAIN	$G = 1 + (49.4\ k\Omega/R_G)$							
Gain Range		1		1000	1		1000	V/V
Gain Error	V_{OUT} = 0 V to 1.7 V							
G = 1				0.07			0.02	%
G = 10				0.3			0.1	%
G = 100				0.3			0.1	%
G = 1000				0.3			0.1	%
Gain Nonlinearity	V_{OUT} = 0 V to 1.7 V							
G = 1	R_L = 10 kΩ							ppm
G = 100	R_L = 10 kΩ							ppm
G = 1000	R_L = 10 kΩ							ppm
G = 1-100	R_L = 2 kΩ							ppm
Gain vs. Temperature								
G = 1	$T_A = T_{MIN}$ to T_{MAX}		2	10		2	5	ppm/°C
G > 1[1]	$T_A = T_{MIN}$ to T_{MAX}			−50			−50	ppm/°C
INPUT	$-V_S$ = 0V; $+V_S$ = 2.7 V to 36 V							
Input Impedance								
Differential			2||2			2||2		GΩ||pF
Common Mode			2||2			2||2		GΩ||pF
Input Operating Voltage Range[2]	T_A = 25°C	− 0.1		$+V_S$ − 0.7	− 0.1		$+V_S$ − 0.7	V
	T_A = −40°C	− 0.15		$+V_S$ − 0.9	− 0.15		$+V_S$ − 0.9	V
	T_A = 105°C	− 0.05		$+V_S$ − 0.6	− 0.05		$+V_S$ − 0.6	V
Input Overvoltage Range	$T_A = T_{MIN}$ to T_{MAX}	$+V_S$ −40		$-V_S$ +40	$+V_S$ −40		$-V_S$ +40	
OUTPUT	$-V_S$ = 0V; $+V_S$ = 2.7 V to 36 V							
Output Swing	R_L = 10 kΩ to opposite supply	0.2		$+V_S$ − 0.2	0.2		$-V_S$ + 0.2	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	0.3		$+V_S$ − 0.3	0.3		$+V_S$ − 0.3	V
Output Swing	R_L = 100 kΩ to opposite supply	0.1		$+V_S$ − 0.1	0.1		$-V_S$ + 0.1	V
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	0.1		$+V_S$ − 0.1	0.1		$-V_S$ + 0.1	V
Short-Circuit Current			13			13		mA
POWER SUPPLY								
Operating Range	Single supply operation	2.6		36	2.6		36	V
Quiescent Current			300	350		300	350	µA
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}							µA
TEMPERATURE RANGE								
Specified Performance: T_{MIN} to T_{MAX}	A and B grades	−40		+85	−40		+85	°C
	C grade	−40		+105				
Operational		−40		+125	−40		+125	°C

[1] Does not include the effects of external resistor R_G

[2] Input voltage range of the AD8226 input stage. Input range depends on common mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section in the Theory of Operation for more information.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current	Indefinite
Maximum Voltage at –IN or +IN	–Vs + 40V
Minimum Voltage at –IN or +IN	+Vs – 40V
REF Voltage	±Vs
Differential Input Voltage	±40V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range[1]	–40°C to +125°C
Maximum Junction Temperature	140°C
ESD	
Human Body Model	2 kV
Charge Device Model	1 kV

[1] Temperature range for specified performance is either –40°C to +85°C or –40°C to +105°C, depending on grade.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air.

Table 5.

Package	θ_{JA}	Unit
8-Lead MSOP, 4-Layer JEDEC Board	135	°C/W
8-Lead SOIC, 4-Layer JEDEC Board	121	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

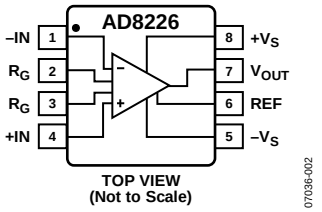


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input.
2, 3	R_G	Gain Setting Pins. Place gain resistor between these two pins.
4	+IN	Positive Input.
5	$-V_S$	Negative Supply.
6	REF	Reference. Must be driven by low impedance.
7	V_{OUT}	Output.
8	$+V_S$	Positive Supply.

THEORY OF OPERATION

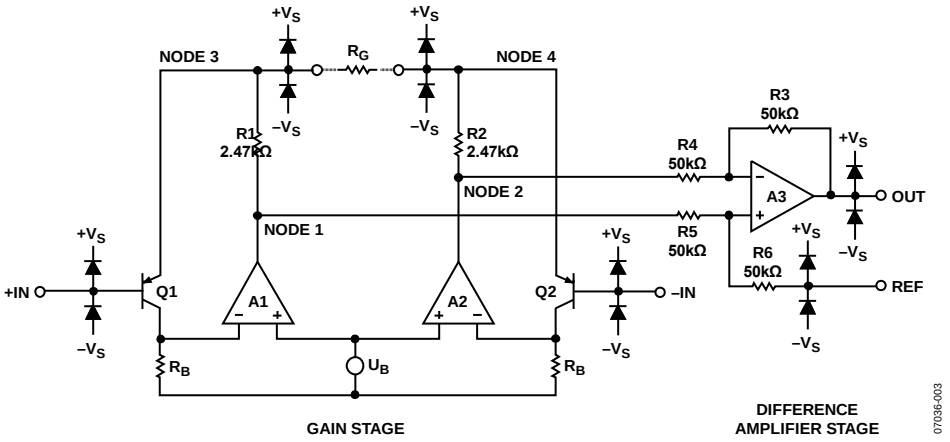


Figure 3. Simplified Schematic

ARCHITECTURE

The AD8226 is based on the classic three op amp topology. This topology has two stages: a preamplifier to provide differential amplification, followed by a difference amplifier to remove the common-mode voltage. Figure 3 shows a simplified schematic of the AD8226.

The first stage works as follows: in order to maintain a constant voltage across the Bias Resistor R_B, Amplifier A1 must keep Node 3 a constant diode drop above the positive input voltage. Similarly, Amplifier A2 keeps Node 4 at a constant diode drop above the negative input voltage. Therefore a replica of the differential input voltage is placed across the gain setting resistor, R_G. The current that flows across this resistance must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs. Note that, in addition to a gained differential signal, the original common-mode signal, shifted a diode drop down, is also still present.

The second stage is a difference amplifier, composed of A3 and four 50 kΩ resistors. The purpose of this stage is to remove the common-mode signal from the amplified differential signal.

Because the input amplifiers employ a current feedback architecture, the gain-bandwidth product of the AD8226 increases with gain, resulting in a system that does not suffer from the expected bandwidth loss of voltage feedback architectures at higher gains.

The transfer function of the AD8226 is

$$V_{OUT} = G(V_{IN+} - V_{IN-}) + V_{REF}$$

where

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G}$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8226, which can be calculated by referring to Table 7 or by using the following gain equation:

$$R_G = \frac{49.4\ \text{k}\Omega}{G - 1}$$

Table 7. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Calculated Gain
49.9 k	1.990
12.4 k	4.984
5.49 k	9.998
2.61 k	19.93
1.00 k	50.40
499	100.0
249	199.4
100	495.0
49.9	991.0

The AD8226 defaults to G = 1 when no gain resistor is used. The tolerance and gain drift of the R_G resistor should be added to the AD8226's specifications to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal.

INPUT PROTECTION

The input terminals of the AD8226 have input protection that allows the input voltage to go beyond the rails without damaging the part. Maximum voltage is –Vs+40 V and minimum voltage is +Vs-40 V. For example: with ±15 V supplies, the part can withstand input voltages of ±25 V; with a 5 V single supply, maximum input voltage is 40 V and minimum input voltage is 35 V.

REFERENCE TERMINAL

The output voltage of the AD8226 is developed with respect to the potential on the reference terminal. This is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8226 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For the best performance, source impedance to the REF terminal should be kept below 2 Ω. As shown in Figure 3, the reference terminal, REF, is at one end of a 50 kΩ resistor. Additional impedance at the REF terminal adds to this 50 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be computed by $2(50\ k\Omega + R_{REF})/100\ k\Omega + R_{REF}$.

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.

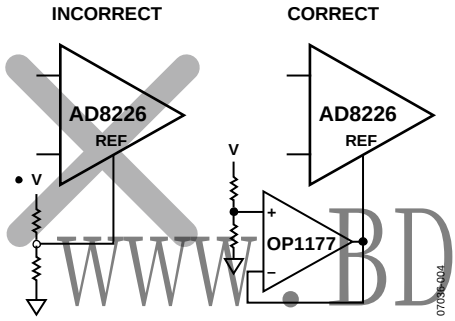


Figure 4. Driving the Reference Pin

INPUT VOLTAGE RANGE

The three op amp architecture of the AD8226 applies gain in the first stage before removing common-mode voltage in the difference amplifier stage. In addition, the input transistors in the first stage shift the common mode voltage up one diode drop (about 650 mV.) Therefore, internal nodes between the first and second stages (nodes 1 and 2 in Figure 3) experience a combination of gained signal, common-mode signal, and 650 mV. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. Figure XX through Figure XX show the allowable common-mode input voltage ranges for various output voltages and supply voltages.

The following formulas can also be used to understand how the reference voltage (V_{REF}), common mode input voltage (V_{CM}), and differential input voltage (V_{DIFF}) interact. These two formulas, along with the input range specifications in Table 1 and Table 3, set the boundaries where the part operates with best performance.

$$-V_S - 0.4\,V < \left|\frac{(V_{DIFF})(GAIN)}{2}\right| + V_{CM} < +V_S - 0.9\,V$$

$$\frac{(V_{DIFF})(GAIN)}{2} + V_{CM} + V_{REF} < +V_S - 1.6\,V$$

The common-mode input range shifts upwards with temperature. At cold temperatures, the part requires an extra 200 mV of headroom from the positive supply, and operation near the negative supply has more margin. Conversely, hot temperatures require less headroom from the positive supply, but are the worst-case conditions for input voltages near the negative supply.

LAYOUT

To ensure optimum performance of the AD8226 at the PCB level, care must be taken in the design of the board layout. The AD8226 pins are arranged in a logical manner to aid in this task.

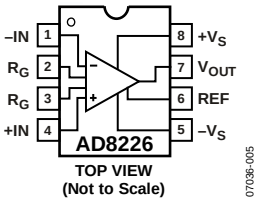


Figure 5. Pinout Diagram

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To keep CMRR across frequency high, input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input path (for example, for input protection) should be placed close to the in-amp inputs, which minimizes their interaction with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), the part should be chosen so that the parasitic capacitance is as small as possible.

Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance.

A 0.1 µF capacitor should be placed as close as possible to each supply pin. As shown in Figure 6, a 10 µF tantalum capacitor can be used farther away from the part. In most cases, it can be shared by other precision integrated circuits.

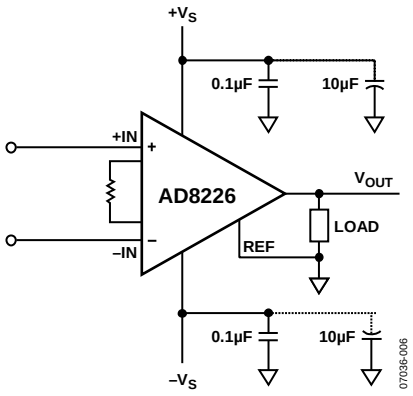


Figure 6. Supply Decoupling, REF, and Output Referred to Local Ground

References

The output voltage of the AD8226 is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8226 must have a return path to ground. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 7.

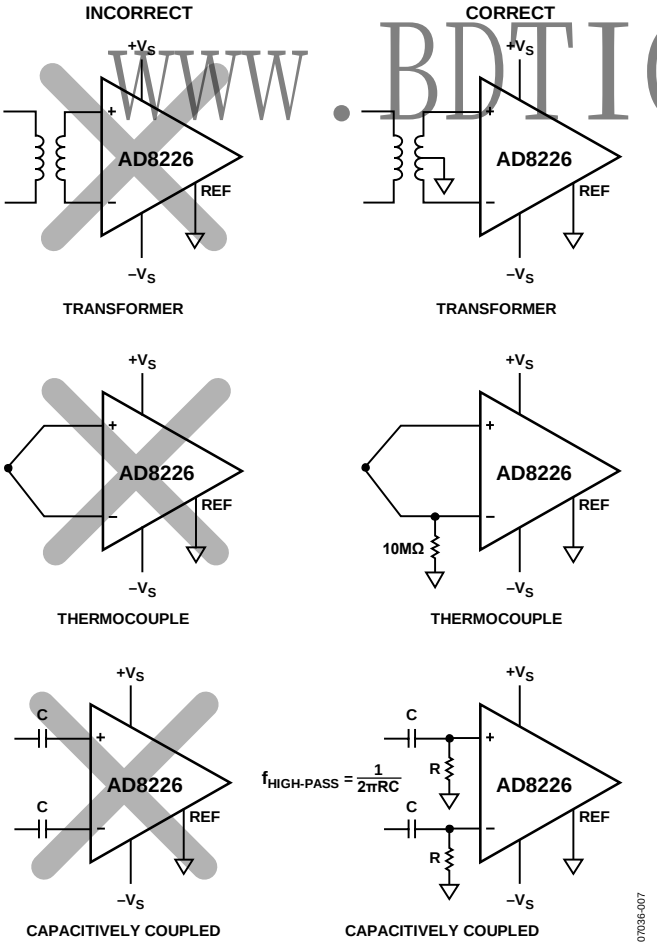


Figure 7. Creating an I_{BIAS} Path

RADIO FREQUENCY INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications having strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 8. The filter limits the input signal bandwidth, according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

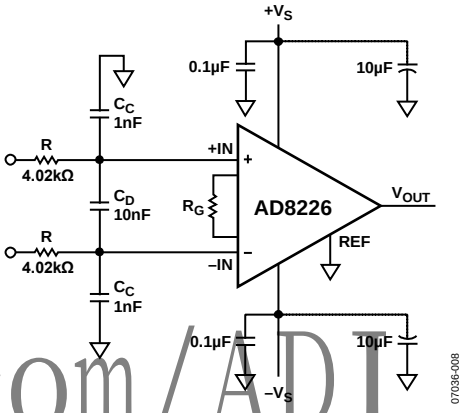
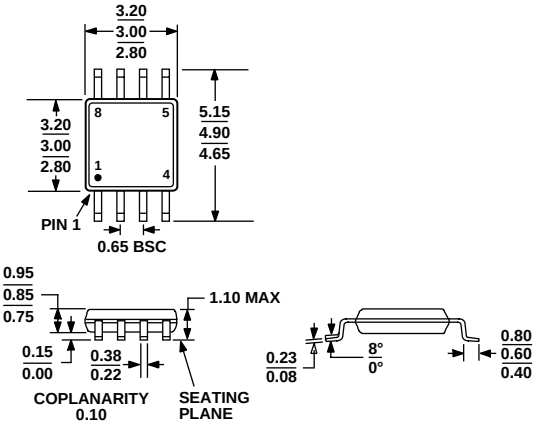


Figure 8. RFI Suppression

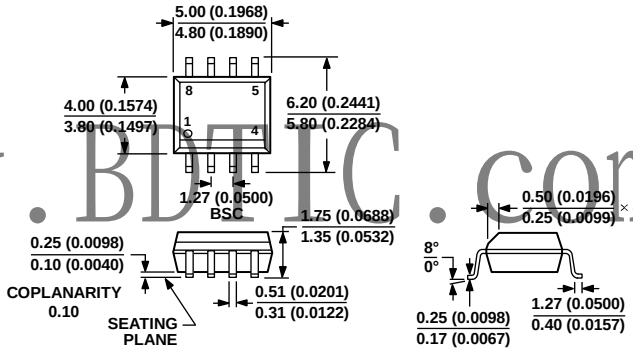
C_D affects the difference signal, and C_C affects the common-mode signal. Values of R and C_C should be chosen to minimize RFI. Mismatch between the R × C_C at the positive input and the R × C_C at the negative input degrades the CMRR of the AD8226. By using a value of C_D one magnitude larger than C_C, the effect of the mismatch is reduced, and performance is improved.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 9. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 10. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	PackageOption	Branding
AD8226ARMZ[1]	–40°C to +85°C	8-Lead MSOP	RM-8	Y16
AD8226ARMZ-RL[1]	–40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y16
AD8226ARMZ-R7[1]	–40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y16
AD8226ARZ[1]	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8226ARZ-RL[1]	–40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8226ARZ-R7[1]	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8226BRMZ[1]	–40°C to +85°C	8-Lead MSOP	RM-8	Y1M
AD8226BRMZ-RL[1]	–40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y1M
AD8226BRMZ-R7[1]	–40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y1M
AD8226BRZ[1]	–40°C to +85°C	8-Lead SOIC_N	R-8	
AD8226BRZ-RL[1]	–40°C to +85°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8226ARZ-R7[1]	–40°C to +85°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	
AD8226CRMZ[1]	–40°C to +105°C	8-Lead MSOP	RM-8	Y1Y
AD8226CRMZ-RL[1]	–40°C to +105°C	8-Lead MSOP, 13" Tape and Reel	RM-8	Y1Y
AD8226CRMZ-R7[1]	–40°C to +105°C	8-Lead MSOP, 7" Tape and Reel	RM-8	Y1Y
AD8226CRZ[1]	–40°C to +105°C	8-Lead SOIC_N	R-8	
AD8226CRZ-RL[1]	–40°C to +105°C	8-Lead SOIC_N, 13" Tape and Reel	R-8	
AD8226CRZ-R7[1]	–40°C to +105°C	8-Lead SOIC_N, 7" Tape and Reel	R-8	

[1] Z = RoHS Compliant Part.

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