High Speed, Triple Differential Receiver with Comparators

AD8145

FEATURES

High speed: 500 MHz, 2000 V/µs @ G = 1, V_O = 2 V p-p
0.1 dB flatness out to 75 MHz
High CMRR: 69 dB @ 10 MHz
High differential input impedance: 1 MΩ
Wide input common-mode range: ± 3.8 V (±5 V supplies)
On-chip gain-setting resistors
Can be configured for gain of 1 or 2
Fast settling: 15 ns to 0.1% @ 2 V p-p
Low input referred noise: 13nV/√Hz
Disable feature
Small packaging: 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

RGB video receivers
YPbPr video receivers
KVM (keyboard, video, mouse)
UTP (unshielded twisted pair) receivers

FUNCTIONAL BLOCK DIAGRAM

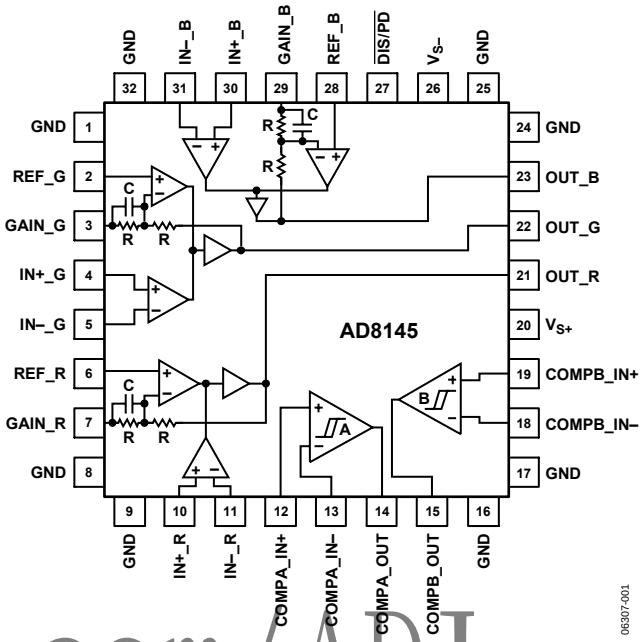

Figure 1.

GENERAL DESCRIPTION

The AD8145 is a triple, low cost, differential-to-single-ended receiver specifically designed for receiving red-green-blue (RGB) video signals over twisted pair cable or differential printed circuit board traces. It can also be used to receive any type of analog signal or high speed data transmission. Two auxiliary comparators with hysteresis are provided, which can be used to decode video sync signals that are encoded on the received common-mode voltages, to receive digital signals, or as general-purpose comparators. The AD8145 can be used in conjunction with the AD8133 or AD8134 triple differential drivers to provide a complete low cost solution for RGB over Category 5 UTP cable applications, including KVM.

The excellent common-mode rejection (69 dB @ 10 MHz) of the AD8145 allows for the use of low cost, unshielded twisted pair cables in noisy environments.

The AD8145 can be configured for a differential-to-single-ended gain of 1 or 2 by connecting the GAIN pin of each channel to its respective output (G = 1) or connecting it to a reference voltage (G = 2), which is normally grounded.

A REF input is provided on each channel that allows designers to level shift the output signals.

The AD8145 is available in a 5 mm × 5 mm, 32-lead LFCSP and is rated to work over the extended industrial temperature range of −40°C to +105°C.

Rev. 0

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REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, REF = 0 V, R_L = 150 Ω, C_L = 2 pF, G = 1, T_{MIN} to T_{MAX} = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p		530		MHz
	V_{OUT} = 2 V p-p		500		MHz
	V_{OUT} = 0.2 V p-p, G = 2		200		MHz
	V_{OUT} = 2 V p-p, G = 2		200		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p		75		MHz
	V_{OUT} = 2 V p-p, G = 2		100		MHz
Slew Rate	V_{OUT} = 2 V p-p		2100		V/µs
	V_{OUT} = 2 V p-p, G = 2		2100		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		15		ns
Output Overdrive Recovery			20		ns
NOISE/DISTORTION					
Second Harmonic	V_{OUT} = 2 V p-p, 1 MHz		−67		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 1 MHz		−88		dBc
Crosstalk	V_{OUT} = 2 V p-p, 10 MHz		−62		dB
Input Voltage Noise (RTI)	f ≥ 10 kHz		13		nV/√Hz
Differential Gain Error	NTSC, 200 IRE, R_L ≥ 150 Ω		0.25		%
Differential Phase Error	NTSC, 200 IRE, R_L ≥ 150 Ω		0.1		Degrees
INPUT CHARACTERISTICS					
Common-Mode Rejection	DC, V_{CM} = −3.5 V to +3.5 V	81	90		dB
	V_{CM} = 1 V p-p, f = 10 MHz		69		dB
	V_{CM} = 1 V p-p, f = 100 MHz		41		dB
Common-Mode Voltage Range	$V_{+IN} - V_{-IN}$ = 0 V		±3.5		V
Differential Operating Range			±2.5		V
Resistance	Differential		1		MΩ
	Common mode		1.3		MΩ
Capacitance	Differential		1		pF
	Common mode		2		pF
DC PERFORMANCE					
Closed-Loop Gain	DC, G = 2	1.955	1.985	2.020	V/V
Output Offset Voltage	G = 2	−17.5	7.0	1.0	mV
	T_{MIN} to T_{MAX}		−18		µV/°C
Input Bias Current (+IN, −IN)		6	−3.4	−0.9	µA
Input Bias Current Drift	T_{MIN} to T_{MAX} (+IN, −IN)		25		nA/°C
Input Offset Current		−400	−65	300	nA
OUTPUT PERFORMANCE					
Voltage Swing		−4.04		3.55	V
Output Current			50		mA
Short-Circuit Current	Short to GND, source/sink		195/−230		mA

Parameter	Conditions	Min	Typ	Max	Unit
COMPARATOR PERFORMANCE					
V_{OH}	R_L = 1 kΩ	3.205	3.310		V
V_{OL}	R_L = 1 kΩ		0.390	0.420	V
Input Offset Voltage			±2.5		mV
Hysteresis Width			18		mV
Input Bias Current			1.5		µA
Propagation Delay, t_{PLH}			6		ns
Propagation Delay, t_{PHL}			6		ns
Rise Time	10% to 90%		6		ns
Fall Time	10% to 90%		2		ns
POWER-DOWN PERFORMANCE					
Power-Down V_{IH}			V_{S+} − 1.65		V
Power-Down V_{IL}			V_{S+} − 2.65		V
Power-Down I_{IH}			0.5		µA
Power-Down I_{IL}			−250		µA
Power-Down Assert Time			1		µs
POWER SUPPLY					
Operating Range		4.5		11	V
Quiescent Current, Positive Supply			48.5	57.5	mA
	Disabled		16	19.5	mA
Quiescent Current, Negative Supply		−52	−43.5		mA
	Disabled	−13.9	−11		mA
PSRR, Positive Supply	DC		−79	−70	dB
PSRR, Negative Supply	DC		−68	−57	dB

T_A = 25°C, V_S = ±2.5 V, REF = 0 V, R_L = 1 kΩ, C_L = 2 pF, G = 1, T_{MIN} to T_{MAX} = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 0.2 V p-p		450		MHz
	V_{OUT} = 2 V p-p		425		MHz
	V_{OUT} = 0.2 V p-p, G = 2, R_L = 150 Ω		180		MHz
	V_{OUT} = 2 V p-p, G = 2, R_L = 150 Ω		180		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p		53		MHz
	V_{OUT} = 2 V p-p, G = 2, R_L = 150 Ω		100		MHz
Slew Rate	V_{OUT} = 2 V p-p		2000		V/µs
	V_{OUT} = 2 V p-p, G = 2, R_L = 150 Ω		2000		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		16		ns
Output Overdrive Recovery			10		ns
NOISE/DISTORTION					
Second Harmonic	V_{OUT} = 1 V p-p, 1 MHz		−71		dBc
Third Harmonic	V_{OUT} = 1 V p-p, 1 MHz		−76		dBc
Crosstalk	V_{OUT} = 1 V p-p, 10 MHz		−62		dB
Input Voltage Noise (RTI)	f ≥ 10 kHz		13		nV/√Hz
INPUT CHARACTERISTICS					
Common-Mode Rejection	DC, V_{CM} = −3.5 V to +3.5 V	78	86		dB
	V_{CM} = 1 V p-p, f = 10 MHz		72		dB
	V_{CM} = 1 V p-p, f = 100 MHz		43		dB
Common-Mode Voltage Range	$V_{+IN} - V_{-IN}$ = 0 V		±1.25		V
Differential Operating Range			±1.6		V
Resistance	Differential		1		MΩ
	Common mode		1.3		MΩ
Capacitance	Differential		1		pF
	Common mode		2		pF
DC PERFORMANCE					
Closed-Loop Gain	DC, G = 2	1.960	1.985	2.016	V/V
Output Offset Voltage	G = 2	−13.5	−4.5	2	mV
	T_{MIN} to T_{MAX}		−18		µV/°C
Input Bias Current (+IN, −IN)		−6	−3.5	−0.9	µA
Input Bias Current Drift	T_{MIN} to T_{MAX} (+IN, −IN)		25		nA/°C
Input Offset Current		−400	−60	300	nA
OUTPUT PERFORMANCE					
Voltage Swing	R_L = 150 Ω/1 kΩ	−1.35		1.3	V
Output Current			25		mA
Short-Circuit Current	Short to GND, source/sink		100/−100		mA
POWER-DOWN PERFORMANCE					
Power-Down V_{IH}			V_{S+} − 1.5		V
Power-Down V_{IL}			V_{S+} − 2.5		V
Power-Down I_{IH}			0.25		µA
Power-Down I_{IL}			50		µA
Power-Down Assert Time			1		µs

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		4.5		11	V
Quiescent Current, Positive Supply			40	47	mA
	Disabled		13.5	16	
Quiescent Current, Negative Supply		−43.5	−36		mA
	Disabled	−12.5	−10		
PSRR, Positive Supply	DC		−83	−73	dB
PSRR, Negative Supply	DC		−67	−62	dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12 V
Power Dissipation	See Figure 2
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +105°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad on the PCB surface, which is thermally connected to a copper plane.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5 mm × 5 mm, 32-Lead LFCSP	47	8.5	°C/W

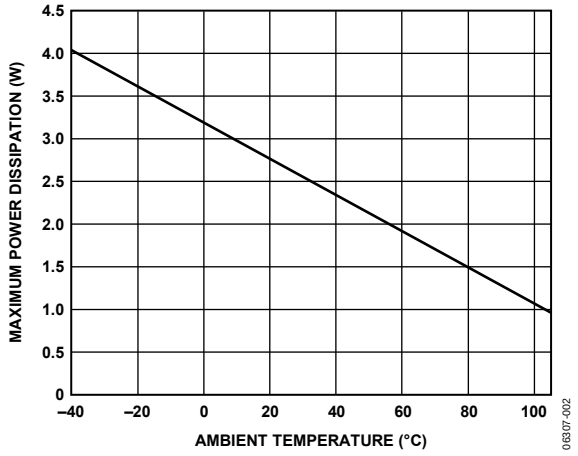


Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

Maximum Power Dissipation

The maximum safe power dissipation in the AD8145 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8145. Exceeding a junction temperature of 150°C for an extended period of time can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to all of the loads is equal to the sum of the power dissipation due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through-holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface, which is thermally connected to a copper plane to achieve the specified θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 32-lead LFCSP (47°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad, which is thermally connected to a PCB plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

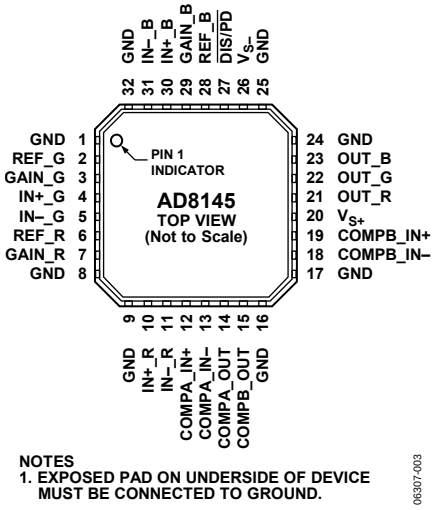


Figure 3. 32-Lead LFCSP Pin Configuration

Table 5. 32-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9,16, 17, 24, 25, 32	GND	Signal Ground and Thermal Plane Connection. (See the Absolute Maximum Ratings section.)
2	REF_G	Reference Input, Green Channel.
3	GAIN_G	Gain Connection, Green Channel.
4	IN+_G	Noninverting Input, Green Channel.
5	IN–_G	Inverting Input, Green Channel.
6	REF_R	Reference Input, Red Channel.
7	GAIN_R	Gain Connection, Red Channel.
10	IN+_R	Noninverting Input, Red Channel.
11	IN–_R	Inverting Input, Red Channel.
12	COMPA_IN+	Positive Input, Comparator A.
13	COMPA_IN-	Negative Input, Comparator A.
14	COMPA_OUT	Output, Comparator A.
15	COMPB_OUT	Output, Comparator B.
18	COMPB_IN-	Negative Input, Comparator B.
19	COMPB_IN+	Positive Input, Comparator B.
20	V_{S+}	Positive Power Supply.
21	OUT_R	Output, Red Channel.
22	OUT_G	Output, Green Channel.
23	OUT_B	Output, Blue Channel.
26	V_{S-}	Negative Power Supply.
27	$\overline{\text{DIS/PD}}$	Disable/Power Down.
28	REF_B	Reference Input, Blue Channel.
29	GAIN_B	Gain Connection, Blue Channel.
30	IN+_B	Noninverting Input, Blue Channel.
31	IN–_B	Inverting Input, Blue Channel.
Exposed Underside Pad	GND	Signal Ground and Thermal Plane Connection.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, G = 1, R_L = 150 Ω, C_L = 2 pF, REF = midsupply, V_S = ±5 V, T_A = 25°C. Refer to the circuit in Figure 35.

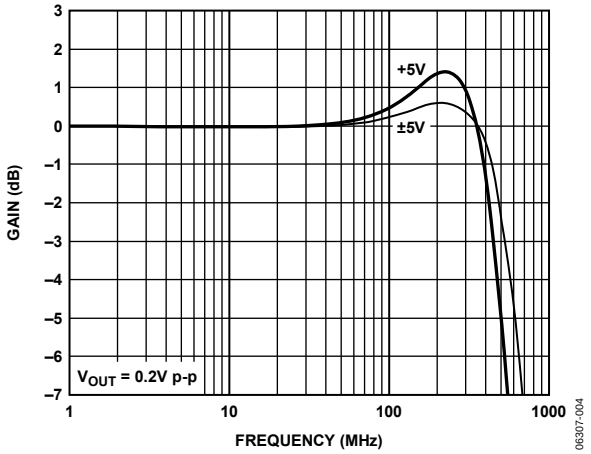


Figure 4. Small Signal Frequency Response at Various Power Supplies, G = 1

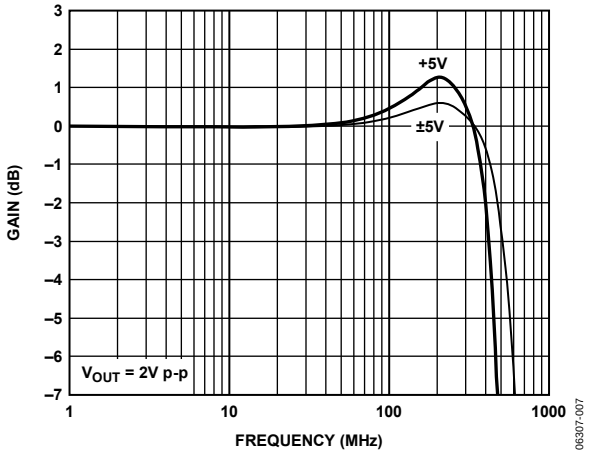


Figure 7. Large Signal Frequency Response at Various Power Supplies, G = 1

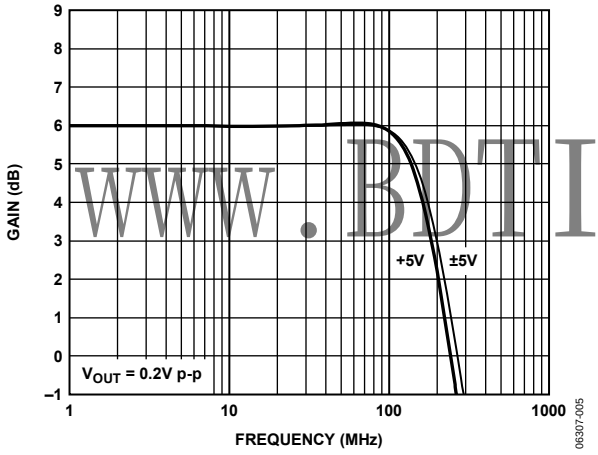


Figure 5. Small Signal Frequency Response at Various Power Supplies, G = 2

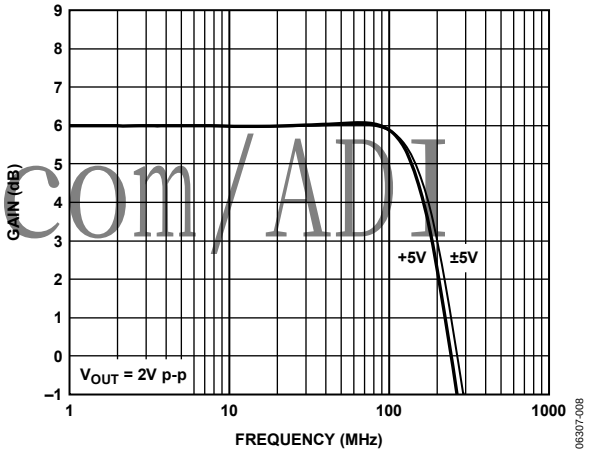


Figure 8. Large Signal Frequency Response at Various Power Supplies, G = 2

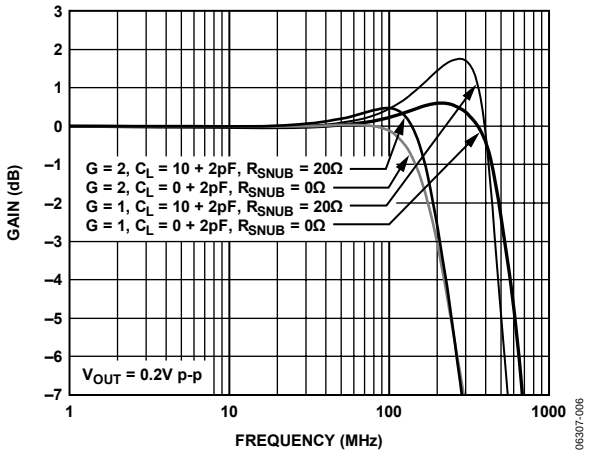


Figure 6. Small Signal Frequency Response at Various Gains and 10 pF Capacitive Load Buffered by 20 Ω Resistor

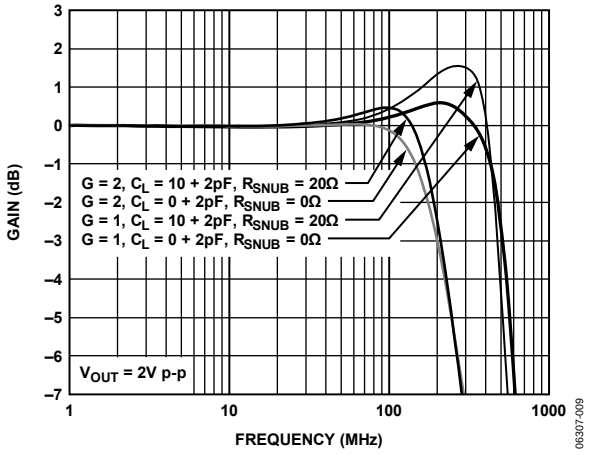


Figure 9. Large Signal Frequency Response at Various Gains and 10 pF Capacitive Load Buffered by 20 Ω Resistor

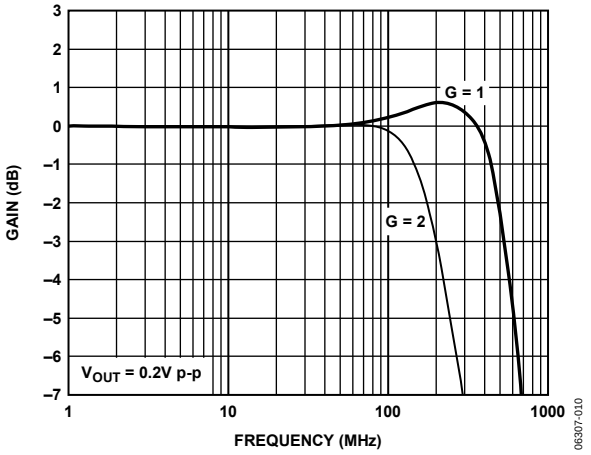


Figure 10. Small Signal Frequency Response at Various Gains

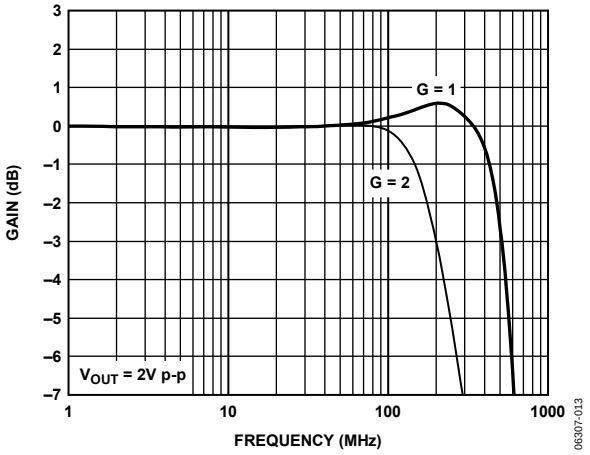


Figure 13. Large Signal Frequency Response at Various Gains

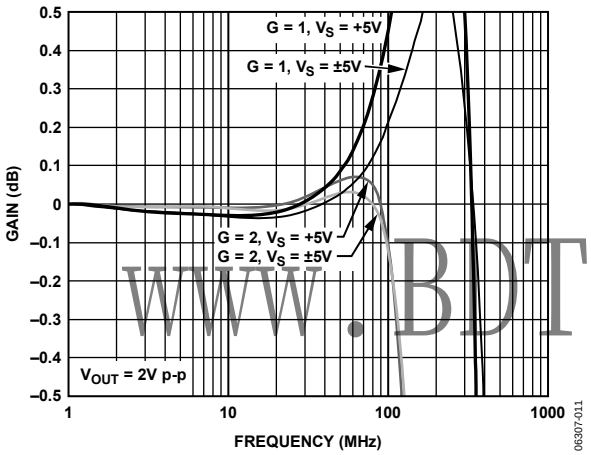


Figure 11. 0.1 dB Flatness for Various Power Supplies and Gains

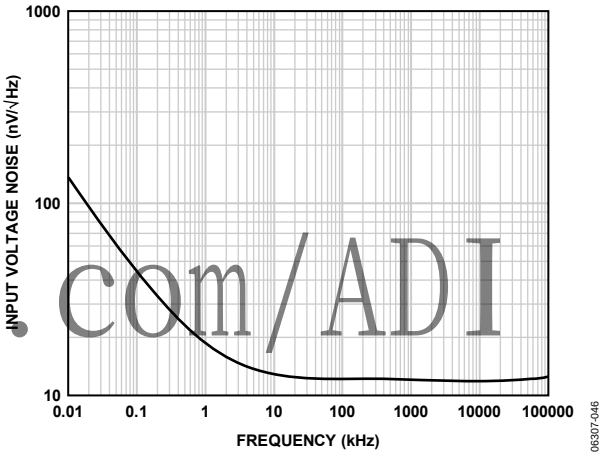


Figure 14. Input Referred Voltage Noise vs. Frequency

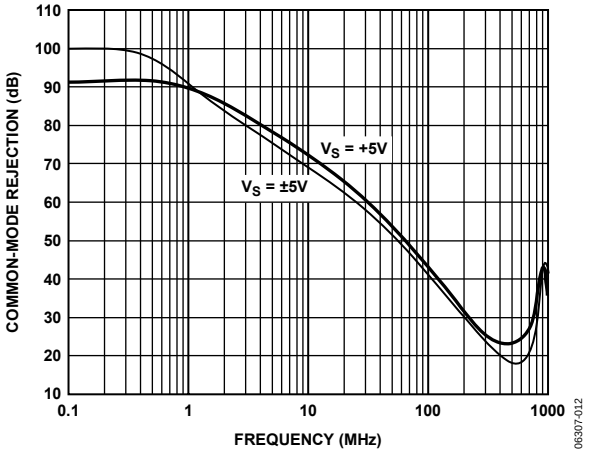


Figure 12. Common-Mode Rejection vs. Frequency at Various Supplies

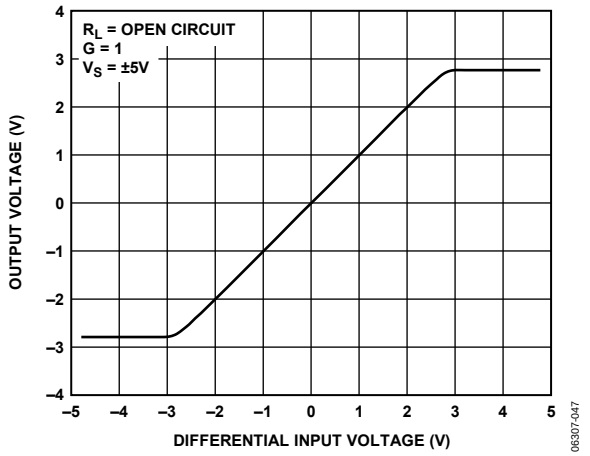


Figure 15. Differential Input Operating Range

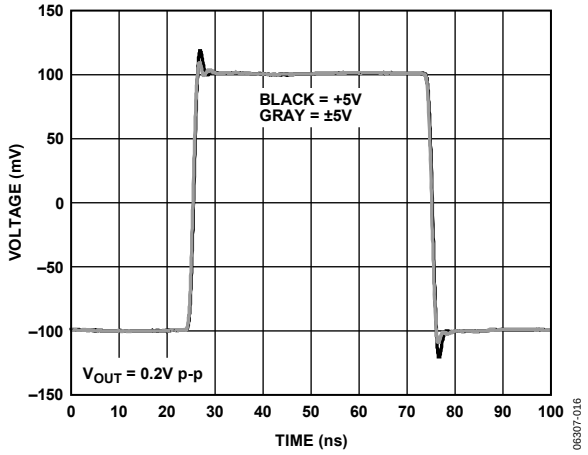


Figure 16. Small Signal Transient Response at Various Power Supplies, G = 1

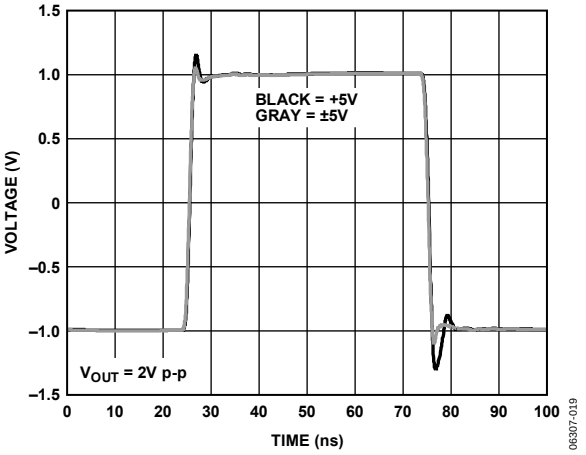


Figure 19. Large Signal Transient Response at Various Power Supplies, G = 1

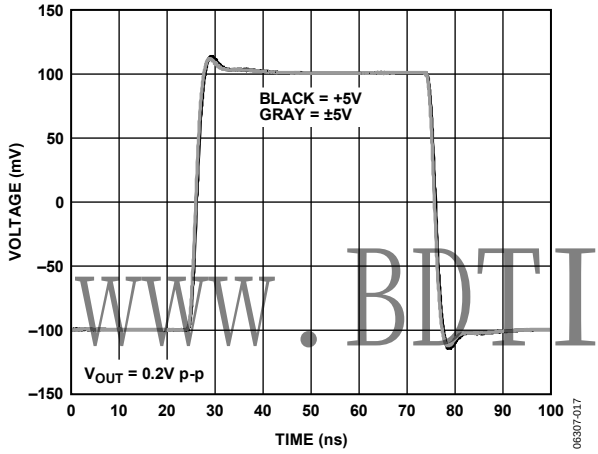


Figure 17. Small Signal Transient Response at Various Power Supplies, G = 2

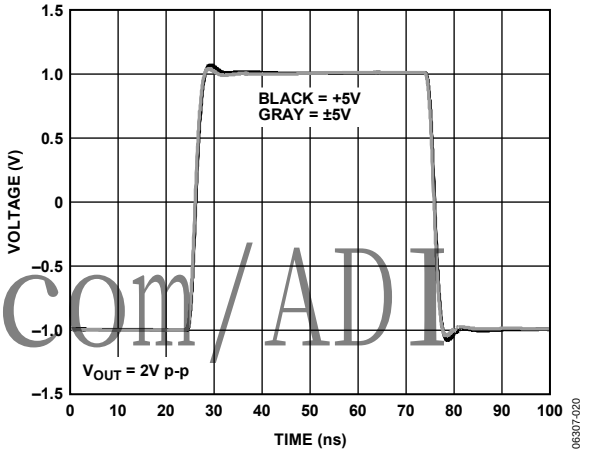


Figure 20. Large Signal Transient Response at Various Power Supplies, G = 2

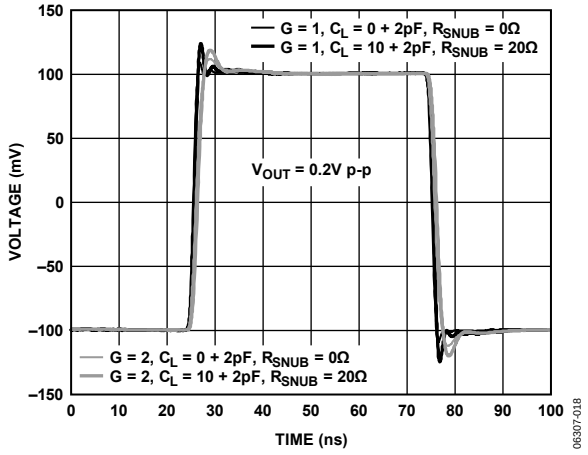


Figure 18. Small Signal Transient Response at Various Gains and 10 pF Capacitive Load Buffered by 20 Ω Resistor

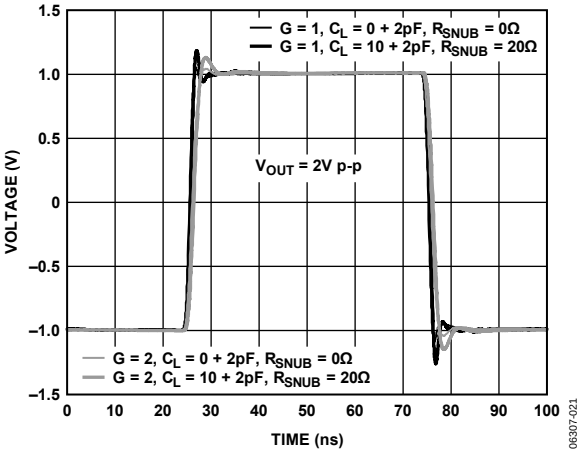


Figure 21. Large Signal Transient Response at Various Gains and 10 pF Capacitive Load Buffered by 20 Ω Resistor

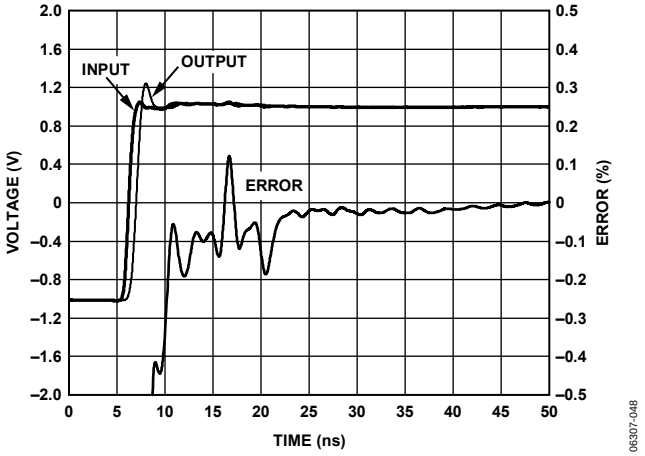


Figure 22. Settling Time

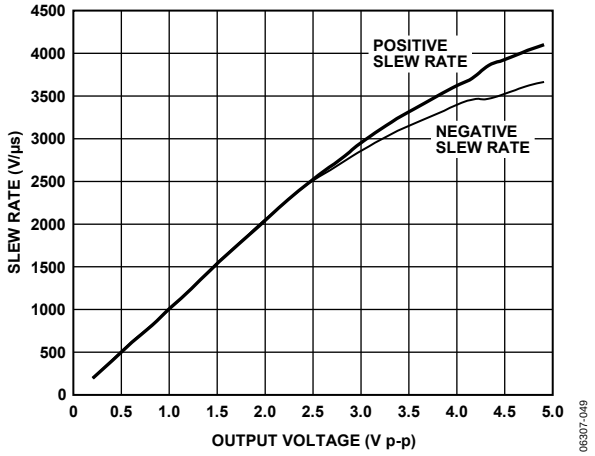


Figure 25. Slew Rate vs. Input Voltage Swing

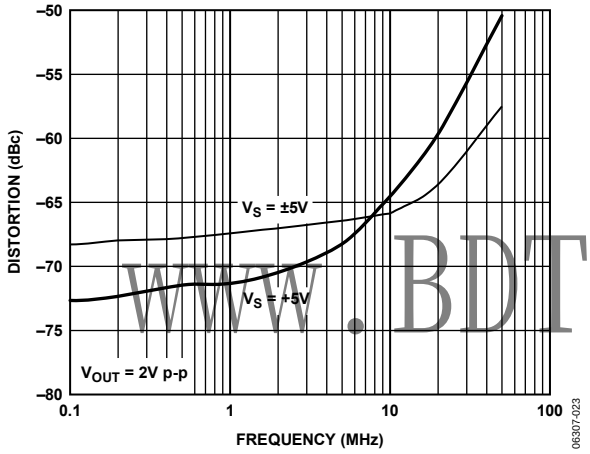


Figure 23. Second Harmonic Distortion vs. Frequency and Power Supplies, V_O = 2 V p-p, G = 1

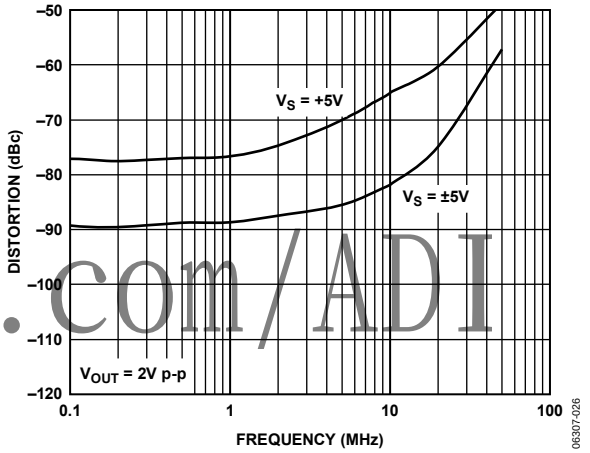


Figure 26. Third Harmonic Distortion vs. Frequency and Power Supplies, V_O = 2 V p-p, G = 1

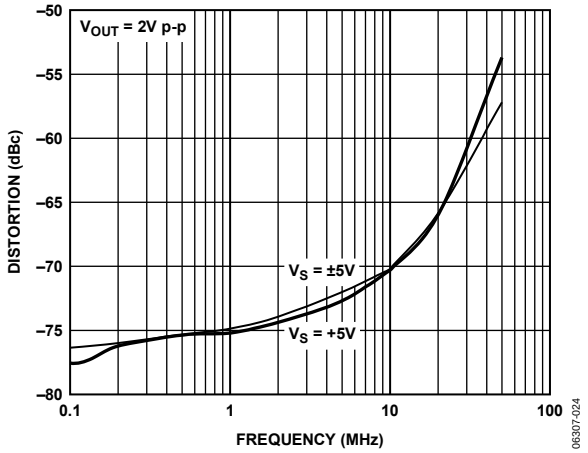


Figure 24. Second Harmonic Distortion vs. Frequency and Power Supplies, V_O = 2 V p-p, G = 2

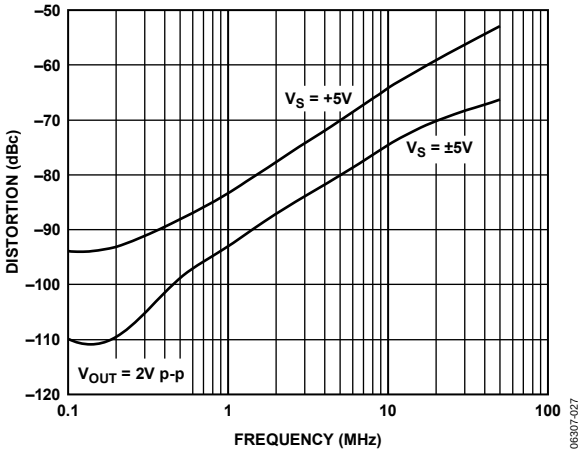


Figure 27. Third Harmonic Distortion vs. Frequency and Power Supplies, V_O = 2 V p-p, G = 2

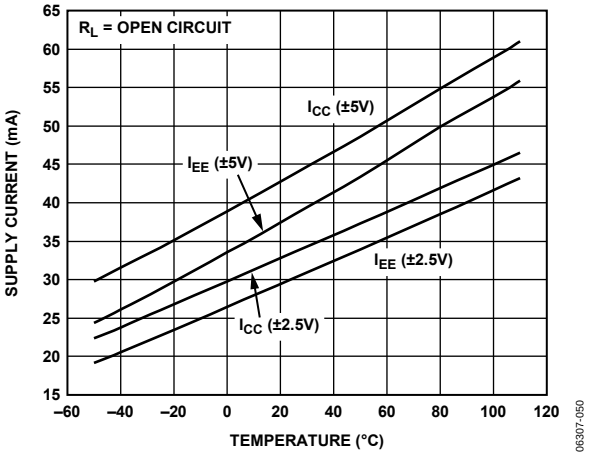


Figure 28. Power Supply Current vs. Temperature

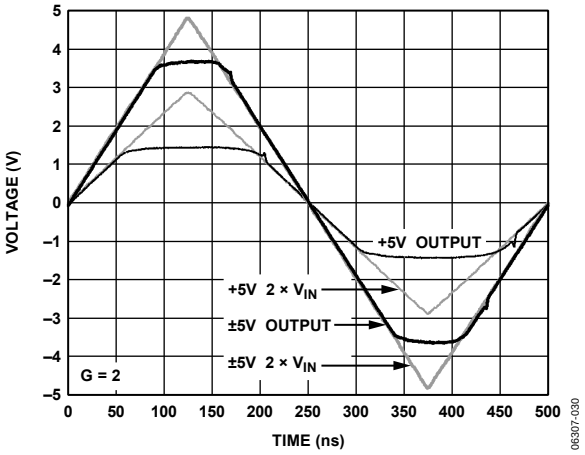


Figure 31. Output Overdrive Recovery

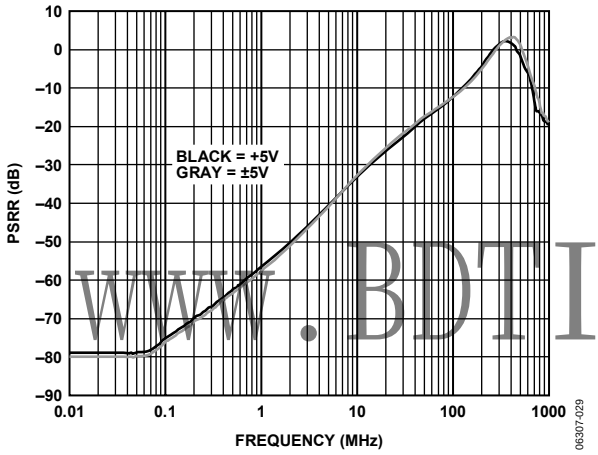


Figure 29. Positive Power Supply Rejection Ratio vs. Frequency

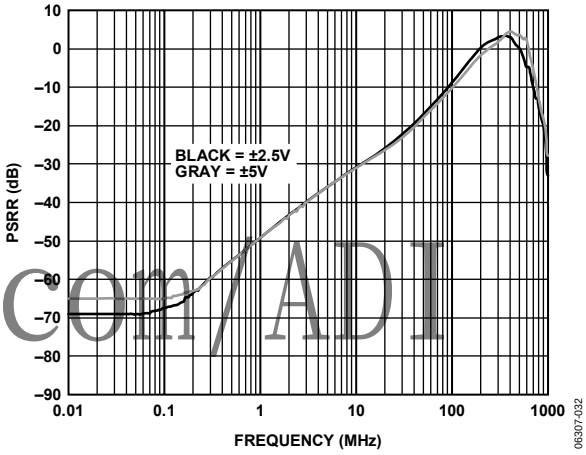


Figure 32. Negative Power Supply Rejection Ratio vs. Frequency

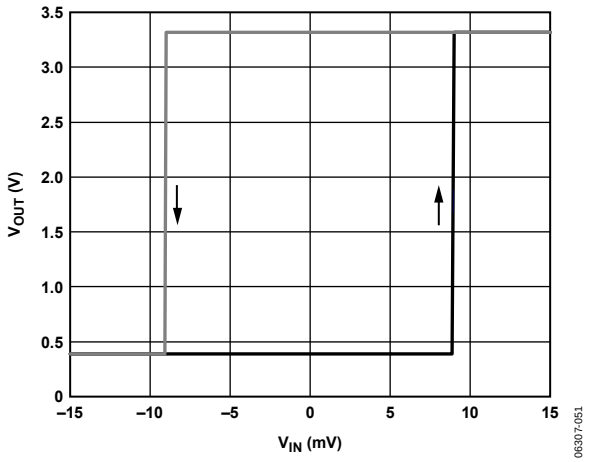


Figure 30. Comparator Hysteresis

THEORY OF OPERATION

The AD8145 amplifiers use an architecture called active feedback, which differs from that of conventional op amps. The most obvious differentiating feature is the presence of two separate pairs of differential inputs compared to a conventional op amp's single pair. Typically, for the active-feedback architecture, one of these input pairs is driven by a differential input signal, while the other is used for the feedback. This active stage in the feedback path is where the term active feedback is derived. The AD8145 has an internal feedback resistor from each amplifier output to the negative input of its feedback input stage. This limits the possible closed-loop gain configurations for the AD8145.

The active feedback architecture offers several advantages over a conventional op amp in several types of applications. Among these are excellent common-mode rejection, wide input common-mode range, and a pair of inputs that are high impedance and completely balanced in a typical application. In addition, while an external feedback network establishes the gain response as in a conventional op amp, its separate path makes it entirely independent of the signal input. This eliminates any interaction between the feedback and input circuits, which traditionally causes problems with CMRR in conventional differential-input op amp circuits.

Another advantage of active feedback is the ability to change the polarity of the gain merely by switching the differential inputs. A high input impedance inverting amplifier can therefore be made. Besides high input impedance, a unity-gain inverter with the AD8145 has noise gain of unity, producing lower output noise and higher bandwidth than op amps that have noise gain equal to 2 for a unity-gain inverter.

The two differential input stages of the AD8145 are each transconductance stages that are well matched. These stages convert the respective differential input voltages to internal currents. The currents are then summed and converted to a voltage, which is buffered to drive the output. The compensation capacitor is included in the summing circuit. When the feedback path is closed around the part, the output drives the feedback input to that voltage which causes the internal currents to sum to zero. This occurs when the two differential inputs are equal and opposite; that is, their algebraic sum is zero.

In a closed-loop application, a conventional op amp has its differential input voltage driven to near zero under non-transient conditions. The AD8145 generally has differential input voltages at each of its input pairs, even under equilibrium conditions. As a practical consideration, it is necessary to internally limit the differential input voltage with a clamp circuit. Thus, the input dynamic ranges are limited to about 2.5 V for the AD8145 (see the Specifications section for more detail). For this and other reasons, it is not recommended to reverse the input and feedback stages of the AD8145, even though some apparently normal functionality may be observed under some conditions.

APPLICATIONS

OVERVIEW

The AD8145 contains three independent active feedback amplifiers that can be effectively applied as differential line receivers for red-green-blue (RGB) signals or component video signals, such as YPbPr, transmitted over unshielded twisted pair (UTP) cable. The AD8145 also contains two general-purpose comparators with hysteresis that can be used to receive digital signals or to extract video synchronization pulses from received common-mode signals that contain encoded synchronization signals.

The comparators, which receive power from the positive supply, are referenced to GND and require greater than 4.5 V on the positive supply for proper operation. If the comparators are not used, then a split ±2.5 V can be used with the amplifiers operating normally.

The AD8145 includes a power-down feature that can be asserted to reduce the supply current when a particular device is not in use.

BASIC CLOSED-LOOP GAIN CONFIGURATIONS

Each amplifier in the AD8145 comprises two transconductance amplifiers—one for the input signal and one for negative feedback. It is important to note that the closed-loop gain of the amplifier used in the signal path is defined as the single-ended output voltage of the amplifier divided by its differential input voltage. Therefore, each amplifier in the AD8145 provides differential-to-single-ended gain. Additionally, the amplifier used for feedback has two high impedance inputs—the feedback input, where the negative feedback is applied, and the REF input, which can be used as an independent single-ended input to apply a dc offset to the output signal.

The AD8145 contains on-chip feedback networks between each amplifier output and its respective feedback input. Closed-loop gain of an amplifier is set to 1 by connecting the amplifier output directly to its respective GAIN pin. Doing this places the on-chip resistors and capacitor in parallel across the amplifier output and feedback pin. The small feedback capacitor mitigates the effects of summing-node capacitance, which is most problematic in the unity gain case. Closed-loop gain of an amplifier is set to 2 by connecting the respective GAIN pin to a reference voltage, often directly to ground. In Figure 1, R = 350 Ω and C = 2 pF.

Some basic gain configurations implemented with an AD8145 amplifier are shown in Figure 33 through Figure 36.

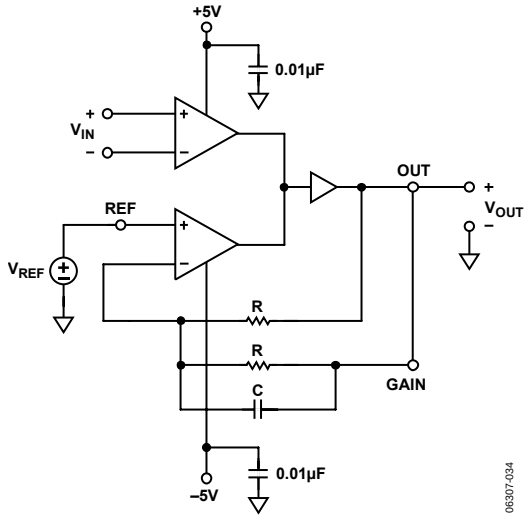


Figure 33. Basic Gain = 1 Circuit: $V_{OUT} = V_{IN} + V_{REF}$

The gain equation for the circuit in Figure 33 is

$$V_{OUT} = V_{IN} + V_{REF} \quad (1)$$

In this configuration, the voltage applied to the REF pin appears at the output with a gain of 1.

Figure 34 illustrates one way to operate an AD8145 amplifier with a gain of 2.

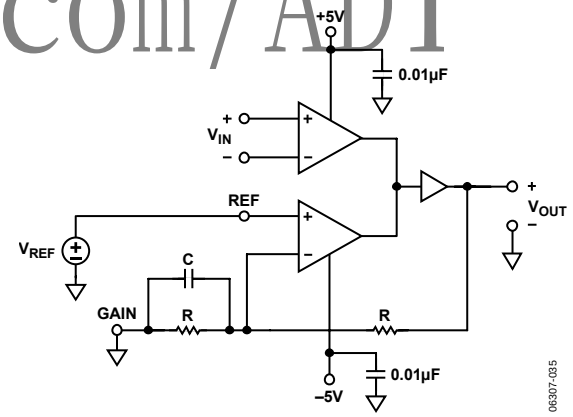


Figure 34. Basic Gain = 2 Circuit: $V_{OUT} = 2(V_{IN} + V_{REF})$

The gain equation for the circuit in Figure 34 is

$$V_{OUT} = 2(V_{IN} + V_{REF}) \quad (2)$$

To achieve unity gain from V_{REF} to V_{OUT} in this configuration, divide V_{REF} by the same factor used in the feedback loop; the divider resistors, R_D, need not be the same values used in the internal feedback loop. Figure 35 illustrates this approach.

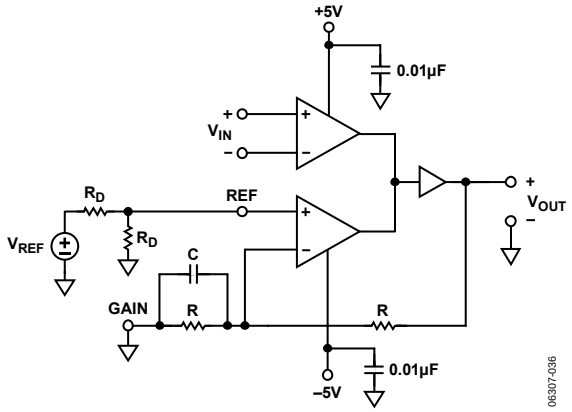


Figure 35. Basic Gain Circuit: $V_{OUT} = 2V_{IN} + V_{REF}$

The gain equation for the circuit in Figure 35 is

$$V_{OUT} = 2V_{IN} + V_{REF} \quad (3)$$

Another configuration that provides the same gain equation as Equation 3 is shown in Figure 36. In this configuration, it is important to keep the source resistance of V_{REF} much smaller than 350 Ω to avoid gain errors.

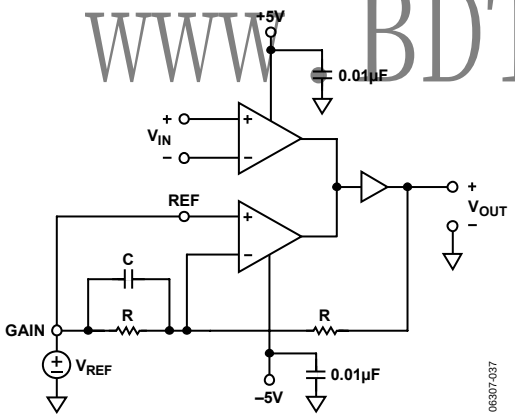


Figure 36. Basic Gain Circuit: $V_{OUT} = 2V_{IN} + V_{REF}$

For stability reasons, the inductance of the trace connected to the REF pin must be kept to less than 10 nH. The typical inductance of 50 Ω traces on the outer layers of the FR-4 boards is 7 nH/in, and on the inner layers, it is typically 9 nH/in. Vias must be accounted for as well. The inductance of a typical via in a 0.062 inch board is on the order of 1.5 nH. If longer traces are required, a 200 Ω resistor should be placed in series with the trace to reduce the Q-factor of the inductance.

In many dual-supply applications, V_{REF} can be directly connected to ground right at the device.

TERMINATING THE INPUT

One of the key benefits of the active feedback architecture is the separation that exists between the differential input signal and the feedback network. Because of this separation, the differential input maintains its high CMRR and provides high differential and common-mode input impedances, making line termination a simple task.

Most applications that use the AD8145 involve transmitting broadband video signals over 100 Ω UTP cable and use dc-coupled terminations. The two most common types of dc-coupled terminations are differential and common-mode. Differential termination of 100 Ω UTP is implemented by simply connecting a 100 Ω resistor across the amplifier input, as shown in Figure 37.

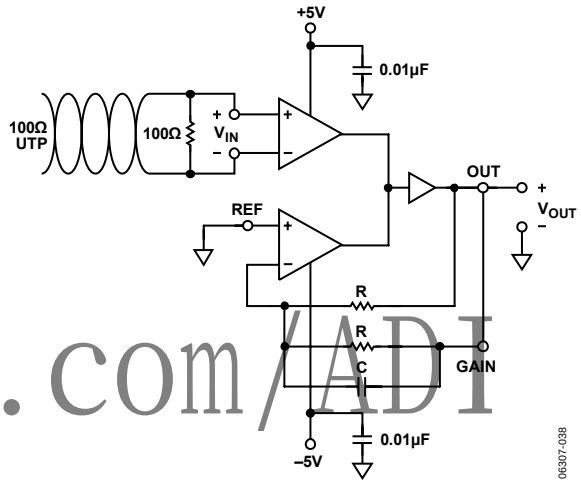


Figure 37. Differential-Mode Termination with G = 1

Some applications require common-mode terminations for common-mode currents generated at the transmitter. In these cases, the 100 Ω termination resistor is split into two 50 Ω resistors. The required common-mode termination voltage is applied at the tap between the two resistors. In many of these applications, the common-mode tap is connected to ground (V_{TERM} (CM) = 0). This scheme is illustrated in Figure 38.

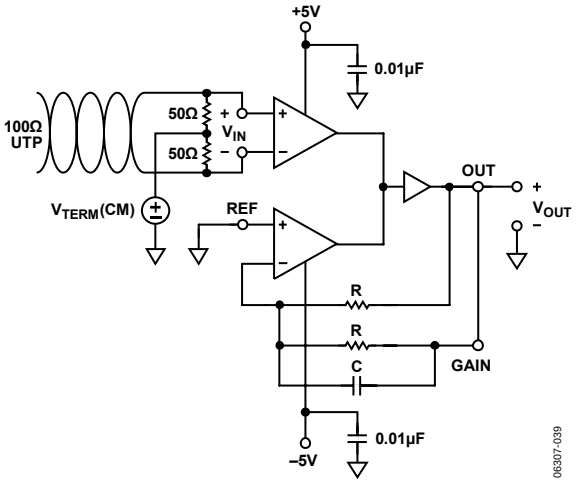


Figure 38. Common-Mode Termination with G = 1

INPUT CLAMPING

The differential input that is assigned to receive the input signal includes clamping diodes that limit the differential input swing to approximately 5.5 V p-p at 25°C. Because of this, the input and feedback stages should never be interchanged.

The supply current drawn by the AD8145 has a strong dependence on input signal magnitude because the input transconductance stages operate with differential input signals that can be up to a few volts peak-to-peak. This behavior is distinctly different from that of traditional op amps, where the differential input signal is driven to essentially 0 V by negative feedback.

For most applications, including receiving RGB video signals, the input signal magnitudes encountered are well within the safe operating limits of the AD8145 over its full power supply and operating temperature ranges. In some extreme applications where large differential and/or common-mode voltages are encountered, external clamping may be necessary. Another application in which external common-mode clamping is sometimes required is when an unpowered AD8145 receives a signal from an active driver. In this case, external diodes are required when the current drawn by the internal ESD diodes cannot be kept to less than 5 mA.

Figure 39 shows a general approach to external differential-mode clamping.

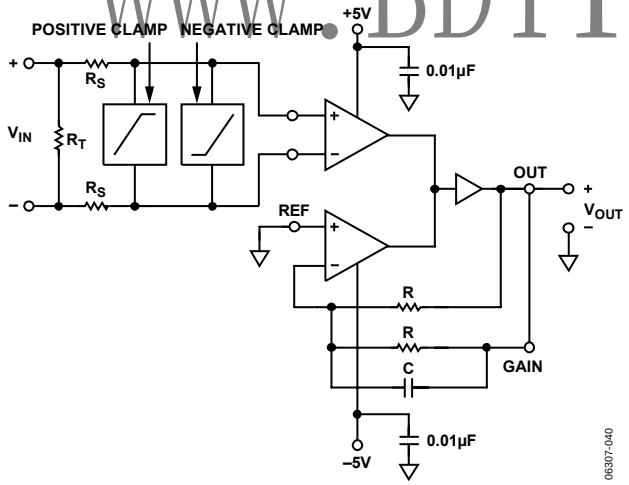


Figure 39. Differential-Mode Clamping with G = 1

The positive and negative clamps are nonlinear devices that exhibit very low impedance when the voltage across them reaches a critical threshold (clamping voltage), thereby limiting the voltage across the AD8145 input. The positive clamp has a positive threshold, and the negative clamp has a negative threshold.

A diode is a simple example of such a clamp. Schottky diodes generally have lower clamping voltages than typical signal diodes. The clamping voltage should be larger than the largest expected signal amplitude, with enough margin to ensure that the received signal passes without being distorted.

A simple way to implement a clamp is to use a number of diodes in series. The resultant clamping voltage is then the sum of the clamping voltages of individual diodes.

A 1N4448 diode has a forward voltage of approximately 0.70 V to 0.75 V at typical current levels that are seen when it is being used as a clamp, and 2 pF maximum capacitance at 0 V bias. (The capacitance of a diode decreases as its reverse bias voltage is increased.) The series connection of two 1N4448 diodes, therefore, has a clamping voltage of 1.4 V to 1.5 V. Figure 40 shows how to limit the differential input voltage applied to an AD8145 amplifier to ±1.4 V to ±1.5 V (2.8 V p-p to 3.0 V p-p). Note that the capacitance of the two series diodes is half that of one diode. Different numbers of series diodes can be used to obtain different clamping voltages.

R_T is the differential termination resistor, and the series resistances, R_S, limit the current into the diodes. The series resistors should be highly matched in value to preserve high frequency CMRR.

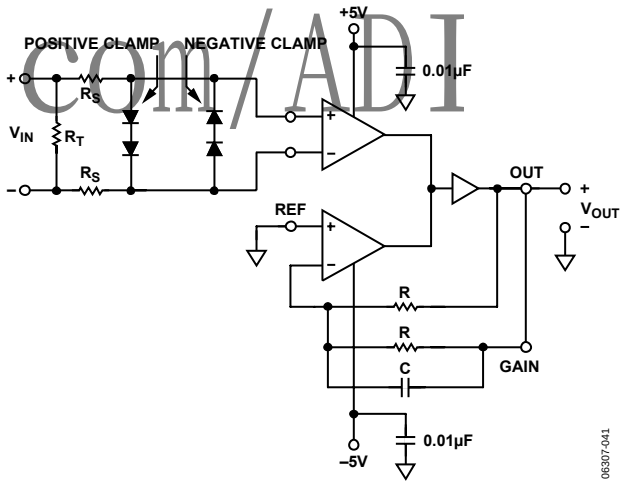


Figure 40. Using Two 1N4448 Diodes in Series as a Clamp

There are many other nonlinear devices that can be used as clamps. The best choice for a particular application depends upon the desired clamping voltage, response time, parasitic capacitance, and other factors.

When using external differential-mode clamping, it is important to ensure that the series resistors (R_S), the sum of the parasitic capacitance of the clamping devices, and the input capacitance of the AD8145 are small enough to preserve the desired signal bandwidth.

Figure 41 shows a specific example of external common-mode clamping.

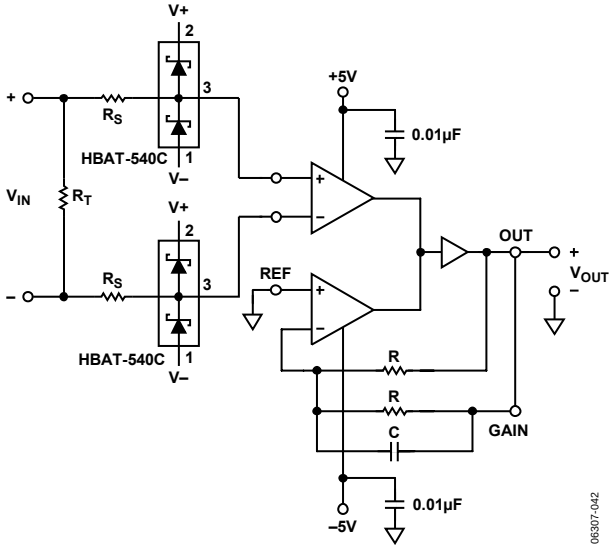


Figure 41. External Common-Mode Clamping

The series resistances, R_S, limit the current in each leg, and the Schottky diodes limit the voltages on each input to approximately 0.3 V to 0.4 V over the positive power supply, V+, and to 0.3 V to 0.4 V below the negative power supply, V−. The maximum value of R_S is determined by the required signal bandwidth, the line impedance, and the effective differential capacitance due to the AD8145 inputs and the diodes.

As with the differential clamp, the series resistors should be highly matched in value to preserve high frequency CMRR.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The two most important issues with regard to printed circuit board (PCB) layout are minimizing parasitic signal trace reactances in the feedback network and providing sufficient thermal relief.

Excessive parasitic reactances in the feedback network cause excessive peaking in the frequency response of the amplifier and excessive overshoot in its step response due to a reduction in phase margin. Oscillation occurs when these parasitic reactances are increased to a critical point where the phase margin is reduced to zero. Minimizing these reactances is important to obtain optimal performance from the AD8145. General high speed layout practices should be adhered to when applying the AD8145. Controlled impedance transmission lines are required for incoming and outgoing signals, referenced to a ground plane.

Typically, the input signals are received over 100 Ω differential transmission lines. A 100 Ω differential transmission line is readily realized on the printed circuit board using two well-matched, closely-spaced, 50 Ω single-ended traces that are coupled through the ground plane. The traces that carry the single-ended output signals are most often 75 Ω for video signals. Output signal connections should include series termination resistors that are matched to the impedance of the line they are driving. When driving high impedance loads over very short traces, impedance matching is not required. In these cases, small series resistors should be used to buffer the capacitance presented by the load.

Broadband power supply decoupling networks should be placed as close as possible to the supply pins. Small surface-mount ceramic capacitors are recommended for these networks, and tantalum capacitors are recommended for bulk supply decoupling.

Minimizing Parasitic Feedback Reactances

Parasitic trace capacitance and inductance are both reduced in the unity-gain configuration when the feedback trace that connects the OUT pin to the GAIN pin is reduced in length. Removing the copper from all planes below the trace reduces trace capacitance, but increases trace inductance, since the loop area formed by the trace and ground plane is increased. A reasonable compromise that works well is to void all copper directly under the feedback trace and component pads with margins on each side approximately equal to one trace width. Combining this technique with minimizing trace length is effective in keeping parasitic trace reactance in the unity-gain feedback loop to a minimum.

Maximizing Heat Removal

A 5 × 5 array of thermal vias works well to connect the exposed paddle to internal ground planes. The vias should be placed inside the PCB pad that is soldered to the exposed paddle, and should connect to all ground planes.

The AD8145 includes ground connections on its corner pins. These pins can be used to provide additional heat removal from the AD8145 by connecting them between the PCB pad that is soldered to the exposed paddle and a ground plane on the component side of the board. This layout technique lowers the overall package thermal resistance. Use of this technique is not required, but it does result in a lower junction temperature. Designs must often conform to design for manufacturing (DFM) rules that stipulate how to lay out PCBs in such a way as to facilitate the manufacturing process. Some of these rules require thermal relief on pads that connect to planes, and the rules may limit the extent to which this technique can be used.

DRIVING A CAPACITIVE LOAD

The AD8145 typically drives either high impedance loads over short PCB traces, such as crosspoint switch inputs, or doubly terminated coaxial cables. A gain of 1 is commonly used in the high impedance case since the 6 dB transmission line termination loss is not incurred. A gain of 2 is required when driving cables to compensate for the 6 dB termination loss.

In all cases, the output must drive the parasitic capacitance of the feedback loop, conservatively estimated to be 1 pF, in addition to the capacitance presented by the actual load. When driving a high impedance input, it is recommended that a small series resistor be used to buffer the input capacitance of the device being driven. Clearly, the resistor value must be small enough to preserve the required bandwidth. In the ideal doubly terminated cable case, the AD8145 output sees a purely resistive load. In reality, there is some residual capacitance, and this is buffered by the series termination resistor. Figure 42 illustrates the high impedance case, and Figure 43 illustrates the cable-driving case.

POWER-DOWN

The power-down feature is intended to be used to reduce power consumption when a particular device is not in use, and does not place the output in a high-Z state when asserted. The power-down feature is asserted when the voltage applied to the power-down pin drops to approximately 2 V below the positive supply. The AD8145 is enabled by pulling the power-down pin to the positive supply.

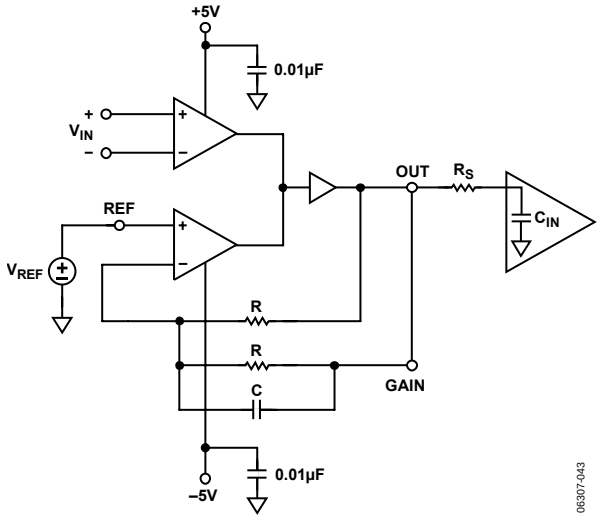


Figure 42. Buffering the Input Capacitance of a High-Z Load with G = 1

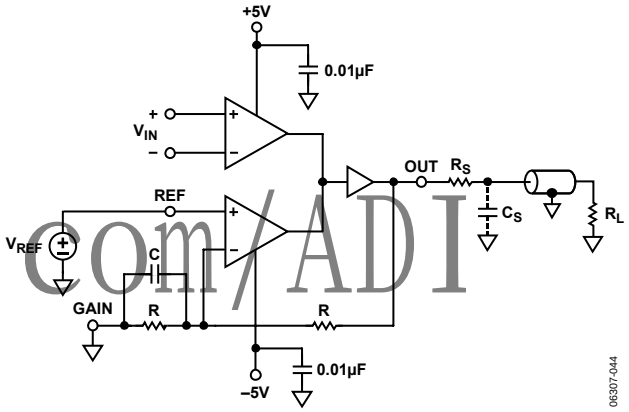


Figure 43. Driving a Doubly Terminated Cable with G = 2

COMPARATORS

In addition to general-purpose applications, the two on-chip comparators can be used to decode video sync pulses from the received common-mode voltages, or to receive differential digital information. Built-in hysteresis helps to eliminate false triggers from noise.

The comparator outputs are designed to drive source-terminated transmission lines. The source termination technique uses a resistor in series with each comparator output such that the sum of the comparator source resistance (≈ 20 Ω) and the series resistor equals the transmission line characteristic impedance. The load end of the transmission line is high impedance. When the signal is launched into the source termination, its initial value is one-half of its source value, since its amplitude is divided by two by the voltage divider formed by the source termination and the transmission line. At the load, the signal experiences nearly 100% positive reflection due to the high impedance load, and is restored to nearly its full value. This technique is commonly used in PCB layouts that involve high speed digital logic.

An internal linear voltage regulator derives power for the comparators from the positive supply; therefore, the AD8145 must always have a minimum positive supply voltage of 4.5 V.

SYNC PULSE EXTRACTION USING COMPARATORS

The AD8145 is particularly useful in keyboard, video, mouse (KVM) applications. KVM networks transmit and receive computer video signals, which typically comprise red, green, and blue (RGB) video signals and separate horizontal and vertical sync signals. Because the sync signals are separate and not embedded in the color signals, it is advantageous to transmit them using a simple scheme that encodes them among the three common-mode voltages of the RGB signals. The AD8134 triple differential driver is a natural complement to the AD8145 and performs the sync pulse encoding with the necessary circuitry on-chip.

The AD8134 encoding equations are given in Equation 4, Equation 5, and Equation 6.

$$Red\ V_{CM} = \frac{K}{2}\left[V - H\right] \quad (4)$$

$$Green\ V_{CM} = \frac{K}{2}\left[-2\ \mathrm{V}\right] \quad (5)$$

$$Blue\ V_{CM} = \frac{K}{2}\left[V + H\right] \quad (6)$$

where:

Red V_{CM}, *Green* V_{CM}, and *Blue* V_{CM} are the transmitted common-mode voltages of the respective color signals.

K is an adjustable gain constant that is set by the AD8134.

V and *H* are the vertical and horizontal sync pulses, defined with a weight of −1 when the pulses are in their low states, and a weight of +1 when they are in their high states.

The AD8134 data sheet contains further details regarding the encoding scheme. Figure 44 illustrates how the AD8145 comparators can be used to extract the horizontal and vertical sync pulses that are encoded on the RGB common-mode voltages by the AD8134.

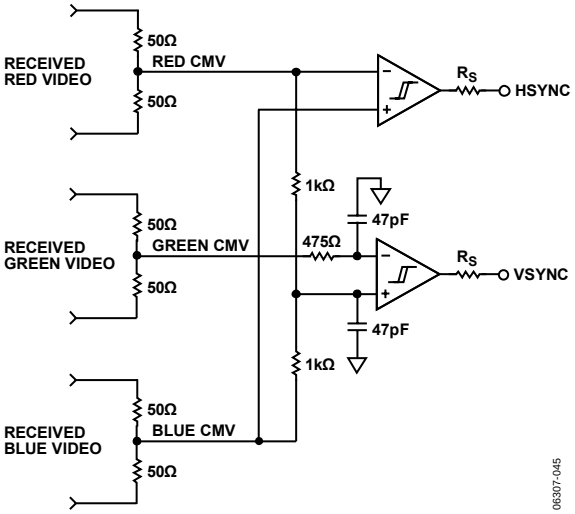
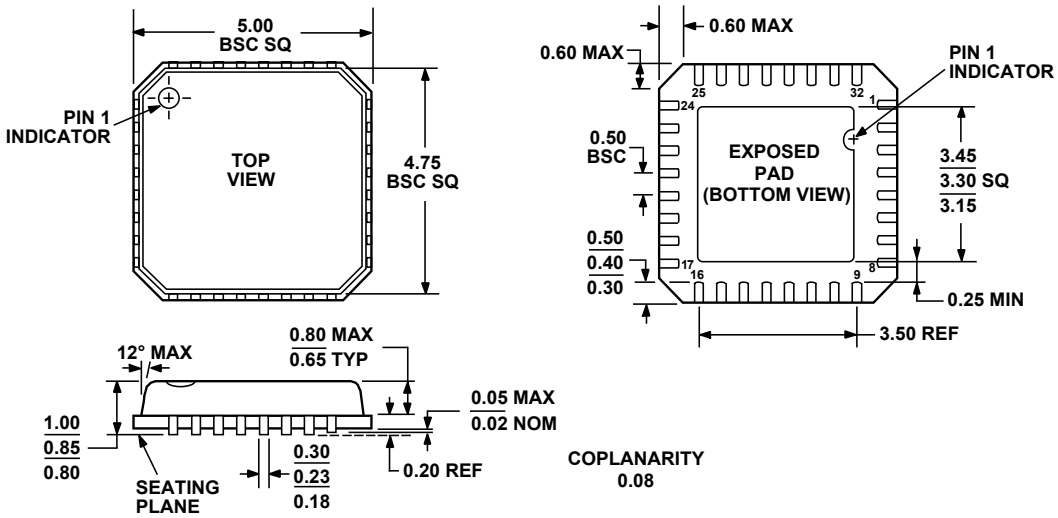


Figure 44. Extracting Sync Signals from Received Common-Mode Signal

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 45. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8145YCPZ-R2[1]	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
AD8145YCPZ-RL[1]	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3
AD8145YCPZ-R7[1]	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-3

[1] Z = Pb-free part.

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