Fiber Optic Receiver with Quantizer and Clock Recovery and Data Retiming

AD808

FEATURES

Meets CCITT G.958 Requirements for STM-4 Regenerator—Type A
Meets Bellcore TR-NWT-000253 Requirements for OC-12
Output Jitter: 2.5 Degrees RMS
622 Mbps Clock Recovery and Data Retiming
Accepts NRZ Data, No Preamble Required
Phase-Locked Loop Type Clock Recovery—No Crystal Required
Quantizer Sensitivity: 4 mV
Level Detect Range: 10 mV to 40 mV, Programmable
Single Supply Operation: +5 V or –5.2 V
Low Power: 400 mW
10 KH ECL/PECL Compatible Output
Package: 16-Lead Narrow 150 mil SOIC

PRODUCT DESCRIPTION

The AD808 provides the receiver functions of data quantization, signal level detect, clock recovery and data retiming for 622 Mbps NRZ data. The device, together with a PIN diode/preamplifier combination, can be used for a highly integrated, low cost, low power SONET OC-12 or SDH STM-4 fiber optic receiver.

The receiver front end signal level detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The threshold is set with a single external resistor. The signal level detect circuit 3 dB optical hysteresis prevents chatter at the signal level detect output.

The PLL has a factory trimmed VCO center frequency and a frequency acquisition control loop that combine to guarantee frequency acquisition without false lock. This eliminates a reliance on external components such as a crystal or a SAW filter, to aid frequency acquisition.

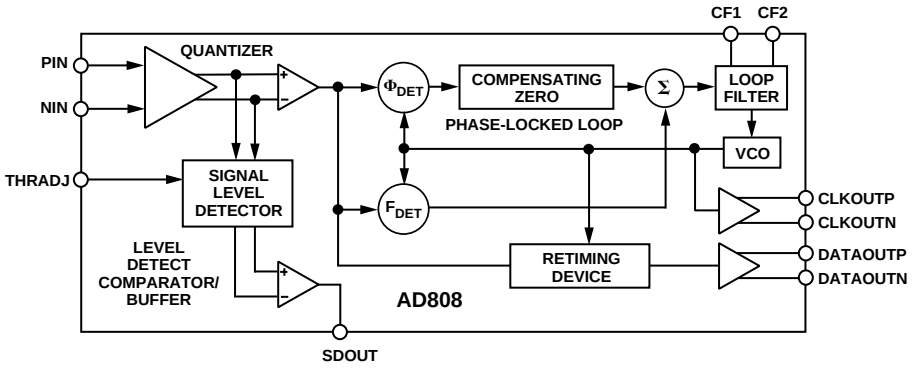
The AD808 acquires frequency and phase lock on input data using two control loops that work without requiring external control. The frequency acquisition control loop initially acquires the frequency of the input data, acquiring frequency lock on random or scrambled data without the need for a preamble. At frequency lock, the frequency error is zero and the frequency detector has no further effect. The phase acquisition control loop then works to ensure that the output phase tracks the input phase. A patented phase detector has virtually eliminated pattern jitter throughout the AD808.

The device VCO uses a ring oscillator architecture and patented low noise design techniques. Jitter is 2.5 degrees rms. This low jitter results from using a fully differential signal architecture, Power Supply Rejection Ratio circuitry and a dielectrically isolated process that provides immunity from extraneous signals on the IC. The device can withstand hundreds of millivolts of power supply noise without an effect on jitter performance.

The user sets the jitter peaking and acquisition time of the PLL by choosing a damping factor capacitor whose value determines loop damping. CCITT G.958 Type A jitter transfer requirements can easily be met with a damping factor of 5 or greater. Device design guarantees that the clock output frequency will drift by less than 20% in the absence of input data transitions. Shorting the damping factor capacitor, C_D, brings the clock output frequency to the VCO center frequency.

The AD808 consumes 400 mW and operates from a single power supply at either +5 V or –5.2 V.

FUNCTIONAL BLOCK DIAGRAM



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AD808–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_S = V_{MIN}$ to V_{MAX}, C_D = 0.47 µF, unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
QUANTIZER–DC CHARACTERISTICS					
Input Voltage Range	@ P_{IN} or N_{IN}	2.5		V_S	V
Input Sensitivity, V_{SENSE}	P_{IN}–N_{IN}, Figure 1, BER = ≤ 1×10^{-10}	10	4.0		mV
Input Overdrive, V_{OD}	Figure 1, BER = ≤ 1×10^{-10}	5	2.0		mV
Input Offset Voltage			1.0		mV
Input Current			10		µA
Input RMS Noise	BER = ≤ 1×10^{-10}		100		µV
Input Peak-to-Peak Noise	BER = ≤ 1×10^{-10}		1.5		mV
QUANTIZER–AC CHARACTERISTICS					
Upper –3 dB Bandwidth		600	800		MHz
Input Resistance			10		kΩ
Input Capacitance			2		pF
Pulsewidth Distortion			50		ps
LEVEL DETECT					
Level Detect Range	R_{THRESH} = 22.1 kΩ	6.5	10	13.5	mV
	R_{THRESH} = 6.98 kΩ	13	18	23	mV
	R_{THRESH} = 0 Ω	28.5	40	45.5	mV
Response Time	DC Coupled	0.1		1.5	µs
Hysteresis (Electrical)	R_{THRESH} = 22.1 kΩ (See Figure 8)		5	9.0	dB
	R_{THRESH} = 6.98 kΩ	3.0	5.1	9.0	dB
	R_{THRESH} = 0 Ω	3.0	7.0	10.0	dB
SDOUT Output Logic High	Load = +3.2 mA	4.0	4.7		V
SDOUT Output Logic Low	Load = –3.2 mA		0.2	0.4	V
PHASE-LOCKED LOOP NOMINAL CENTER FREQUENCY			622.08		MHz
CAPTURE RANGE		620		624	MHz
TRACKING RANGE		620		624	MHz
STATIC PHASE ERROR (See Figure 7)	2^7–1 PRN Sequence		22	81	Degrees
SETUP TIME (t_{SU})	Figure 2	550		900	ps
HOLD TIME (t_H)	Figure 2	700		1050	ps
PHASE DRIFT	240 Bits, No Transitions			50	Degrees
JITTER	2^7–1 PRN Sequence		2.5	3.6	Degrees rms
	2^{23}–1 PRN Sequence		2.5	3.6	Degrees rms
JITTER TOLERANCE	f = 30 Hz		3000		Unit Intervals
	f = 300 Hz	24	300		Unit Intervals
	f = 25 kHz	1.7	3.7		Unit Intervals
	f = 250 kHz	0.28	0.56		Unit Intervals
	f = 5 MHz	0.18	0.45		Unit Intervals
JITTER TRANSFER					
Peaking (Figure 14)	C_D = 0.47 µF		0.04		dB
Bandwidth			333	450	kHz
Acquisition Time					
C_D = 0.1 µF	2^{23}–1 PRN Sequence, T_A = +25°C		2×10^6	3×10^6	Bit Periods
C_D = 0.47 µF	V_{CC} = 5 V, V_{EE} = GND		8×10^6	12×10^6	Bit Periods
POWER SUPPLY VOLTAGE	V_{MIN} to V_{MAX}	4.5		5.5	Volts
POWER SUPPLY CURRENT	V_{CC} = 5.0 V, V_{EE} = GND, T_A = +25°C	55	80	100	mA
PECL OUTPUT VOLTAGE LEVELS					
Output Logic High, V_{OH}	T_A = +25°C	–1.2	–1.0	–0.7	Volts
Output Logic Low, V_{OL}	Referenced to V_{CC}	–2.2	–2.0	–1.7	Volts
SYMMETRY (Duty Cycle)	ρ = 1/2, T_A = +25°C,				
Recovered Clock Output, Pin 5	V_{CC} = 5 V, V_{EE} = GND	45		55	%
OUTPUT RISE / FALL TIMES					
Rise Time (t_R)	20%–80%	174	350	500	ps
Fall Time (t_F)	80%–20%	136	315	500	ps
CLOCK SKEW (t_{RCS})	Positive Number Indicates Clock Leading Data	–100	130	250	ps

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +8 V
Input Voltage (Pin 12 or Pin 13) . . . . . V_{CC} + 0.6 V
Maximum Junction Temperature . . . . . +165°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
ESD Rating (Human Body Model) . . . . . 1500 V

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics:

16-Lead Narrow Body SOIC Package: θ_{JA} = 110°C/Watt.

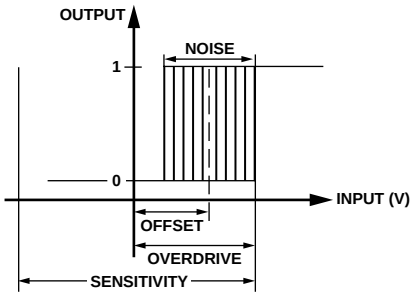


Figure 1. Input Sensitivity, Input Overdrive

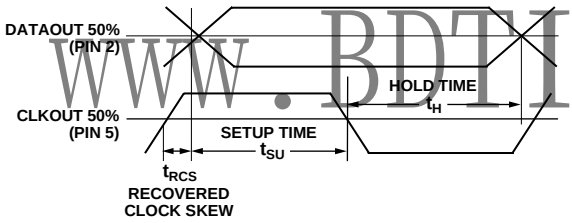
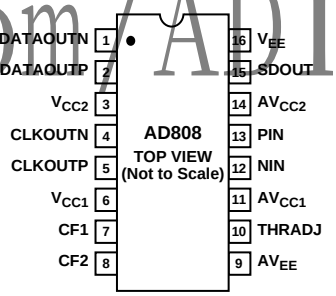


Figure 2. Setup and Hold Time

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	DATAOUTN	Differential Retimed Data Output
2	DATAOUTP	Differential Retimed Data Output
3	V_{CC2}	Digital V_{CC} for ECL Outputs
4	CLKOUTN	Differential Recovered Clock Output
5	CLKOUTP	Differential Recovered Clock Output
6	V_{CC1}	Digital V_{CC} for Internal Logic
7	CF1	Loop Damping Capacitor
8	CF2	Loop Damping Capacitor
9	AV_{EE}	Analog V_{EE}
10	THRADJ	Level Detect Threshold Adjust
11	AV_{CC1}	Analog V_{CC} for PLL
12	NIN	Quantizer Differential Input
13	PIN	Quantizer Differential Input
14	AV_{CC2}	Analog V_{CC} for Quantizer
15	SDOUT	Signal Detect Output
16	V_{EE}	Digital V_{EE} for Internal Logic

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD808-622BR	–40°C to +85°C	16-Pin Narrowbody SOIC	R-16A
AD808-622BRRL7	–40°C to +85°C	750 Pieces, 7" Reel	R-16A
AD808-622BRRL	–40°C to +85°C	2500 Pieces, 13" Reel	R-16A

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD808 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITION OF TERMS

Maximum, Minimum and Typical Specifications

Specifications for every parameter are derived from statistical analyses of data taken on multiple devices from multiple wafer lots. Typical specifications are the mean of the distribution of the data for that parameter. If a parameter has a maximum (or a minimum), that value is calculated by adding to (or subtracting from) the mean six times the standard deviation of the distribution. This procedure is intended to tolerate production variations: if the mean shifts by 1.5 standard deviations, the remaining 4.5 standard deviations still provide a failure rate of only 3.4 parts per million. For all tested parameters, the test limits are guard-banded to account for tester variation to thus guarantee that no device is shipped outside of data sheet specifications.

Input Sensitivity and Input Overdrive

Sensitivity and Overdrive specifications for the Quantizer involve offset voltage, gain and noise. The relationship between the logic output of the quantizer and the analog voltage input is shown in Figure 1.

For sufficiently large positive input voltage the output is always Logic 1 and similarly, for negative inputs, the output is always Logic 0. However, the transitions between output Logic Levels 1 and 0 are not at precisely defined input voltage levels, but occur over a range of input voltages. Within this Zone of Confusion, the output may be either 1 or 0, or it may even fail to attain a valid logic state. The width of this zone is determined by the input voltage noise of the quantizer (1.5 mV at the 1×10^{-10} confidence level). The center of the Zone of Confusion is the quantizer input offset voltage (1 mV typ). Input Overdrive is the magnitude of signal required to guarantee correct logic level with 1×10^{-10} confidence level.

With a single-ended PIN-TIA (Figure 3), ac coupling is used and the inputs to the Quantizer are dc biased at some common-mode potential. Observing the Quantizer input with an oscilloscope probe at the point indicated shows a binary signal with average value equal to the common-mode potential and instantaneous values both above and below the average value. It is convenient to measure the peak-to-peak amplitude of this signal and call the minimum required value the Quantizer Sensitivity. Referring to Figure 1, since both positive and negative offsets need to be accommodated, the Sensitivity is twice the Overdrive. The AD808 Quantizer has 4 mV Sensitivity typical.

With a differential TIA (Figure 3), Sensitivity seems to improve from observing the Quantizer input with an oscilloscope probe. This is an illusion caused by the use of a single-ended probe. A 2 mV peak-to-peak signal appears to drive the AD808 Quantizer. However, the single-ended probe measures only half the signal. The true Quantizer input signal is twice this value since the other Quantizer input is a complementary signal to the signal being observed.

Response Time

Response time is the delay between removal of the input signal and indication of Loss of Signal (LOS) at SDOUT. The response time of the AD808 (1.5 µs maximum) is much faster than the SONET/SDH requirement (3 µs ≤ response time ≤ 100 µs). In practice, the time constant of the ac coupling at the Quantizer input determines the LOS response time.

Nominal Center Frequency

This is the frequency at which the VCO will oscillate with the loop damping capacitor, C_D, shorted.

Tracking Range

This is the range of input data rates over which the AD808 will remain in lock.

Capture Range

This is the range of input data rates over which the AD808 will acquire lock.

Static Phase Error

This is the steady-state phase difference, in degrees, between the recovered clock sampling edge and the optimum sampling instant, which is assumed to be halfway between the rising and falling edges of a data bit. Gate delays between the signals that define static phase error, and IC input and output signals prohibit direct measurement of static phase error.

Data Transition Density, ρ

This is a measure of the number of data transitions, from "0" to "1" and from "1" to "0," over many clock periods. ρ is the ratio ($0 \le \rho \le 1$) of data transitions to bit periods.

Jitter

This is the dynamic displacement of digital signal edges from their long term average positions, measured in degrees rms or Unit Intervals (UI). Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

Output Jitter

This is the jitter on the retimed data, in degrees rms, due to a specific pattern or some pseudorandom input data sequence (PRN Sequence).

Jitter Tolerance

Jitter Tolerance is a measure of the AD808's ability to track a jittery input data signal. Jitter on the input data is best thought of as phase modulation, and is usually specified in unit intervals.

The PLL must provide a clock signal that tracks the phase modulation in order to accurately retime jittered data. In order for the VCO output to have a phase modulation that tracks the input jitter, some modulation signal must be generated at the output of the phase detector. The modulation output from the phase detector can only be produced by a phase error between its data input and its clock input. Hence, the PLL can never perfectly track jittered data. However, the magnitude of the phase error depends on the gain around the loop. At low frequencies, the integrator of the AD808 PLL provides very high gain, and thus very large jitter can be tracked with small phase errors between input data and recovered clock. At frequencies closer to the loop bandwidth, the gain of the integrator is much smaller, and thus less input jitter can be tolerated. The AD808 output will have a bit error rate less than 1×10^{-10} when in lock and retiming input data that has the CCITT G.958 specified jitter applied to it.

Jitter Transfer (Refer to Figure 14)

The AD808 exhibits a low-pass filter response to jitter applied to its input data.

Bandwidth

This describes the frequency at which the AD808 attenuates sinusoidal input jitter by 3 dB.

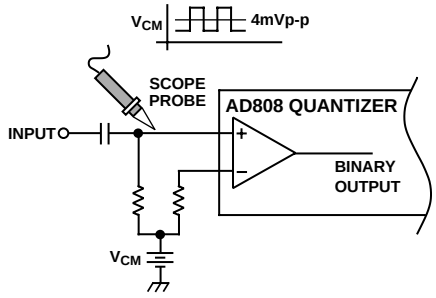
Peaking

This describes the maximum jitter gain of the AD808 in dB.

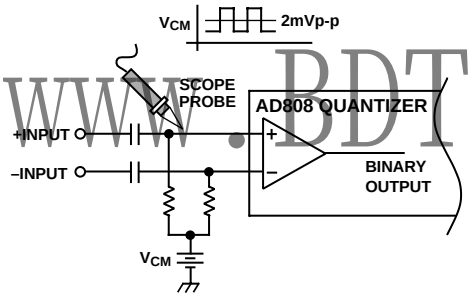
Damping Factor, ζ
Damping factor, ζ describes the compensation of the second order PLL. A larger value of ζ corresponds to more damping and less peaking in the jitter transfer function.

Acquisition Time
This is the transient time, measured in bit periods, required for the AD808 to lock onto input data from its free-running state.

Symmetry—Recovered Clock Duty Cycle
Symmetry is calculated as (100 × on time)/period, where on time equals the time that the clock signal is greater than the midpoint between its "0" level and its "1" level.



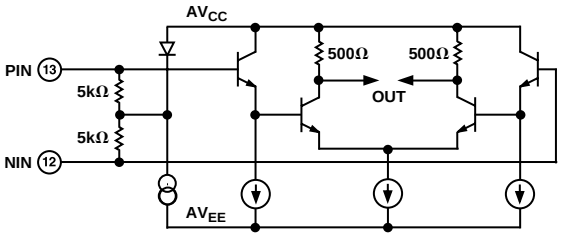
a. Single-Ended Input Application



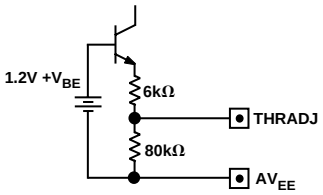
b. Differential Input Application

Figure 3. (a–b) Single-Ended and Differential Input Applications

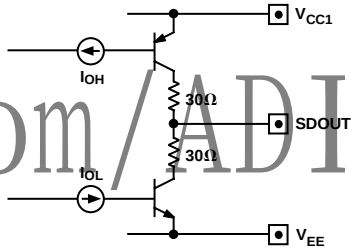
The AD808 has internal circuits to set the common-mode voltage at the quantizer inputs PIN (Pin 13) and NIN (Pin 12) as shown in Figure 4a. This allows very simple capacitive coupling of the signal from the preamp in the AD808 as shown in Figure 3. The internal common-mode potential is a diode drop (approximately 0.8 V) below the positive supply as shown in Figure 4a. Since the common mode is referred to the positive supply, it is useful to bypass the common mode of the preamp to the positive supply as well, if this is an option. Note, it is not necessary to use capacitive coupling of the input signal with the AD808. Figure 14 shows the input common-mode voltage can be externally set.



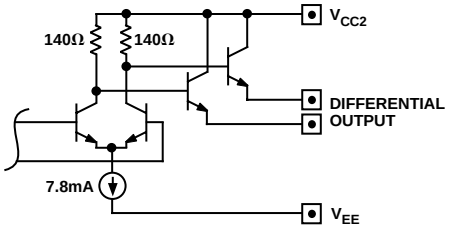
a. Quantizer Differential Input Stage



b. Threshold Adjust



c. Signal Detect Output (SDOUT)



d. PLL Differential Output Stage—DATAOUT(N), CLKOUT(N)

Figure 4. (a–d) Simplified Schematics

AD808–Typical Performance Characteristics

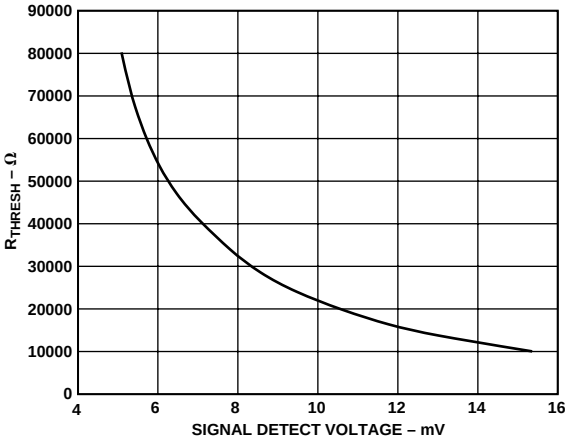


Figure 5. Signal Detect Voltage vs. R_{THRESH}

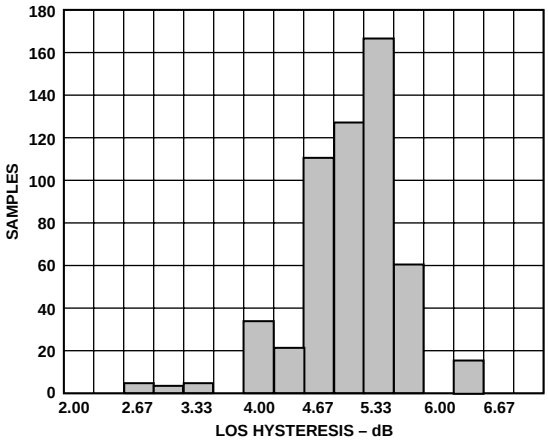


Figure 8. Histogram LOS Hysteresis 22.1 kΩ R_{THRESH} (All Temperature All Supply)

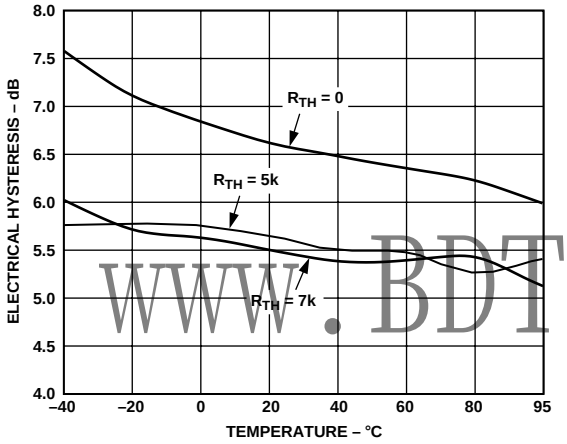


Figure 6. Signal Detect Hysteresis vs. Temperature

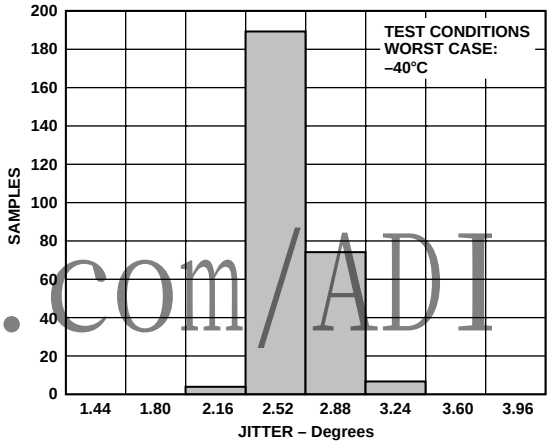


Figure 9. Output Jitter Histogram

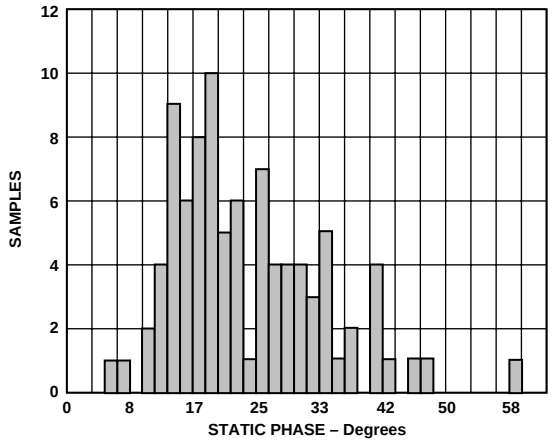


Figure 7. Histogram of Static Phase –40 @ 4.4 V

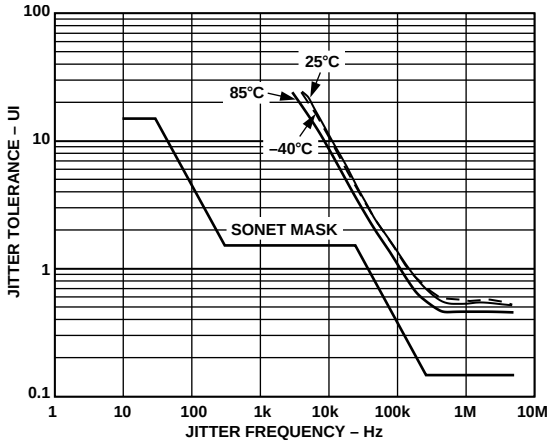


Figure 10. Jitter Tolerance vs. Frequency

THEORY OF OPERATION

Quantizer

The quantizer (comparator) has three gain stages, providing a net gain of 350. The quantizer takes full advantage of the Extra Fast Complementary Bipolar (XFCB) process. The input stage uses a folded cascode architecture to virtually eliminate pulse width distortion, and to handle input signals with common-mode voltage as high as the positive supply. The input offset voltage is factory trimmed and is typically less than 1 mV. XFCB's dielectric isolation allows the different blocks within this mixed-signal IC to be isolated from each other, hence the 4 mV Sensitivity is achieved. Traditionally, high speed comparators are plagued by crosstalk between outputs and inputs, often resulting in oscillations when the input signal approaches 10 mV. The AD808 quantizer toggles at 2 mV (4.0 mV sensitivity) at the input without making bit errors. When the input signal is lowered below 2 mV, circuit performance is dominated by input noise, and not crosstalk.

Signal Detect

The input to the signal detect circuit is taken from the first stage of the quantizer. The input signal is first processed through a gain stage. The output from the gain stage is fed to both a positive and a negative peak detector. The threshold value is subtracted from the positive peak signal and added to the negative peak signal. The positive and negative peak signals are then compared. If the positive peak, POS, is more positive than the negative peak, NEG, the signal amplitude is greater than the threshold, and the output, SDOUT, will indicate the presence of signal by remaining low. When POS becomes more negative than NEG, the signal amplitude has fallen below the threshold, and SDOUT will indicate a loss of signal (LOS) by going high. The circuit provides hysteresis by adjusting the threshold level higher by a factor of two when the low signal level is detected. This means that the input data amplitude needs to reach twice the set LOS threshold before SDOUT will signal that the data is again valid. This corresponds to a 3 dB optical hysteresis.

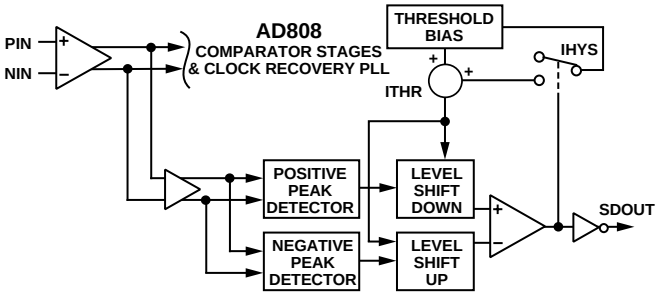


Figure 11. Signal Level Detect Circuit Block Diagram

Phase-Locked Loop

The phase-locked loop recovers clock and retimes data from NRZ data. The architecture uses a frequency detector to aid initial frequency acquisition; refer to Figure 12 for a block diagram. Note the frequency detector is always in the circuit. When the PLL is locked, the frequency error is zero and the frequency detector has no further effect. Since the frequency detector is always in the circuit, no control functions are needed to initiate acquisition or change mode after acquisition.

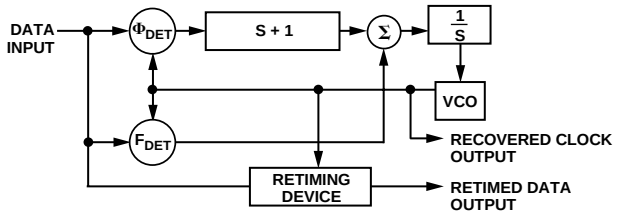


Figure 12. PLL Block Diagram

The frequency detector delivers pulses of current to the charge pump to either raise or lower the frequency of the VCO. During the frequency acquisition process the frequency detector output is a series of pulses of width equal to the period of the VCO. These pulses occur on the cycle slips between the data frequency and the VCO frequency. With a maximum density data pattern (1010 . . .), every cycle slip will produce a pulse at the frequency detector output. However, with random data, not every cycle slip produces a pulse. The density of pulses at the frequency detector output increases with the density of data transitions. The probability that a cycle slip will produce a pulse increases as the frequency error approaches zero. After the frequency error has been reduced to zero, the frequency detector output will have no further pulses. At this point the PLL begins the process of phase acquisition, with a settling time of roughly 2000 bit periods.

Jitter caused by variations of density of data transitions (pattern jitter) is virtually eliminated by use of a new phase detector (patented). Briefly, the measurement of zero phase error does not cause the VCO phase to increase to above the average run rate set by the data frequency. The jitter created by a 2^7–1 pseudorandom code is 1/2 degree, and this is small compared to random jitter.

The jitter bandwidth for the PLL is 0.06% of the center frequency. This figure is chosen so that sinusoidal input jitter at 350 Hz will be attenuated by 3 dB.

The damping ratio of the PLL is user programmable with a single external capacitor. At 622 MHz, a damping ratio of 5 is obtained with a 0.47 μF capacitor. More generally, the damping ratio scales as $(f_{DATA} \times C_D)^{1/2}$.

A lower damping ratio allows a faster frequency acquisition; generally the acquisition time scales directly with the capacitor value. However, at damping ratios approaching one, the acquisition time no longer scales directly with capacitor value. The acquisition time has two components: frequency acquisition and phase acquisition. The frequency acquisition always scales with capacitance, but the phase acquisition is set by the loop bandwidth of the PLL and is independent of the damping ratio. In practice the acquisition time is dominated by the frequency acquisition. The fractional loop bandwidth of 0.06% should give an acquisition time of 2000 bit periods. However, the actual acquisition time is several million bit periods and is comprised mostly of the time needed to slew the voltage on the damping capacitor to final value.

Center Frequency Clamp (Figure 13)

An N-channel FET circuit can be used to bring the AD808 VCO center frequency to within ±10% of 622 MHz when SDOUT indicates a Loss of Signal (LOS). This effectively reduces the frequency acquisition time by reducing the frequency error between the VCO frequency and the input data frequency at clamp release. The N-FET can have "on" resistance as high as 1 kΩ and still attain effective clamping. However, the chosen N-FET should have greater than 10 MΩ "off" resistance and less than 100 nA leakage current (source and drain) so as not to alter normal PLL performance.

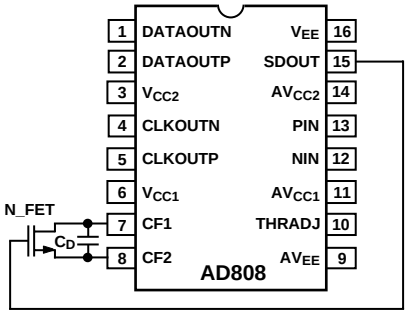


Figure 13. Center Frequency Clamp Schematic

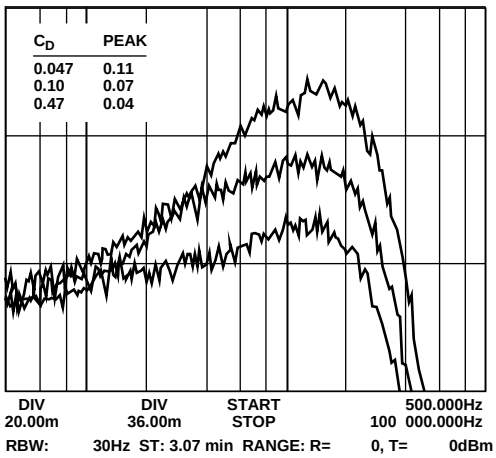


Figure14. Jitter Transfer vs. C_D

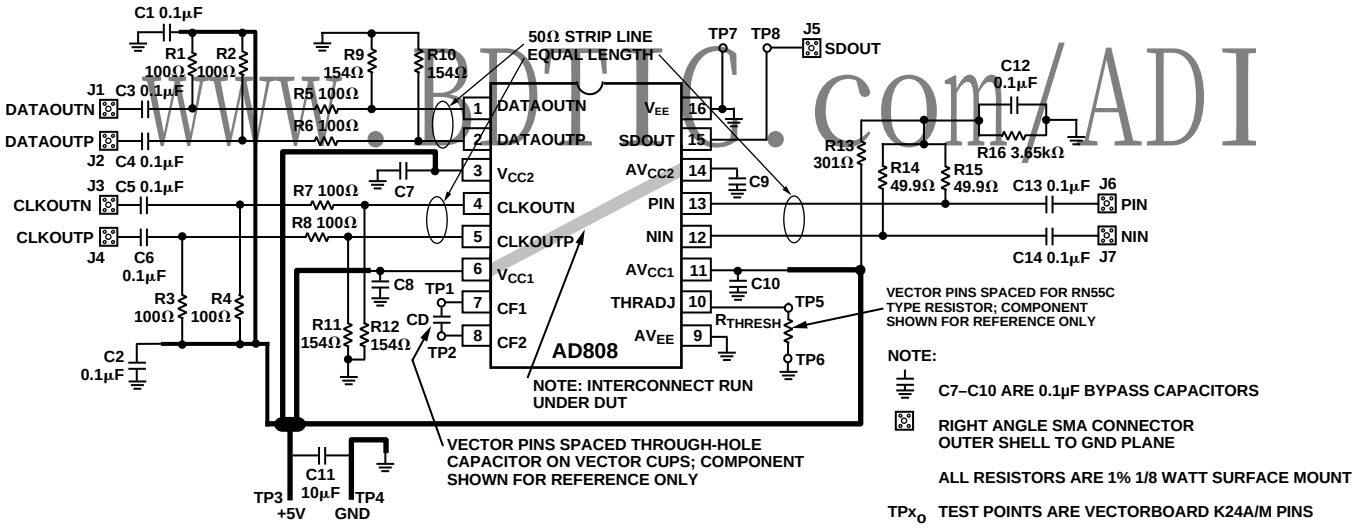


Figure 15. Evaluation Board Schematic

USING THE AD808

Acquisition Time

This is the transient time, measured in bit periods, that required for the AD808 to lock onto the input data from its free running state.

Ground Planes

The use of one ground plane for connections to both analog and digital grounds is recommended.

Power Supply Connections

The use of a 10 µF capacitor between V_{CC} and ground is recommended. The +5 V power supply connection to V_{CC2} should be carefully isolated. The V_{CC2} pin is used inside the AD808 to provide the CLKOUT and DATAOUT signals.

Use a 0.1 µF decoupling capacitor between IC power supply input and ground. This decoupling capacitor should be positioned as closed to the IC as possible. Refer to the schematic in Figure 15 for advised connections.

Transmission Lines

Use 50 Ω transmission line for PIN, NIN, CLKOUT, and DATAOUT signals.

Terminations

Use metal, thick-film, 1% termination resistors for PIN, NIN, CLKOUT, and DATAOUT signals. These termination resistors must be positioned as close to the IC as possible.

Use individual connections, not daisy chained, for connections from the +5 V to load resistors for PIN, NIN, CLKOUT, and DATAOUT signals.

Loop Damping Capacitor, C_D

A ceramic capacitor may be used for the loop damping capacitor. Using a 0.47 µF, ±20% capacitor provides < 0.1 dB jitter peaking.

AD808 Output Squelch Circuit

A simple P-channel FET circuit can be used in series with the Output Signal ECL Supply (V_{CC2}, Pin 3) to squelch clock and data outputs when SDOUT indicates a loss of signal (Figure 16). The V_{CC2} supply pin draws roughly 72 mA (14 mA for each of 4 ECL loads, plus 16 mA for all 4 ECL output stages). This means that selection of a FET with ON RESISTANCE of 0.5 Ω will affect the common mode of the ECL outputs by only 36 mV.

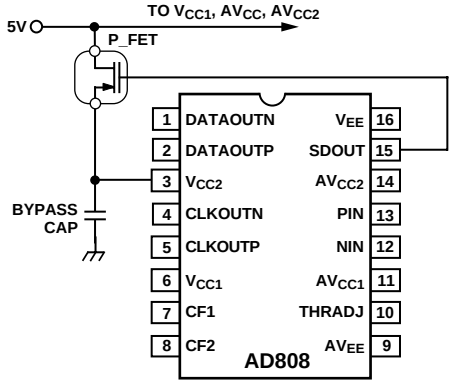
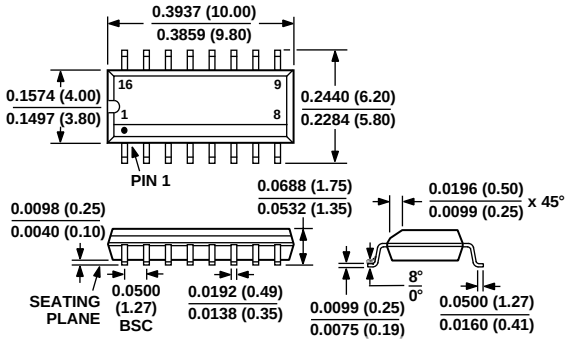


Figure 16. Squelch Circuit Schematic

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Small Outline IC Package
(R-16A)



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