8-Channel DAS with 14-Bit, Bipolar Input, Simultaneous Sampling ADC

AD7607

FEATURES

- 8 simultaneously sampled inputs
- True bipolar analog input ranges: ±10 V, ±5 V
- Single 5 V analog supply and 2.3 V to 5.25 V V_{DRIVE}
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 MΩ analog input impedance
  - Second-order antialiasing analog filter
  - On-chip accurate reference and reference buffer
  - 14-bit ADC with 200 kSPS on all channels
- Flexible parallel/serial interface
  - SPI/QSPI™/MICROWIRE™/DSP compatible
- Pin-compatible solutions from 14 bits to 18 bits
- Performance
  - 7 kV ESD rating on analog input channels
  - Fast throughput rate: 200 kSPS for all channels
  - 85.5 dB SNR at 50 kSPS
  - INL ±0.25 LSB, DNL ±0.25 LSB
  - Low power: 100 mW at 200 kSPS
  - Standby mode: 25 mW typical
- 64-lead LQFP package

APPLICATIONS

- Power-line monitoring and protection systems
- Multiphase motor control
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems (DAS)

Table 1. High Resolution, Bipolar Input, Simultaneous Sampling DAS Solutions

Resolution	Single-Ended Inputs	Number of Simultaneous Sampling Channels
18 Bits	AD7608	8
16 Bits	AD7606	8
	AD7606-6	6
	AD7606-4	4
14 Bits	AD7607	8

FUNCTIONAL BLOCK DIAGRAM

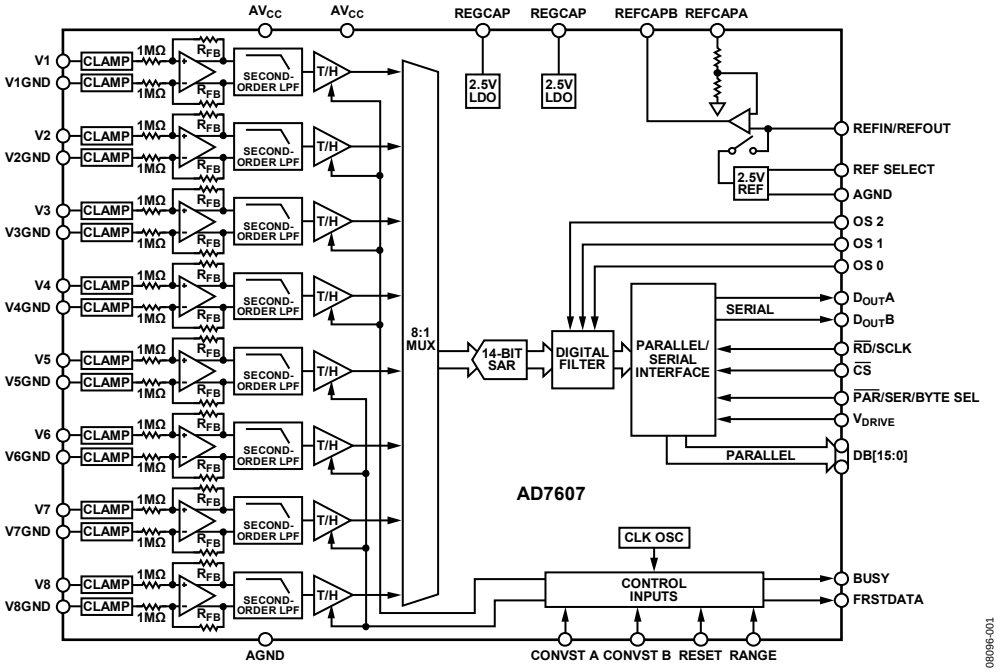

Figure 1.

Rev. A

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REVISION HISTORY

7/10—**Rev. 0 to Rev. A**

Change to Table 1 ... 1

7/10—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD7607[1] is a 14-bit, simultaneous sampling, analog-to-digital data acquisition system (DAS). The part contains analog input clamp protection; a second-order antialiasing filter; a track-and-hold amplifier; a 14-bit charge redistribution, successive approximation analog-to-digital converter (ADC); a flexible digital filter; a 2.5 V reference and reference buffer; and high speed serial and parallel interfaces.

The AD7607 operates from a single 5 V supply and can accommodate ±10 V and ±5 V true bipolar input signals while sampling at throughput rates of up to 200 kSPS for all channels. The input clamp protection circuitry can tolerate voltages of up to ±16.5 V. The AD7607 has 1 MΩ analog input impedance, regardless of sampling frequency. The single supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies. The AD7607 antialiasing filter has a 3 dB cutoff frequency of 22 kHz and provides 40 dB antialias rejection when sampling at 200 kSPS. The flexible digital filter is pin driven and can be used to simplify external filtering.

[1] Patent pending.

SPECIFICATIONS

V_{REF} = 2.5 V external/internal, AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, f_{SAMPLE} = 200 kSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 1 kHz sine wave, unless otherwise noted				
Signal-to-(Noise + Distortion) (SINAD)[2, 3]	No oversampling; ±10 V range	84	84.5		dB
	No oversampling; ±5 V range	83.5	84.5		dB
Signal-to-Noise Ratio (SNR)[2]	Oversampling by 4, f_{IN} = 130 Hz		85.5		dB
	No oversampling		84.5		dB
Total Harmonic Distortion (THD)[2]			−107	−95	dB
Peak Harmonic or Spurious Noise (SFDR)[2]			−108		dB
Intermodulation Distortion (IMD)[2]	fa = 1 kHz, fb = 1.1 kHz				
Second-Order Terms			−110		dB
Third-Order Terms			−106		dB
Channel-to-Channel Isolation[2]	f_{IN} on unselected channels up to 160 kHz		−95		dB
ANALOG INPUT FILTER					
Full Power Bandwidth	−3 dB, ±10 V range		23		kHz
	−3 dB, ±5 V range		15		kHz
	−0.1 dB, ±10 V range		10		kHz
	−0.1 dB, ±5 V range		5		kHz
$t_{GROUP\ DELAY}$	±10 V Range		11		µs
	±5 V Range		15		µs
DC ACCURACY					
Resolution	No missing codes	14			Bits
Differential Nonlinearity[2]			±0.25	±0.95	LSB[4]
Integral Nonlinearity[2]			±0.25	±0.5	LSB
Positive/Negative Full-Scale Error[2, 5]	External reference		±2	±9	LSB
	Internal reference		±2		LSB
Positive Full-Scale Error Drift[2]	External reference		±2		ppm/°C
	Internal reference		±7		ppm/°C
Negative Full-Scale Error Drift	External reference		±4		ppm/°C
	Internal reference		±8		ppm/°C
Positive/Negative Full-Scale Error Matching[2]	±10 V range		2	8	LSB
	±5 V range		4	10	LSB
Bipolar Zero Code Error[2, 6]	±10 V range		±0.5	±2	LSB
	±5 V range		±1	±3.5	LSB
Bipolar Zero Code Error Drift[2]	±10 V range		10		µV/°C
	±5 V range		5		µV/°C
Bipolar Zero Code Error Matching	±10 V range		1	2.5	LSB
	±5 V range		3	6	LSB
Total Unadjusted Error (TUE)	±10 V range		±0.5		LSB
	±5 V range		±1		LSB
ANALOG INPUT					
Input Voltage Ranges	RANGE = 1			±10	V
	RANGE = 0			±5	V
Input Current	+10 V		5.4		µA
	+5 V		2.5		µA
Input Capacitance[7]			5		pF
Input Impedance	See the Analog Input section		1		MΩ

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range		2.475	2.5	2.525	V
DC Leakage Current				±1	μA
Input Capacitance[7]	REF SELECT = 1		7.5		pF
Reference Output Voltage	REFIN/REFOUT		2.49/ 2.505		V
Reference Temperature Coefficient			±10		ppm/°C
LOGIC INPUTS					
Input High Voltage (V_{INH})		0.9 × V_{DRIVE}			V
Input Low Voltage (V_{INL})				0.1 × V_{DRIVE}	V
Input Current (I_{IN})				±2	μA
Input Capacitance (C_{IN})[7]			5		pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 100 μA	V_{DRIVE} − 0.2			V
Output Low Voltage (V_{OL})	I_{SINK} = 100 μA			0.2	V
Floating-State Leakage Current			±1	±20	μA
Floating-State Output Capacitance[7]			5		pF
Output Coding	Twos complement				
CONVERSION RATE					
Conversion Time	All eight channels included; see Table 3		4		μs
Track-and-Hold Acquisition Time			1		μs
Throughput Rate	All eight channels included			200	kSPS
POWER REQUIREMENTS					
AV_{CC}		4.75		5.25	V
V_{DRIVE}		2.3		5.25	V
I_{TOTAL}	Digital inputs = 0 V or V_{DRIVE}				
Normal Mode (Static)			16	22	mA
Normal Mode (Operational)[8]			20	27	mA
Standby Mode			5	8	mA
Shutdown Mode			2	6	μA
Power Dissipation[8]					
Normal Mode (Static)			80	115.5	mW
Normal Mode (Operational)			100	142	mW
Standby Mode			25	42	mW
Shutdown Mode			10	31.5	μW

[1] Temperature range for the B version is −40°C to +85°C.
[2] See the Terminology section.
[3] This specification applies when reading during a conversion or after a conversion. If reading during a conversion in parallel mode with V_{DRIVE} = 5 V, SNR typically reduces by 1.5 dB and THD typically reduces by 3 dB.
[4] LSB means least significant bit. With ±5 V input range, 1 LSB = 610.35 μV. With ±10 V input range, 1 LSB = 1.22 mV.
[5] This specification includes the full temperature range variation and contribution from the internal reference buffer but does not include the error contribution from the external reference.
[6] Bipolar zero code error is calculated with respect to the analog input voltage.
[7] Sample tested during initial release to ensure compliance.
[8] Operational power/current figure includes contribution when running in oversampling mode.

TIMING SPECIFICATIONS

AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, V_{REF} = 2.5 V external reference/internal reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 3.

	Limit at T_{MIN}, T_{MAX}				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Description**
PARALLEL/SERIAL/BYTE MODE					
t_{CYCLE}					1/throughput rate
			5	µs	Parallel mode, reading during or after conversion; or serial mode (V_{DRIVE} = 3.3 V to 5.25 V), reading during a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines
		5		µs	Serial mode reading during conversion; V_{DRIVE} = 2.7 V
			9.1	µs	Serial mode reading after a conversion; V_{DRIVE} = 2.3 V, $D_{OUT}A$ and $D_{OUT}B$ lines
t_{CONV}					Conversion time
	3.45	4	4.15	µs	Oversampling off
	7.87		9.1	µs	Oversampling by 2
	16.05		18.8	µs	Oversampling by 4
	33		39	µs	Oversampling by 8
	66		78	µs	Oversampling by 16
	133		158	µs	Oversampling by 32
	257		315	µs	Oversampling by 64
$t_{WAKE-UP\ STANDBY}$			100	µs	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from standby mode
$t_{WAKE-UP\ SHUTDOWN}$					
Internal Reference			30	ms	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from shutdown mode
External Reference			13	ms	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from shutdown mode
t_{RESET}	50			ns	RESET high pulse width
t_{OS_SETUP}	20			ns	BUSY to OS x pin setup time
t_{OS_HOLD}	20			ns	BUSY to OS x pin hold time
t_1			40	ns	CONVST x high to BUSY high
t_2	25			ns	Minimum CONVST x low pulse
t_3	25			ns	Minimum CONVST x high pulse
t_4	0			ns	BUSY falling edge to $\overline{CS}$ falling edge setup time
t_5[2]			0.5	ms	Maximum delay allowed between CONVST A, CONVST B rising edges
t_6			25	ns	Maximum time between last $\overline{CS}$ rising edge and BUSY falling edge
t_7	25			ns	Minimum delay between RESET low to CONVST x high
PARALLEL/BYTE READ OPERATION					
t_8	0			ns	$\overline{CS}$ to $\overline{RD}$ setup time
t_9	0			ns	$\overline{CS}$ to $\overline{RD}$ hold time
t_{10}					$\overline{RD}$ low pulse width
	16			ns	V_{DRIVE} above 4.75 V
	21			ns	V_{DRIVE} above 3.3 V
	25			ns	V_{DRIVE} above 2.7 V
	32			ns	V_{DRIVE} above 2.3 V
t_{11}	15			ns	$\overline{RD}$ high pulse width
t_{12}	22			ns	$\overline{CS}$ high pulse width (see Figure 5); $\overline{CS}$ and $\overline{RD}$ linked

Parameter	Limit at T_{MIN}, T_{MAX} Min	Typ	Max	Unit	Description
t_{13}					Delay from $\overline{CS}$ until DB[15:0] three-state disabled
			16	ns	V_{DRIVE} above 4.75 V
			20	ns	V_{DRIVE} above 3.3 V
			25	ns	V_{DRIVE} above 2.7 V
			30	ns	V_{DRIVE} above 2.3 V
t_{14}[3]					Data access time after $\overline{RD}$ falling edge
			16	ns	V_{DRIVE} above 4.75 V
			21	ns	V_{DRIVE} above 3.3 V
			25	ns	V_{DRIVE} above 2.7 V
			32	ns	V_{DRIVE} above 2.3 V
t_{15}	6			ns	Data hold time after $\overline{RD}$ falling edge
t_{16}	6			ns	$\overline{CS}$ to DB[15:0] hold time
t_{17}			22	ns	Delay from $\overline{CS}$ rising edge to DB[15:0] three-state enabled
SERIAL READ OPERATION					
f_{SCLK}					Frequency of serial read clock
			23.5	MHz	V_{DRIVE} above 4.75 V
			17	MHz	V_{DRIVE} above 3.3 V
			14.5	MHz	V_{DRIVE} above 2.7 V
			11.5	MHz	V_{DRIVE} above 2.3 V
t_{18}					Delay from $\overline{CS}$ until $D_{OUT}A/D_{OUT}B$ three-state disabled/delay from $\overline{CS}$ until MSB valid
			15	ns	V_{DRIVE} above 4.75 V
			20	ns	V_{DRIVE} above 3.3 V
			30	ns	V_{DRIVE} = 2.3 V to 2.7 V
t_{19}[3]					Data access time after SCLK rising edge
			17	ns	V_{DRIVE} above 4.75 V
			23	ns	V_{DRIVE} above 3.3 V
			27	ns	V_{DRIVE} above 2.7 V
			34	ns	V_{DRIVE} above 2.3 V
t_{20}	0.4 t_{SCLK}			ns	SCLK low pulse width
t_{21}	0.4 t_{SCLK}			ns	SCLK high pulse width
t_{22}	7				SCLK rising edge to $D_{OUT}A/D_{OUT}B$ valid hold time
t_{23}			22	ns	$\overline{CS}$ rising edge to $D_{OUT}A/D_{OUT}B$ three-state enabled
FRSTDATA OPERATION					
t_{24}					Delay from $\overline{CS}$ falling edge until FRSTDATA three-state disabled
			15	ns	V_{DRIVE} above 4.75 V
			20	ns	V_{DRIVE} above 3.3 V
			25	ns	V_{DRIVE} above 2.7 V
			30	ns	V_{DRIVE} above 2.3 V
t_{25}				ns	Delay from $\overline{CS}$ falling edge until FRSTDATA high, serial mode
			15	ns	V_{DRIVE} above 4.75 V
			20	ns	V_{DRIVE} above 3.3 V
			25	ns	V_{DRIVE} above 2.7 V
			30	ns	V_{DRIVE} above 2.3 V
t_{26}					Delay from $\overline{RD}$ falling edge to FRSTDATA high
			16	ns	V_{DRIVE} above 4.75 V
			20	ns	V_{DRIVE} above 3.3 V
			25	ns	V_{DRIVE} above 2.7 V
			30	ns	V_{DRIVE} above 2.3 V

Parameter	Limit at T_{MIN}, T_{MAX} Min	Typ	Max	Unit	Description
t_{27}					Delay from $\overline{RD}$ falling edge to FRSTDATA low
			19	ns	V_{DRIVE} = 3.3 V to 5.25 V
			24	ns	V_{DRIVE} = 2.3 V to 2.7 V
t_{28}					Delay from 16th SCLK falling edge to FRSTDATA low
			17	ns	V_{DRIVE} = 3.3 V to 5.25 V
			22	ns	V_{DRIVE} = 2.3 V to 2.7 V
t_{29}			24	ns	Delay from $\overline{CS}$ rising edge until FRSTDATA three-state enabled

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.
[2] The delay between the CONVST x signals was measured as the maximum time allowed while ensuring a <3 LSB performance matching between channel sets.
[3] A buffer, which is equivalent to a load of 20 pF on the output pins, is used on the data output pins for these measurements.

Timing Diagrams

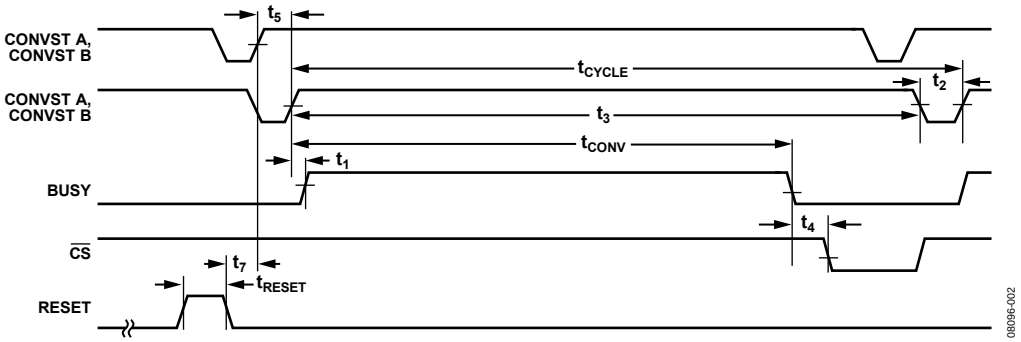


Figure 2. CONVST Timing—Reading After a Conversion

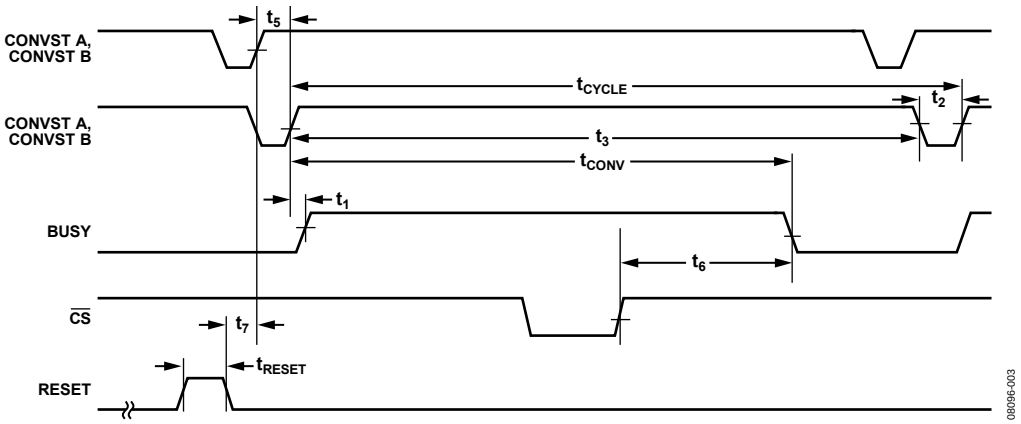


Figure 3. CONVST Timing—Reading During a Conversion

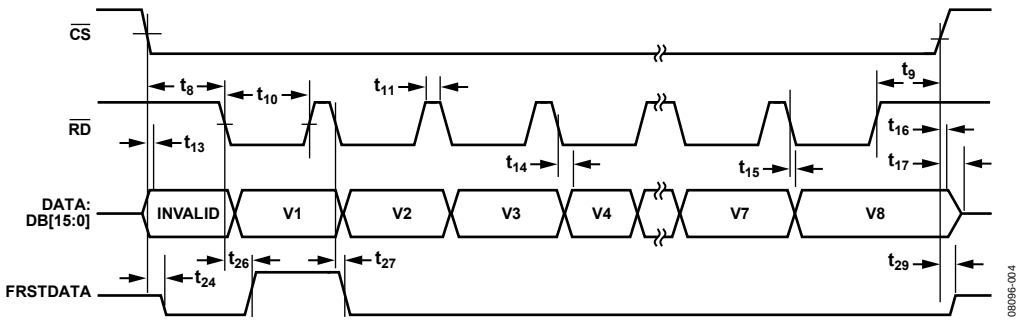


Figure 4. Parallel Mode, Separate $\overline{CS}$ and $\overline{RD}$ Pulses

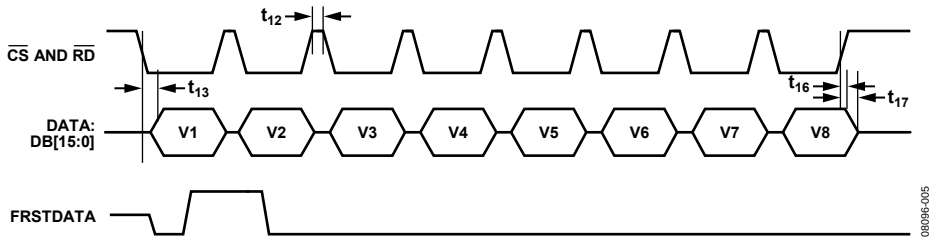


Figure 5. Linked Parallel Mode, $\overline{CS}$ and $\overline{RD}$

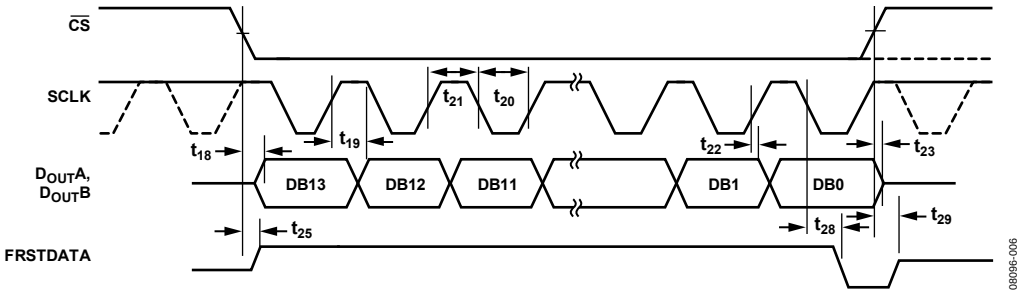


Figure 6. Serial Read Operation (Channel 1)

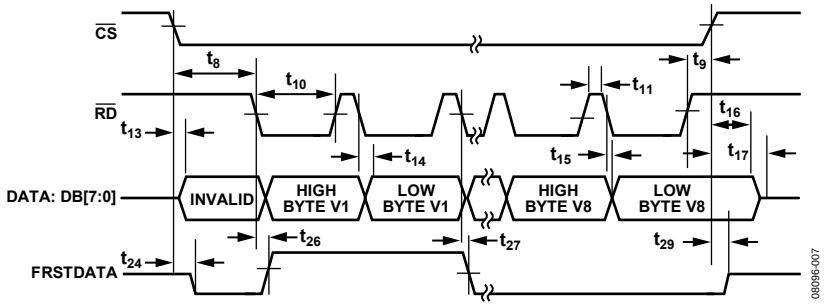


Figure 7. BYTE Mode Read Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to AV_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	±16.5 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
B Version	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/SN Temperature, Soldering	
Reflow (10 sec to 30 sec)	240 (+ 0)°C
Pb-Free Temperature, Soldering Reflow	260 (+ 0)°C
ESD (All Pins Except Analog Inputs)	2 kV
ESD (Analog Input Pins Only)	7 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. These specifications apply to a 4-layer board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead LQFP	45	11	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

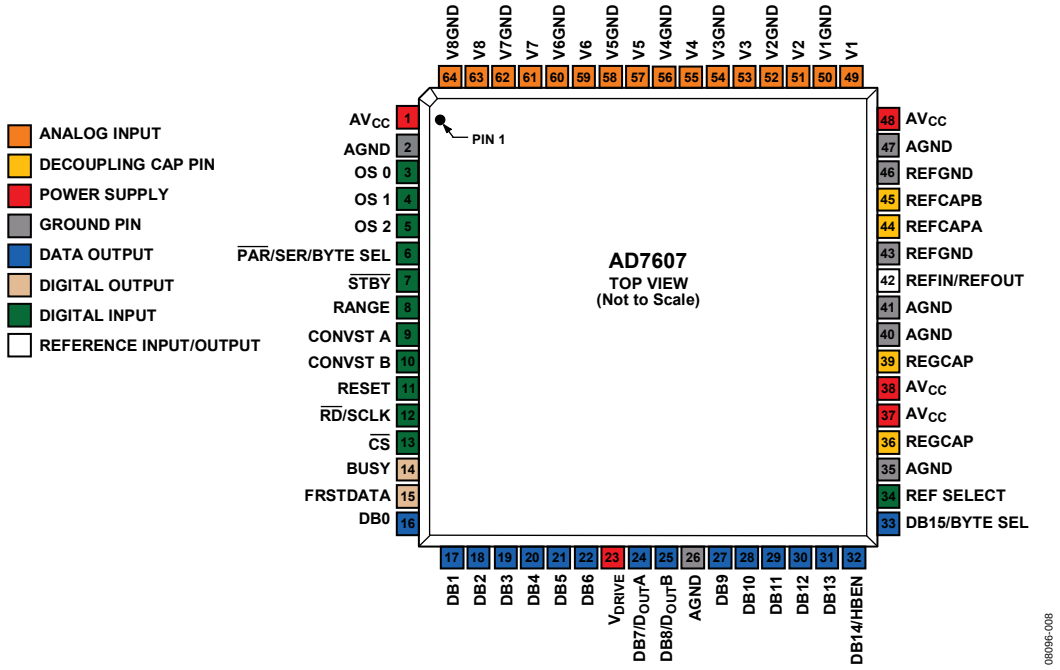


Figure 8. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic	Description
1, 37, 38, 48	P	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. These supply pins should be decoupled to AGND.
2, 26, 35, 40, 41, 47	P	AGND	Analog Ground. These pins are the ground reference points for all analog circuitry on the AD7607. All analog input signals and external reference signals should be referred to these pins. All six of these AGND pins should connect to the AGND plane of a system.
5, 4, 3	DI	OS[2:0]	Oversampling Mode Pins. Logic inputs. These inputs are used to select the oversampling ratio. OS 2 is the MSB control bit, and OS 0 is the LSB control bit. See the Digital Filter section for more details about the oversampling mode of operation and Table 9 for oversampling bit decoding.
6	DI	$\overline{PAR}$/SER/ BYTE SEL	Parallel/Serial/Byte Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. Parallel byte interface mode is selected when this pin is logic high and DB15/BYTE SEL is logic high (see Table 8). In serial mode, the $\overline{RD}$/SCLK pin functions as the serial clock input. The DB7/D_{OUT}A pin and the DB8/D_{OUT}B pin function as serial data outputs. When the serial interface is selected, the DB[15:9] and DB[6:0] pins should be tied to ground. In byte mode, DB15, in conjunction with $\overline{PAR}$/SER/BYTE SEL, is used to select the parallel byte mode of operation (see Table 8). DB14 is used as the HBEN pin. DB[7:0] transfer the 16-bit conversion results in two $\overline{RD}$ operations, with DB0 as the LSB of the data transfers.
7	DI	$\overline{STBY}$	Standby Mode Input. This pin is used to place the AD7607 into one of two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin, as shown in Table 7. When in standby mode, all circuitry, except the on-chip reference, regulators, and regulator buffers, is powered down. When in shutdown mode, all circuitry is powered down.
8	DI	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±10 V for all channels. If this pin is tied to a logic low, the analog input range is ±5 V for all channels. A logic change on this pin has an immediate effect on the analog input range. Changing this pin during a conversion is not recommended. See the Analog Input section for more information.

Pin No.	Type[1]	Mnemonic	Description
9, 10	DI	CONVST A, CONVST B	Conversion Start Input A, Conversion Start Input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels. For simultaneous sampling of all 8 input channels CONVST A and CONVST B can be shorted together and a single convert start signal applied. Alternatively, CONVST A can be used to initiate simultaneous sampling for V1, V2, V3, and V4; and CONVST B can be used to initiate simultaneous sampling on the other analog inputs (V5, V6, V7, and V8). This is possible only when oversampling is not switched on. When the CONVST A or CONVST B pin transitions from low to high, the front-end track-and-hold circuitry for their respective analog inputs is set to hold.
11	DI	RESET	Reset Input. When set to logic high, the rising edge of RESET resets the AD7607. The part should receive a RESET pulse after power-up. The RESET high pulse should typically be 50 ns wide. If a RESET pulse is applied during a conversion, the conversion is aborted. If a RESET pulse is applied during a read, the contents of the output registers reset to all zeros.
12	DI	$\overline{RD}$/SCLK	Parallel Data Read Control Input When the Parallel Interface Is Selected ($\overline{RD}$)/Serial Clock Input When the Serial Interface is Selected (SCLK). When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus is enabled. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{CS}$ falling edge takes the $D_{OUT}A$ and $D_{OUT}B$ data output lines out of tristate and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the $D_{OUT}A$ and $D_{OUT}B$ serial data outputs. For more information, see the Conversion Control section.
13	DI	$\overline{CS}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the DB[15:0] output bus is enabled and the conversion result is output on the parallel data bus lines. In serial mode, $\overline{CS}$ is used to frame the serial read transfer and clock out the MSB of the serial output data.
14	DO	BUSY	Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and is available to read after a Time t_4. Any data read while BUSY is high must be completed before the falling edge of BUSY occurs. Rising edges on CONVST A or CONVST B have no effect while the BUSY signal is high.
15	DO	FRSTDATA	Digital Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on the parallel, parallel byte, or serial interface. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{CS}$ takes FRSTDATA out of three-state. In parallel mode, the falling edge of $\overline{RD}$ corresponding to the result of V1 then sets the FRSTDATA pin high, which indicates that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the next falling edge of $\overline{RD}$. In serial mode, FRSTDATA goes high on the falling edge of $\overline{CS}$ because this clocks out the MSB of V1 on $D_{OUT}A$. It returns low on the 14th SCLK falling edge after the $\overline{CS}$ falling edge. See the Conversion Control section for more details.
22 to 16	DO	DB[6:0]	Parallel Output Data Bits, DB6 to DB0. When $\overline{PAR}$/SER/BYTE SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB6 to DB0 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, these pins should be tied to DGND. When operating in parallel byte interface mode, DB[7:0] outputs the 14-bit conversion result in two $\overline{RD}$ operations. DB7 is the MSB, and DB0 is the LSB.
23	P	V_{DRIVE}	Logic Power Supply Input. The voltage (2.3 V to 5.25 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (that is, DSP and FPGA).
24	DO	DB7/$D_{OUT}A$	Parallel Output Data Bit 7 (DB7)/Serial Interface Data Output Pin ($D_{OUT}A$). When $\overline{PAR}$/SER/BYTE SEL = 0, this pins acts as a three-state parallel digital input/ output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB7 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, this pin functions as $D_{OUT}A$ and outputs serial conversion data (see the Conversion Control section for more details). When operating in parallel byte mode, DB7 is the MSB of the byte.
25	DO	DB8/$D_{OUT}B$	Parallel Output Data Bit 8 (DB8)/Serial Interface Data Output Pin ($D_{OUT}B$). When $\overline{PAR}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB8 of the conversion result. When $\overline{PAR}$/ SER/BYTE SEL = 1, this pin functions as $D_{OUT}B$ and outputs serial conversion data (see the Conversion Control section for more details).
31 to 27	DO	DB[13:9]	Parallel Output Data Bits, DB13 to DB9. When $\overline{PAR}$/SER/BYTE SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB13 to DB9 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, these pins should be tied to DGND.

Pin No.	Type[1]	Mnemonic	Description
32	DO/DI	DB14/HBEN	Parallel Output Data Bit 14 (DB14)/High Byte Enable (HBEN). When $\overline{PAR}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB14 of the conversion result, which is a sign extended bit of the MSB, DB13. When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1, the AD7607 operates in parallel byte interface mode, in which the HBEN pin is used to select if the most significant byte (MSB) or the least significant byte (LSB) of the conversion result is output first. When HBEN = 1, the MSB byte is output first, followed by the LSB byte. When HBEN = 0, the LSB byte is output first, followed by the MSB byte.
33	DO/DI	DB15/ BYTE SEL	Parallel Output Data Bit 15 (DB15)/Parallel Byte Mode Select (BYTE SEL). When $\overline{PAR}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB15, which is a sign extended bit of the MSB, DB13, of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, the BYTE SEL pin is used to select between serial interface mode or parallel byte interface mode (see Table 8). When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 0, the AD7607 operates in serial interface mode. When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1, the AD7607 operates in parallel byte interface mode.
34	DI	REF SELECT	Internal/External Reference Selection Input. Logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
36, 39	P	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. These output pins should be decoupled separately to AGND using a 1 µF capacitor. The voltage on these pins is in the range of 2.5 V to 2.7 V.
42	REF	REFIN/ REFOUT	Reference Input (REFIN)/Reference Output (REFOUT). The gained up on-chip reference of 2.5 V is available on this pin for external use if the REF SELECT pin is set to a logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to a logic low, and an external reference of 2.5 V can be applied to this input (see the Internal/External Reference section). Decoupling is required on this pin for both the internal or external reference options. A 10 µF capacitor should be applied from this pin to ground close to the REFGND pins.
43, 46	REF	REFGND	Reference Ground Pins. These pins should be connected to AGND.
44, 45	REF	REFCAPA, REFCAPB	Reference Buffer Output Force/Sense Pins. These pins must be connected together and decoupled to AGND using a low ESR 10 µF ceramic capacitor.
49, 51, 53, 55, 57, 59, 61, 63	AI	V1 to V8	Analog Inputs. These pins are single-ended analog inputs. The analog input range of these channels is determined by the RANGE pin.
50, 52, 54, 56, 58, 60, 62, 64	AI GND	V1GND to V8GND	Analog Input Ground Pins. These pins correspond to Analog Input Pin V1 to Analog Input Pin V8. All analog input AGND pins should connect to the AGND plane of a system.

[1] P = power supply, DI = digital input, DO = digital output, REF = reference input/output, AI = analog input, GND = ground.

TYPICAL PERFORMANCE CHARACTERISTICS

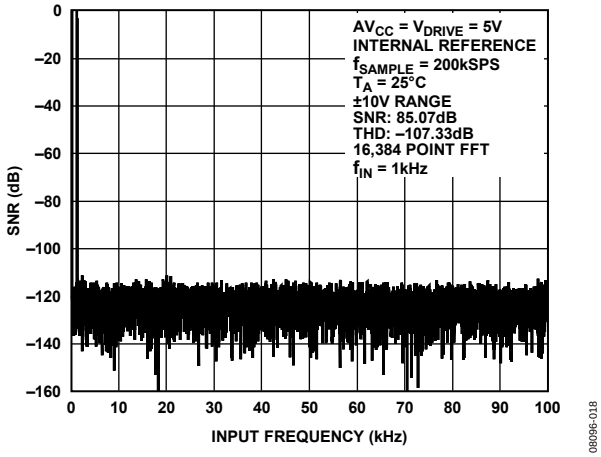


Figure 9. FFT ± 10 V Range

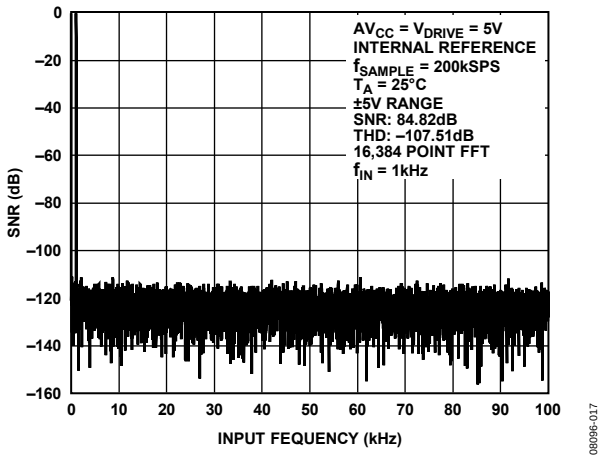


Figure 10. FFT Plot ± 5 V Range

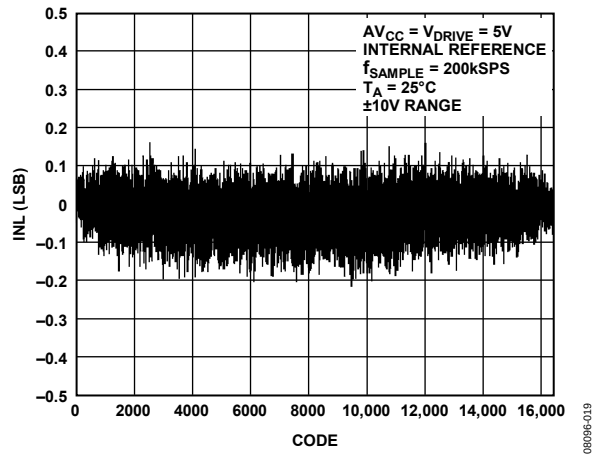


Figure 11. Typical INL ± 10 V Range

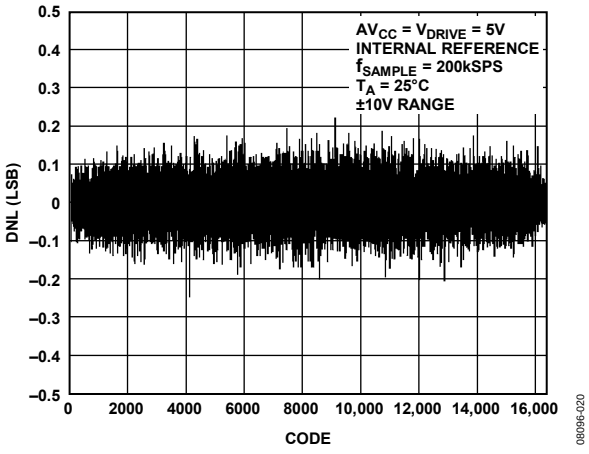


Figure 12. Typical DNL ± 10 V Range

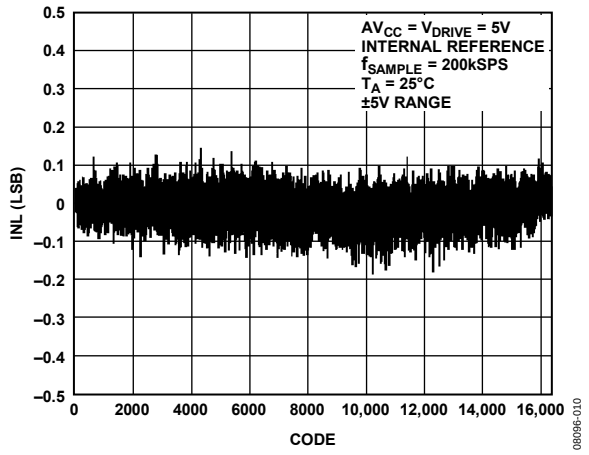


Figure 13. Typical INL ± 5 V Range

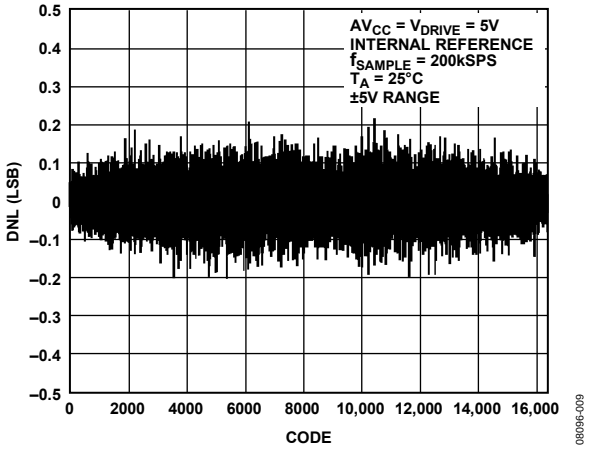


Figure 14. Typical DNL ± 5 V Range

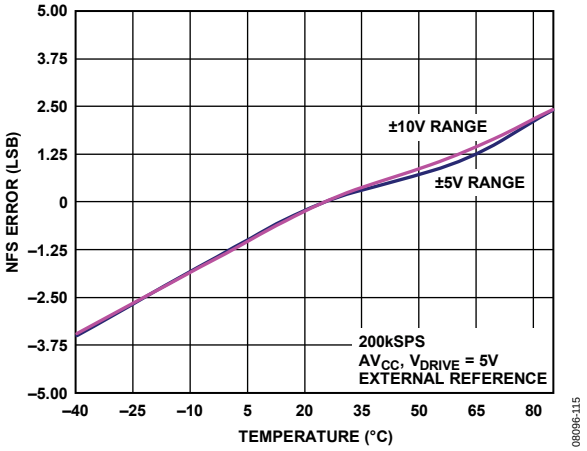


Figure 15. NFS Error vs. Temperature

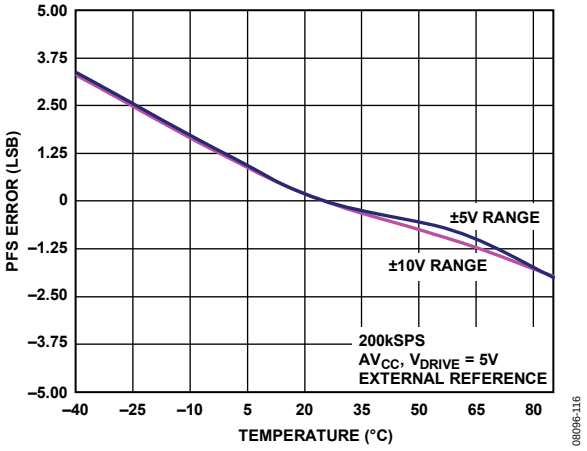


Figure 16. PFS Error vs. Temperature

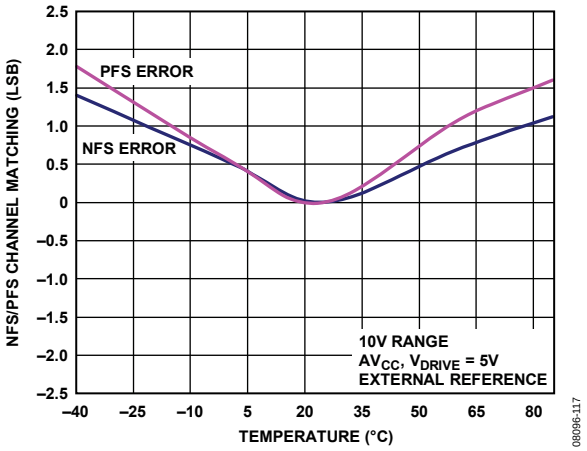


Figure 17. PFS and NFS Error Matching vs. Temperature

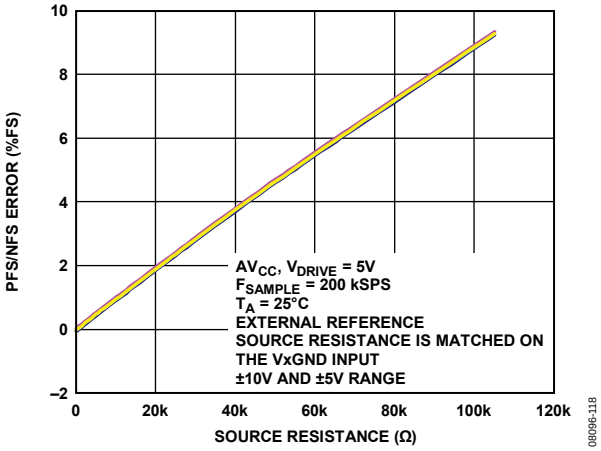


Figure 18. PFS and NFS Error vs. Source Resistance

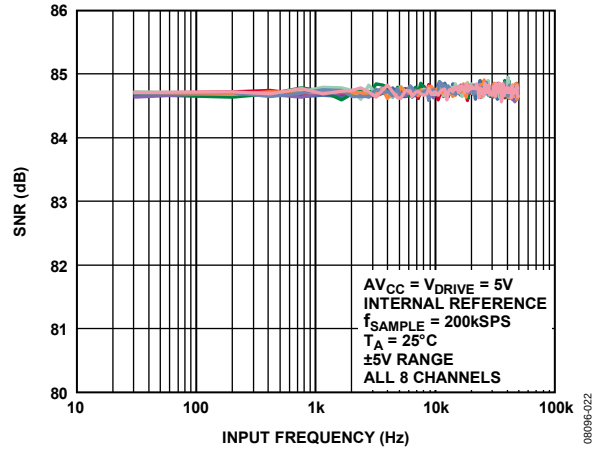


Figure 19. SNR vs. Input Frequency ± 5 V Range

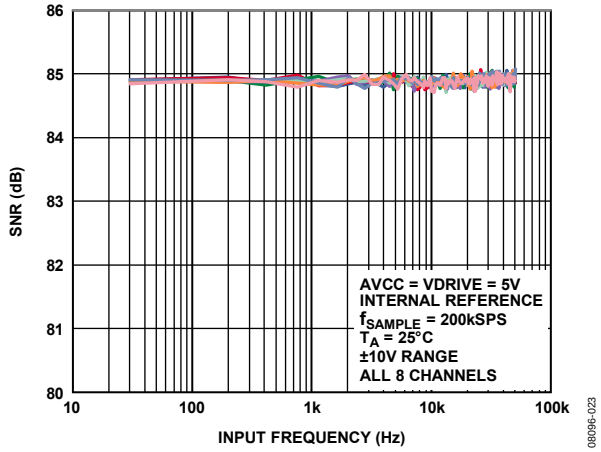


Figure 20. SNR vs. Input Frequency ± 10 V Range

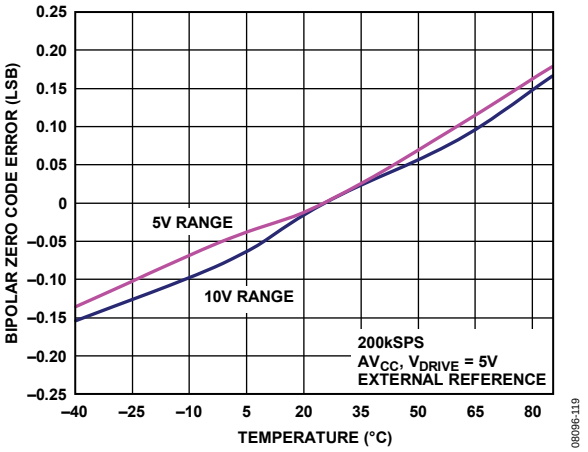


Figure 21. Bipolar Zero Code Error vs. Temperature

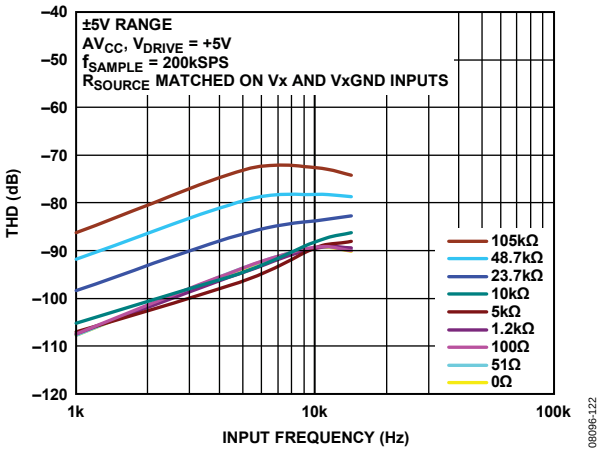


Figure 24. THD vs. Input Frequency for Various Source Impedances, ±5 V Range

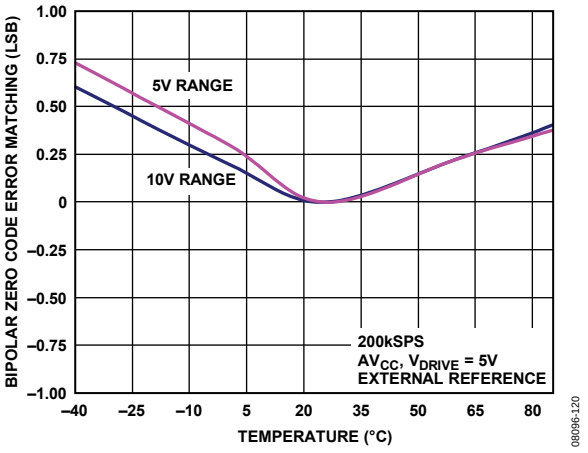


Figure 22. Bipolar Zero Code Error Matching vs. Temperature

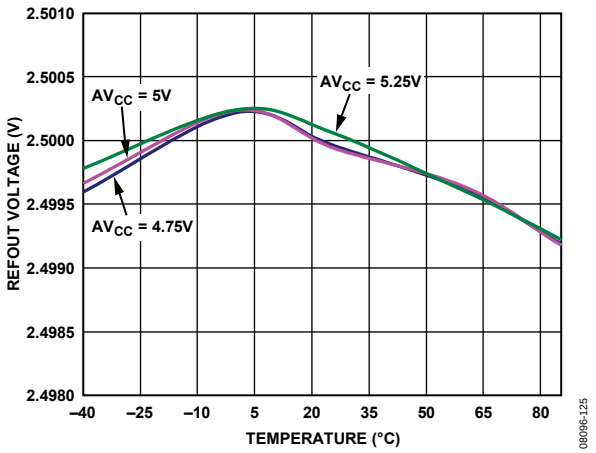


Figure 25. Reference Output Voltage vs. Temperature for Different Supply Voltages

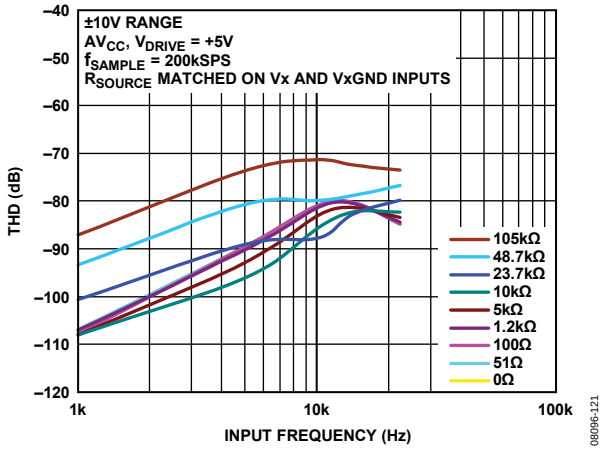


Figure 23. THD vs. Input Frequency for Various Source Impedances, ±10 V Range

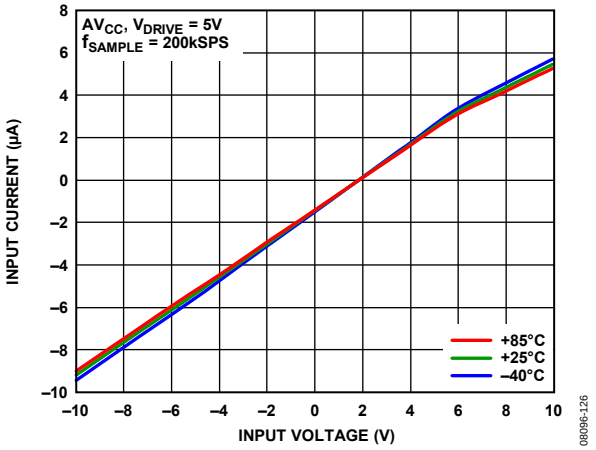


Figure 26. Analog Input Current vs. Input Voltage for Various Temperatures

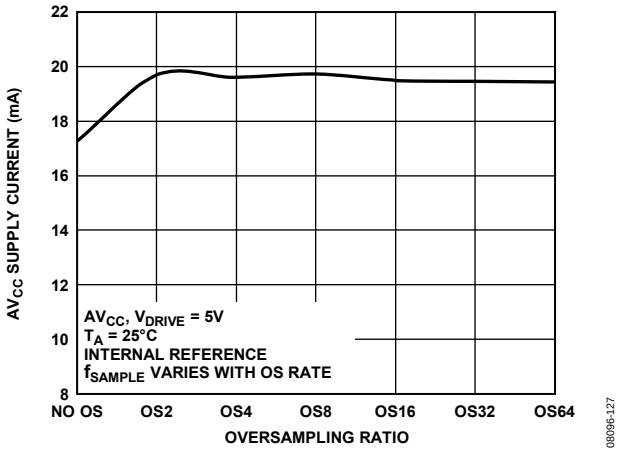


Figure 27. Supply Current vs. Oversampling Rate

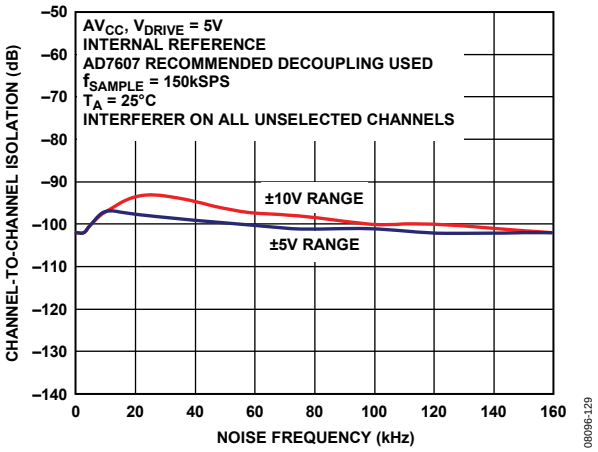


Figure 29. Channel-to-Channel Isolation

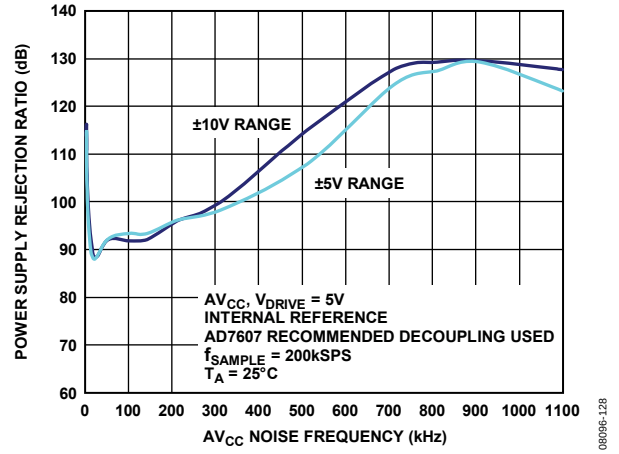


Figure 28. PSRR

TERMINOLOGY

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, at ½ LSB below the first code transition; and full scale, at ½ LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error
The deviation of the midscale transition (all 1s to all 0s) from the ideal, which is 0 V − ½ LSB.

Bipolar Zero Code Error Match
The absolute difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error

The deviation of the actual last code transition from the ideal last code transition (10 V − 1½ LSB (9.998) and 5 V − 1½ LSB (4.99908)) after bipolar zero code error is adjusted out. The positive full-scale error includes the contribution from the internal reference buffer.

Positive Full-Scale Error Match
The absolute difference in positive full-scale error between any two input channels.

Negative Full-Scale Error

The deviation of the first code transition from the ideal first code transition (−10 V + ½ LSB (−9.9993) and −5 V + ½ LSB (−4.99969)) after the bipolar zero code error is adjusted out. The negative full-scale error includes the contribution from the internal reference buffer.

Negative Full-Scale Error Match
The absolute difference in negative full-scale error between any two input channels.

Signal-to-(Noise + Distortion) Ratio
The measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$, excluding dc).

The ratio depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise.

The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, for a 14-bit converter, the signal-to-(noise + distortion) is 86.04 dB.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the harmonics to the fundamental. For the AD7607, it is defined as

$$THD\ (\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + V_8^2 + V_9^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2 to V_9 are the rms amplitudes of the second through ninth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities create distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSR is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The PSR ratio (PSRR) is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC's V_{DD} and V_{SS} supplies of frequency, f_S.

$$PSRR\ (\text{dB}) = 10\log\ (Pf/Pf_S)$$

where:
Pf is equal to the power at Frequency f in the ADC output.
Pf_S is equal to the power at Frequency f_S coupled onto the AV_{CC} supplies.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale sine wave signal of up to 160 kHz to all unselected input channels, and then determining the degree to which the signal attenuates in the selected channel with a 1 kHz sine wave signal applied (see Figure 29).

THEORY OF OPERATION

CONVERTER DETAILS

The AD7607 is a data acquisition system that employs a high speed, low power, charge redistribution, successive approximation analog-to-digital converter (ADC) and allows the simultaneous sampling of eight analog input channels. The analog inputs on the AD7607 can accept true bipolar input signals. The RANGE pin is used to select either ±10 V or ±5 V as the input range. The AD7607 operates from a single 5 V supply.

The AD7607 contains input clamp protection, input signal scaling amplifiers, a second-order antialiasing filter, track-and-hold amplifiers, an on-chip reference, reference buffers, a high speed ADC, a digital filter, and high speed parallel and serial interfaces. Sampling on the AD7607 is controlled using the CONVST signals.

ANALOG INPUT

Analog Input Ranges

The AD7607 can handle true bipolar input voltages. The logic level on the RANGE pin determines the analog input range of all analog input channels. If this pin is tied to a logic high, the analog input range is ±10 V for all channels. If this pin is tied to a logic low, the analog input range is ±5 V for all channels. A logic change on this pin has an immediate effect on the analog input range; however, there is a typical settling time of ~80 µs, in addition to the normal acquisition time requirement. Recommended practice is to hardwire the RANGE pin according to the desired input range for the system signals.

Analog Input Impedance

The analog input impedance of the AD7607 is 1 MΩ. This is a fixed input impedance that does not vary with the AD7607 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7607, allowing for direct connection to the source or sensor. With the need for a driver amplifier eliminated, bipolar supplies (which are often a source of noise in a system) can be removed from the signal chain.

Analog Input Clamp Protection

Figure 30 shows the analog input structure of the AD7607. Each AD7607 analog input contains clamp protection circuitry. Despite single 5 V supply operation, this analog input clamp protection allows for an input overvoltage of up to ±16.5 V.

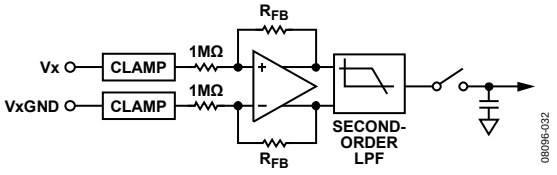


Figure 30. Analog Input Circuitry

Figure 31 shows the voltage vs. current characteristic of the clamp circuit. For input voltages of up to ±16.5 V, no current flows in the clamp circuit. For input voltages that are above ±16.5 V, the AD7607 clamp circuitry turns on and clamps the analog input to ±16.5 V.

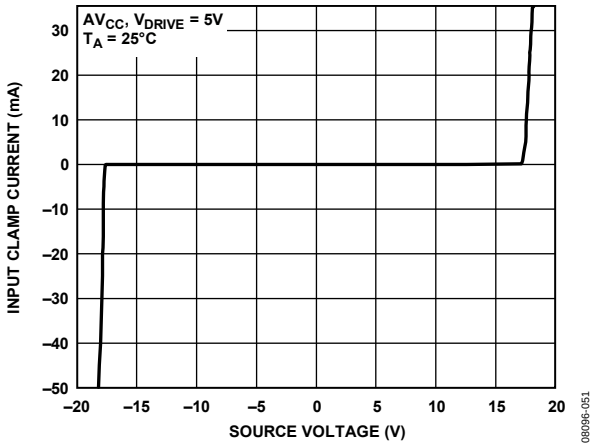


Figure 31. Input Protection Clamp Profile

A series resistor should be placed on the analog input channels to limit the current to ±10 mA for input voltages above ±16.5 V. In an application where there is a series resistance on an analog input channel, Vx, a corresponding resistance is required on the analog input GND channel, VxGND (see Figure 32). If there is no corresponding resistor on the VxGND channel, an offset error occurs on that channel.

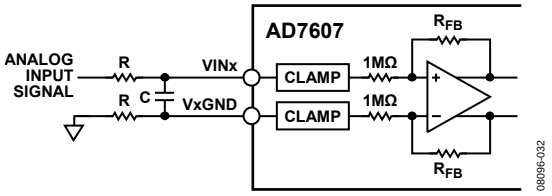
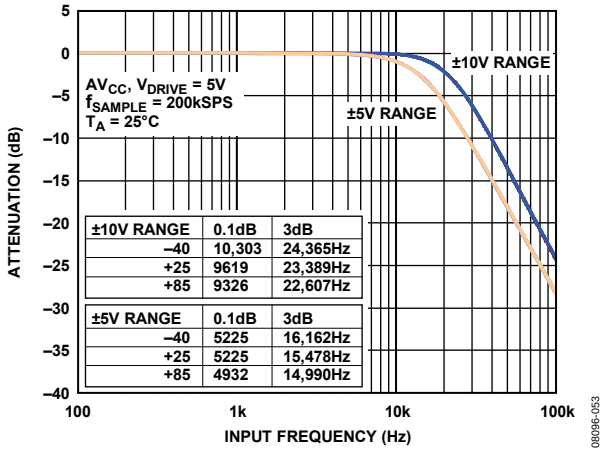


Figure 32. Input Resistance Matching on the Analog Input

Analog Input Antialiasing Filter

An analog antialiasing filter (a second-order Butterworth) is also provided on the AD7607. Figure 33 and Figure 34 show the frequency and phase response, respectively, of the analog antialiasing filter. In the ±5 V range, the −3 dB frequency is typically 15 kHz. In the ±10 V range, the −3 dB frequency is typically 23 kHz.



±10V RANGE	0.1dB	3dB
–40	10,303	24,365Hz
+25	9619	23,389Hz
+85	9326	22,607Hz

±5V RANGE	0.1dB	3dB
–40	5225	16,162Hz
+25	5225	15,478Hz
+85	4932	14,990Hz

Figure 33. Analog Antialiasing Filter Frequency Response

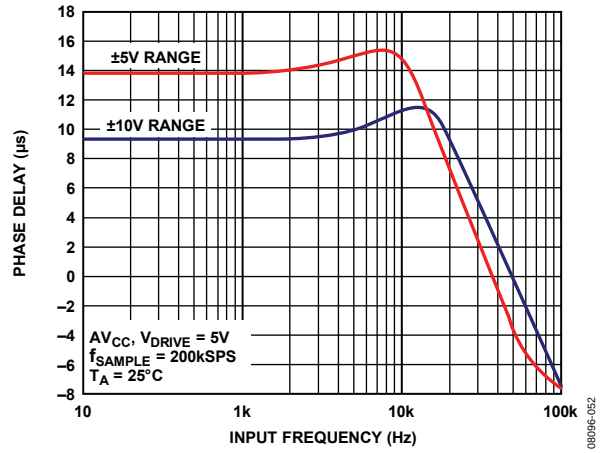


Figure 34. Analog Antialiasing Filter Phase Response

Track-and-Hold Amplifiers

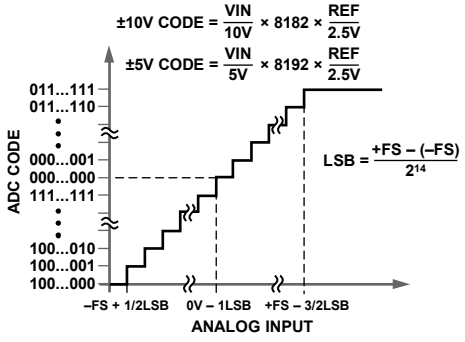
The track-and-hold amplifiers on the AD7607 allow the ADC to accurately acquire an input sine wave of full-scale amplitude to 14-bit resolution. The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVST x. The aperture time for the track-and-hold (that is, the delay time between the external CONVST x signal and the track-and-hold actually going into hold) is well matched, by design, across all eight track-and-holds on one device and from device to device. This matching allows more than one AD7607 device to be sampled simultaneously in a system.

The end of the conversion process across all eight channels is indicated by the falling edge of BUSY, and it is at this point that the track-and-holds return to track mode and the acquisition time for the next set of conversions begins.

The conversion clock for the part is internally generated, and the conversion time for all channels is 4 µs. On the AD7607, the BUSY signal returns low after all eight conversions to indicate the end of the conversion process. On the falling edge of BUSY, the track-and-hold amplifiers return to track mode. New data can be read from the output register via the parallel, parallel byte, or serial interface after BUSY goes low; or, alternatively, data from the previous conversion can be read while BUSY is high. Reading data from the AD7607 while a conversion is in progress has little effect on performance and allows a faster throughput to be achieved. In parallel mode at V_{DRIVE} > 3.3 V, the SNR is reduced by ~1.5 dB when reading during a conversion.

ADC TRANSFER FUNCTION

The output coding of the AD7607 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB, 3/2 LSB. The LSB size is FSR/16,384. The ideal transfer characteristic is shown in Figure 35.



	+FS	MIDSCALE	–FS	LSB
±10V RANGE	+10V	0V	–10V	1.22mV
±5V RANGE	+5V	0V	–5V	610µV

Figure 35. Transfer Characteristics

The LSB size is dependent on the analog input range selected.

INTERNAL/EXTERNAL REFERENCE

The AD7607 contains an on-chip 2.5 V bandgap reference. The REFIN/REFOUT pin allows access to the 2.5 V reference that generates the on-chip 4.5 V reference internally, or it allows an external reference of 2.5 V to be applied to the AD7607. An externally applied reference of 2.5 V is also gained up to 4.5 V, using the internal buffer. This 4.5 V buffered reference is the reference used by the SAR ADC.

The REF SELECT pin is a logic input pin that allows the user to select between the internal reference or an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After a reset, the AD7607 operates in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal and external reference options. A 10 µF ceramic capacitor is required on the REFIN/REFOUT pin.

The AD7607 contains a reference buffer configured to gain the REF voltage up to ~4.5 V, as shown in Figure 36. The REFCAPA and REFCAPB pins must be shorted together externally, and a ceramic capacitor of 10 µF applied to REFGND, to ensure that the reference buffer is in closed-loop operation. The reference voltage available at the REFIN/REFOUT pin is 2.5 V.

When the AD7607 is configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin. For applications using multiple AD7607 devices, the following configurations are recommended, depending on the application requirements.

External Reference Mode

One ADR421 external reference can be used to drive the REFIN/REFOUT pins of all AD7607 devices (see Figure 37). In this configuration, each REFIN/REFOUT pin of the AD7607 should be decoupled with a 100 nF decoupling capacitor.

Internal Reference Mode

One AD7607 device, configured to operate in the internal reference mode, can be used to drive the remaining AD7607 devices, which are configured to operate in external reference mode (see Figure 38). The REFIN/REFOUT pin of the AD7607, configured in internal reference mode, should be decoupled using a 10 µF ceramic decoupling capacitor. The other AD7607 devices, configured in external reference mode, should use a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

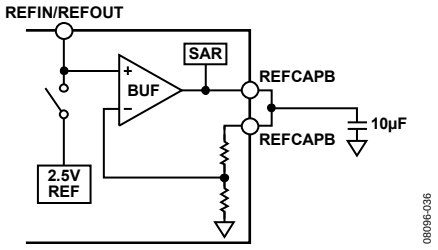


Figure 36. Reference Circuitry

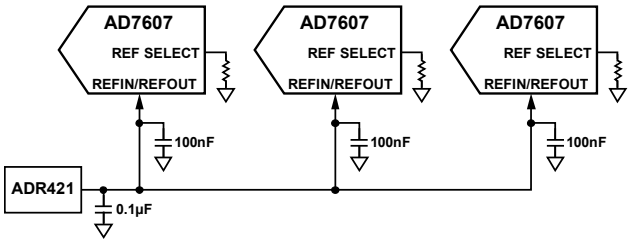


Figure 37. Single External Reference Driving Multiple AD7607 REFIN Pins

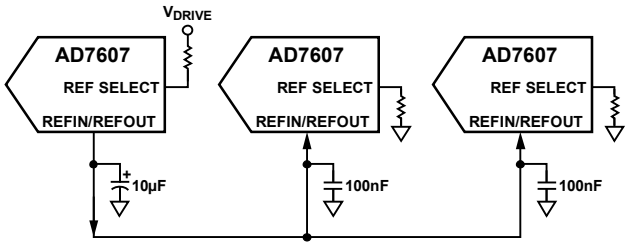


Figure 38. Internal Reference Driving Multiple AD7607 REFIN Pins.

TYPICAL CONNECTION DIAGRAM

Figure 39 shows the typical connection diagram for the AD7607. There are four AV_{CC} supply pins on the part, and each of the four pins should be decoupled using a 100 nF capacitor at each supply pin and a 10 µF capacitor at the supply source. The AD7607 can operate with the internal reference or an externally applied reference. In this configuration, the AD7607 is configured to operate with the internal reference. When using a single AD7607 device on the board, the REFIN/REFOUT pin should be decoupled with a 10 µF capacitor. When using an application with multiple AD7607 devices, refer to the Internal/External Reference section. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 µF ceramic capacitor.

The V_{DRIVE} supply is connected to the same supply as the processor. The V_{DRIVE} voltage controls the voltage value of the output logic signals. For layout, decoupling, and grounding hints, see the Layout Guidelines section.

POWER-DOWN MODES

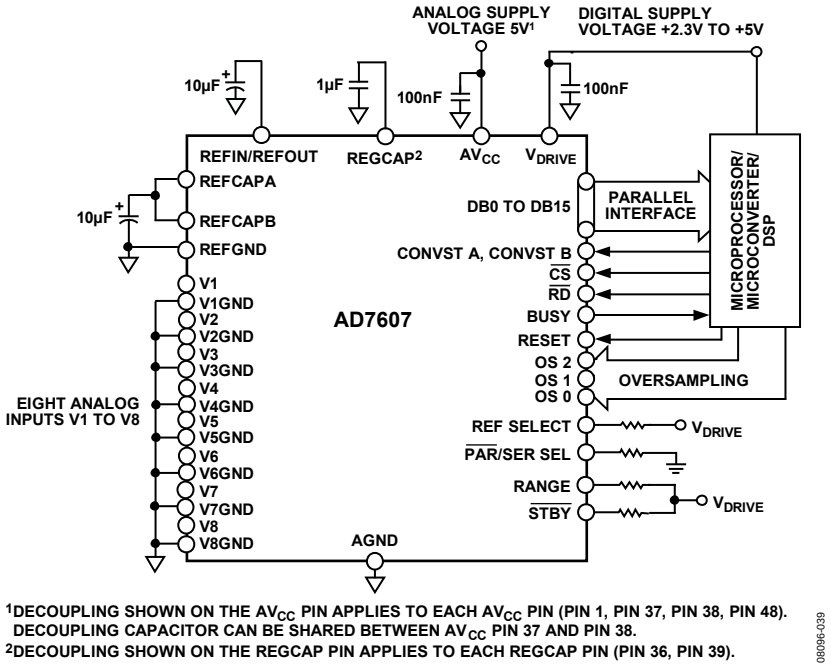
Two power-down modes are available on the AD7607: standby mode and shutdown mode. The $\overline{STBY}$ pin controls whether the AD7607 is in normal mode or in one of the two power-down modes.

The power-down mode is selected through the state of the RANGE pin when the $\overline{STBY}$ pin is low. Table 7 shows the configurations required to choose the desired power-down mode. When the AD7607 is placed in standby mode, current consumption is 8 mA maximum and power-up time is approximately 100 µs because the capacitor on the REFCAPA and REFCAPB pins must charge up. In standby mode, the on-chip reference and regulators remain powered up, and the amplifiers and ADC core are powered down.

When the AD7607 is placed in shutdown mode, current consumption is 6 µA maximum and power-up time is approximately 13 ms (external reference mode). In shutdown mode, all circuitry is powered down. When the AD7607 is powered up from shutdown mode, a RESET signal must be applied to the AD7607 after the required power-up time has elapsed.

Table 7. Power-Down Mode Selection

Power-Down Mode	$\overline{STBY}$	RANGE
Standby	0	1
Shutdown	0	0



1DECOUPLING SHOWN ON THE AV_{CC} PIN APPLIES TO EACH AV_{CC} PIN (PIN 1, PIN 37, PIN 38, PIN 48). DECOUPLING CAPACITOR CAN BE SHARED BETWEEN AV_{CC} PIN 37 AND PIN 38.
2DECOUPLING SHOWN ON THE REGCAP PIN APPLIES TO EACH REGCAP PIN (PIN 36, PIN 39).

Figure 39. Typical Connection Diagram

CONVERSION CONTROL

Simultaneous Sampling on All Analog Input Channels

The AD7607 allows simultaneous sampling of all analog input channels. All channels are sampled simultaneously when both CONVST pins (CONVST A, CONVST B) are tied together. A single CONVST signal is used to control both CONVST x inputs. The rising edge of this common CONVST signal initiates simultaneous sampling on all analog input channels.

The AD7607 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all ADC channels is t_{CONV}. The BUSY signal indicates to the user when conversions are in progress, so when the rising edge of CONVST is applied, BUSY goes logic high and transitions low at the end of the entire conversion process. The falling edge of the BUSY signal is used to place all eight track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data can now be read from the parallel bus (DB[15:0]), the $D_{OUT}A$ and $D_{OUT}B$ serial data lines, or the parallel byte bus (DB[7:0]).

Simultaneously Sampling Two Sets of Channels

The AD7607 also allows the analog input channels to be sampled simultaneously in two sets. This can be used in power-line protection and measurement systems to compensate for phase differences between current and voltage sensors. In a 50 Hz system, this allows for up to 9° of phase compensation; and in a 60 Hz system, it allows for up to 10° of phase compensation.

This is accomplished by pulsing the two CONVST pins independently and is possible only if oversampling is not in use. CONVST A is used to initiate simultaneous sampling of the first set of channels (V1 to V4), and CONVST B is used to initiate simultaneous sampling on the second set of analog input channels (V5 to V8), as illustrated in Figure 40.

On the rising edge of CONVST A, the track-and-hold amplifiers for the first set of channels are placed into hold mode. On the rising edge of CONVST B, the track-and-hold amplifiers for the second set of channels are placed into hold mode. The conversion process begins when both rising edges of CONVST x have occurred; therefore, BUSY goes high on the rising edge of the later CONVST x signal. In Table 3, Time t_5 indicates the maximum allowable time between CONVST x sampling points.

There is no change to the data read process when using two separate CONVST x signals.

Connect all unused analog input channels to AGND. The results for any unused channels are still included in the data read because all channels are always converted.

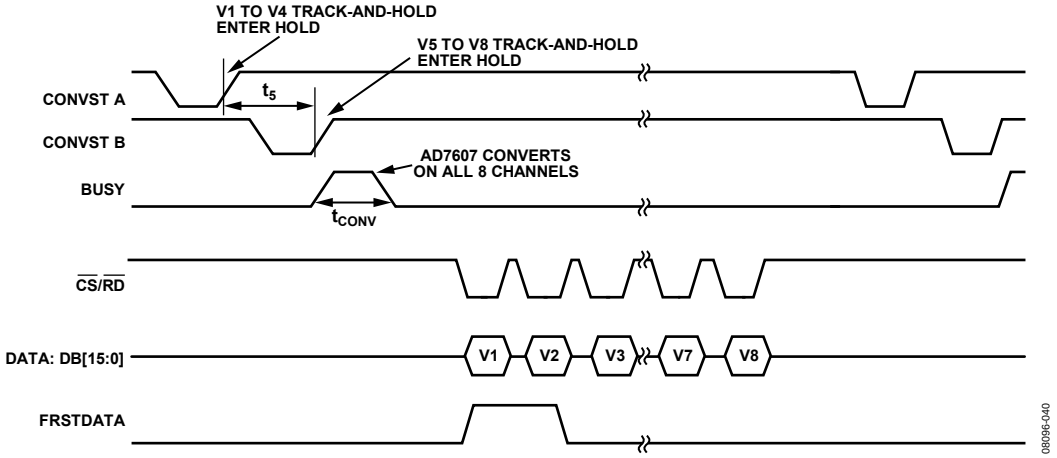


Figure 40. Simultaneous Sampling on Channel Sets While Using Independent CONVST A and CONVST B Signals—Parallel Interface Mode

DIGITAL INTERFACE

The AD7607 provides three interface options: a parallel interface, a high speed serial interface, and a parallel byte interface. The required interface mode is selected via the PAR/SER/BYTE SEL and the DB15/BYTE SEL pins.

Table 8. Interface Mode Selection

PAR/SER/BYTE SEL	DB15	Interface Mode
0	0	Parallel interface mode
1	0	Serial interface mode
1	1	Parallel byte interface mode

Interface mode operation is discussed in the following sections.

PARALLEL INTERFACE (PAR/SER/BYTE SEL = 0)

Data can be read from the AD7607 via the parallel data bus with standard CS and RD signals. To read the data over the parallel bus, the PAR/SER/BYTE SEL pin should be tied low. The CS and RD input signals are internally gated to enable the conversion result onto the data bus. The data lines, DB15 to DB0, leave their high impedance state when both CS and RD are logic low. When CS and RD are low, DB15 and DB14 are used to output a sign extended bit of the MSB (DB13) of the conversion result.

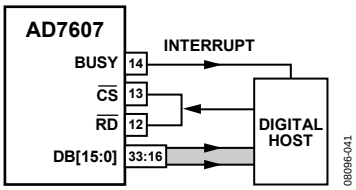


Figure 41. Interface Diagram—One AD7607 Using the Parallel Bus, with CS and RD Shorted Together

The rising edge of the CS input signal tristates the bus, and the falling edge of the CS input signal takes the bus out of the high impedance state. CS is the control signal that enables the data lines; it is the function that allows multiple AD7607 devices to share the same parallel data bus.

The CS signal can be permanently tied low, and the RD signal can be used to access the conversion results as shown in Figure 4. A read operation of new data can take place after the BUSY signal goes low (see Figure 2); or, alternatively, a read operation of data from the previous conversion process can take place while BUSY is high (see Figure 3).

The RD pin is used to read data from the output conversion results register. Applying a sequence of RD pulses to the RD pin of the AD7607 clocks the conversion results out from each channel onto the parallel output bus, DB[15:0], in ascending order. The first RD falling edge after BUSY goes low clocks out the conversion result from Channel V1. The next RD falling edge updates the bus with the V2 conversion result, and so on. The eighth falling edge of RD clocks out the conversion result for Channel V8. When the RD signal is logic low, it enables the data conversion result from each channel to be transferred to the digital host (DSP, FPGA).

When there is only one AD7607 in a system/board and it does not share the parallel bus, data can be read using just one control signal from the digital host. The CS and RD signals can be tied together, as shown in Figure 5. In this case, the data bus comes out of three-state on the falling edge of CS/RD. The combined CS and RD signal allows the data to be clocked out of the AD7607 and to be read by the digital host. In this case, CS is used to frame the data transfer of each data channel.

PARALLEL BYTE INTERFACE (PAR/SER/BYTE SEL = 1, DB15 = 1)

Parallel byte interface mode operates much like the parallel interface mode, except that each channel conversion result is read out in two 8-bit transfers. Therefore, 16 RD pulses are required to read all eight conversion results from the AD7607. To configure the AD7607 to operate in parallel byte interface mode, the PAR/SER/BYTE SEL and BYTE SEL/DB15 pins should be tied to logic high (see Table 8). DB[7:0] are used to transfer the data to the digital host. DB0 is the LSB of the data transfer, and DB7 is the MSB of the data transfer. In parallel byte mode, DB14 acts as an HBEN pin. When the DB14/HBEN pin is tied to logic high, the most significant byte (MSB) of the conversion result is output first, followed by the LSB byte of the conversion result. When DB14/HBEN is tied to logic low, the LSB byte of the conversion result is output first, followed by the MSB byte of the conversion result. The FRSTDATA pin remains high until the entire 14 bits of the conversion result from V1 is read. If the MSB byte is always to be read first, the HBEN pin should be set high and remain high. If the LSB byte is always to be read first, the HBEN pin should be set low and remain low. In this circumstance, the MSB byte contains two sign extended bits in the two MSB positions.

SERIAL INTERFACE (PAR/SER/BYTE SEL = 1)

To read data back from the AD7607 over the serial interface, the PAR/SER/BYTE SEL pin must be tied high. The CS and SCLK signals are used to transfer data from the AD7607. The AD7607 has two serial data output pins, $D_{OUT}A$ and $D_{OUT}B$. Data can be read back from the AD7607 using one or both of these D_{OUT} lines. For the AD7607, conversion results from Channel V1 to Channel V4 first appear on $D_{OUT}A$, and conversion results from Channel V5 to Channel V8 first appear on $D_{OUT}B$.

The CS falling edge takes the data output lines, $D_{OUT}A$ and $D_{OUT}B$, out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, $D_{OUT}A$ and $D_{OUT}B$. The CS input can be held low for the entire serial read, or it can be pulsed to frame each channel read of 14 SCLK cycles.

Figure 42 shows a read of eight simultaneous conversion results using two D_{OUT} lines on the AD7607. In this case, a 56 SCLK transfer is used to access data from the AD7607, and $\overline{CS}$ is held low to frame the entire 56 SCLK cycles. Data can also be clocked out using just one D_{OUT} line; in which case, it is recommended that $D_{OUT}A$ be used to access all conversion data because the channel data is output in ascending order. For the AD7607 to access all eight conversion results on one D_{OUT} line, a total of 112 SCLK cycles are required. These 112 SCLK cycles can be framed by one $\overline{CS}$ signal, or each group of 14 SCLK cycles can be individually framed by the $\overline{CS}$ signal. The disadvantage of using just one D_{OUT} line is that the throughput rate is reduced if reading occurs after conversion. The unused D_{OUT} line should be left unconnected in serial mode. If $D_{OUT}B$ is to be used as a single D_{OUT} line, the channel results are output in the following order: V5, V6, V7, V8, V1, V2, V3, and V4; however, the FRSTDATA indicator returns low after V5 is read on $D_{OUT}B$.

Figure 6 shows the timing diagram for reading one channel of data, framed by the $\overline{CS}$ signal, from the AD7607 in serial mode. The SCLK input signal provides the clock source for the serial read operation. The $\overline{CS}$ goes low to access the data from the AD7607. The falling edge of $\overline{CS}$ takes the bus out of three-state and clocks out the MSB of the 14-bit conversion result. This MSB is valid on the first falling edge of the SCLK after the $\overline{CS}$ falling edge.

The subsequent 13 data bits are clocked out of the AD7607 on the SCLK rising edge. Data is valid on the SCLK falling edge. To access each conversion result, 14 clock cycles must be provided.

The FRSTDATA output signal indicates when the first channel, V1, is being read back. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. In serial mode, the falling edge of $\overline{CS}$ takes FRSTDATA out of three-state and sets the FRSTDATA pin high, indicating that the result from V1 is available on the $D_{OUT}A$ output data line. The FRSTDATA output returns to a logic low following the 14th SCLK falling edge. If all channels are read on $D_{OUT}B$, the FRSTDATA output does not go high when V1 is output on this serial data output pin. It goes high only when V1 is available on $D_{OUT}A$ (and this is when V5 is available on $D_{OUT}B$).

READING DURING CONVERSION

Data can be read from the AD7607 while BUSY is high and the conversions are in progress. This has little effect the performance of the converter, and it allows a faster throughput rate to be achieved. A parallel, parallel byte, or serial read can be performed during conversions and when oversampling is or is not enabled. Figure 3 shows the timing diagram for reading while BUSY is high in parallel or serial mode. Reading during conversions allows the full throughput rate to be achieved when using the serial interface with V_{DRIVE} above 3.3 V.

Data can be read from the AD7607 at any time other than on the falling edge of BUSY because this is when the output data registers get updated with the new conversion data. Time t_6, as outlined in Table 3, should be observed in this condition.

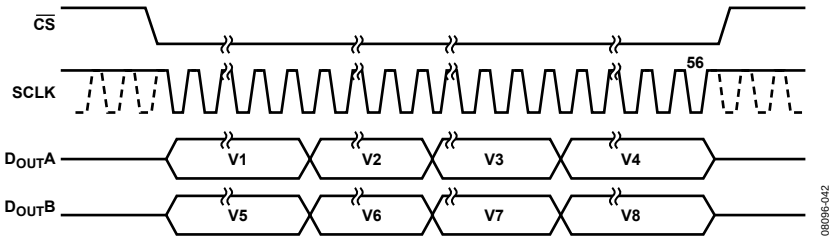


Figure 42. Serial Interface with Two D_{OUT} Lines

DIGITAL FILTER

The AD7607 contains an optional first-order digital sinc filter that should be used in applications where slower throughput rates are used and digital filtering is required. The oversampling ratio of the digital filter is controlled using the oversampling pins, OS[2:0] (see Table 9). OS 2 is the MSB control bit, and OS 0 is the LSB control bit. Table 9 lists the oversampling bit decoding to select the different oversample rates. The OS pins are latched on the falling edge of BUSY. This sets the oversampling rate for the next conversion (see Figure 43).

Selection of the oversampling mode has the effect of adding a digital filter function after the ADC. The different oversampling rates and the CONVST x sampling frequency produce different digital filter frequency profiles.

Table 9. Oversample Bit Decoding

OS[2:0]	Oversampling Ratio	3 dB BW, 5 V Range (kHz)	3 dB BW, 10 V Range (kHz)	Maximum Throughput, CONVST Frequency (kHz)
000	No oversampling	15	22	200
001	2	15	22	100
010	4	13.7	18.5	50
011	8	10.3	11.9	25
100	16	6	6	12.5
101	32	3	3	6.25
110	64	1.5	1.5	3.125
111	Invalid			

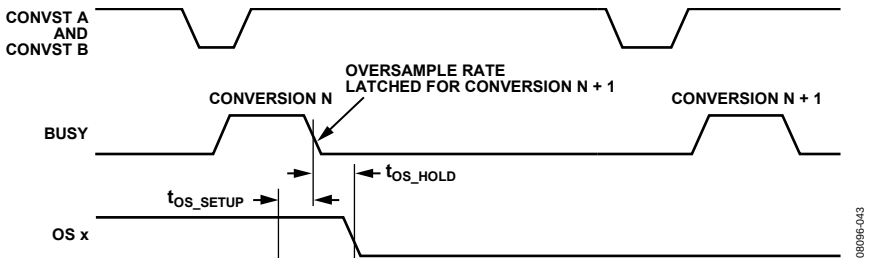


Figure 43. OS x Pin Timing

Figure 44 to Figure 49 show the digital filter frequency profiles for the different oversampling ratios. The combination of the analog antialiasing filter and the oversampling digital filter helps to reduce the complexity of the design of the filter before the AD7607. The digital filtering combines steep roll-off and linear phase response.

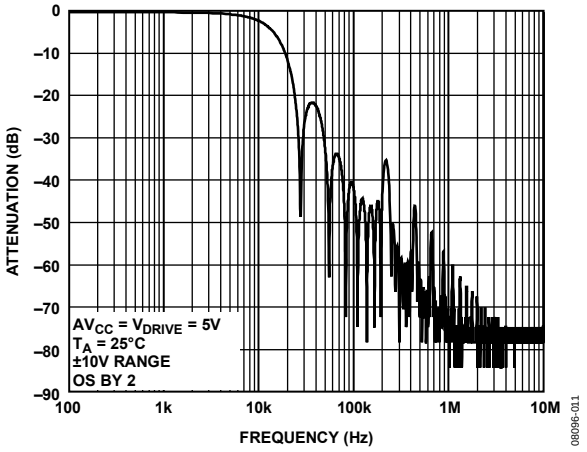


Figure 44. Digital Filter Response for Oversampling by 2

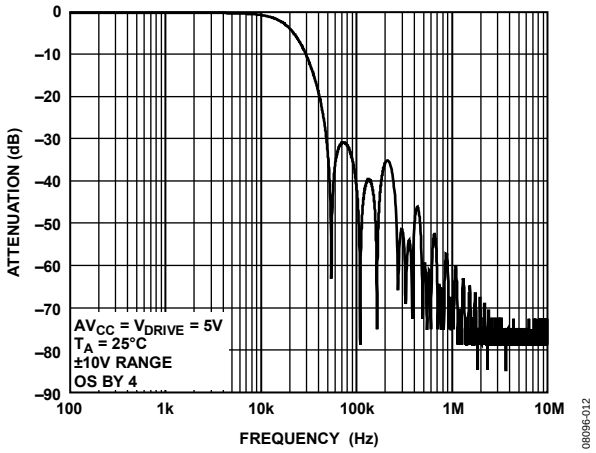


Figure 45. Digital Filter Response for Oversampling by 4

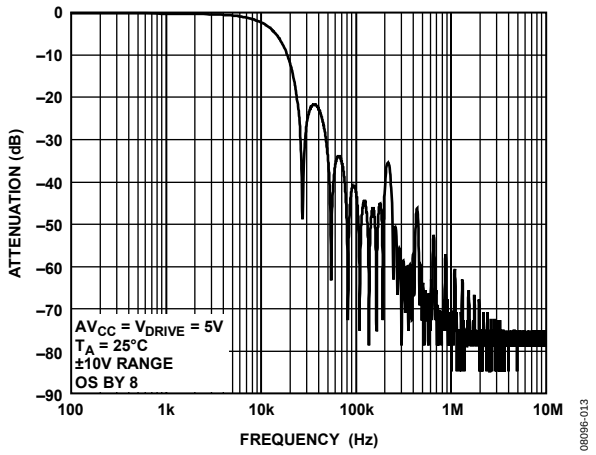


Figure 46. Digital Filter Response for Oversampling by 8

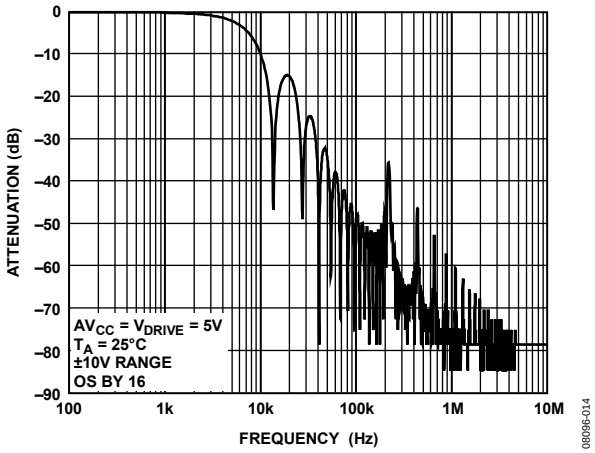


Figure 47. Digital Filter Response for Oversampling by 16

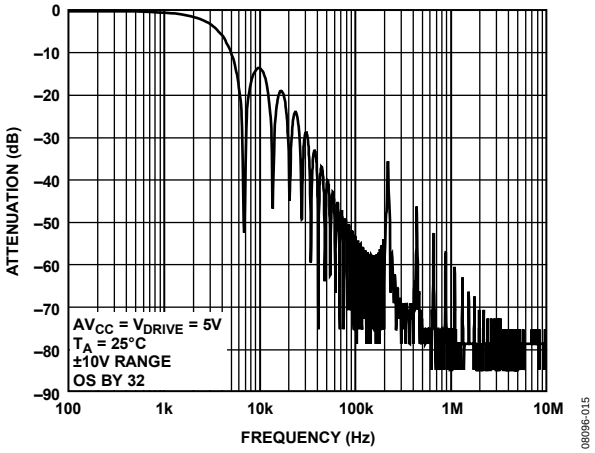


Figure 48. Digital Filter Response for Oversampling by 32

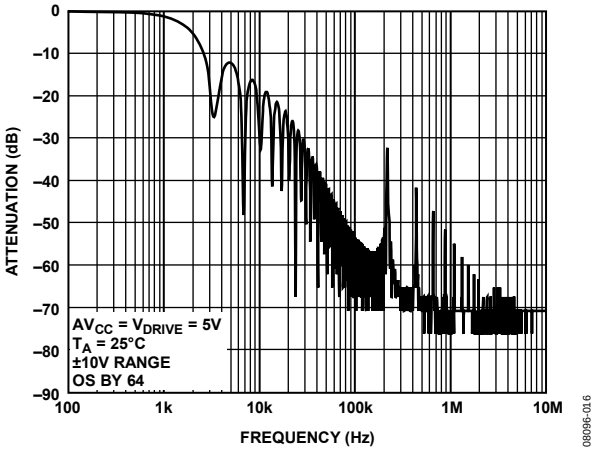


Figure 49. Digital Filter Response for Oversampling by 64

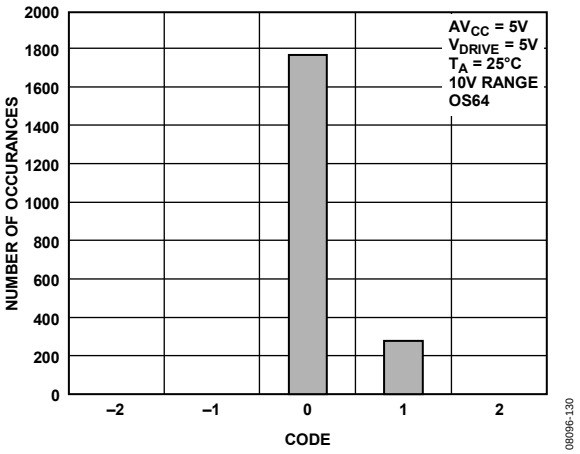


Figure 50. Histogram of Codes, Oversampling by 64

If the OS[2:0] pins are set to select an oversampling ratio of 8, for example, the next CONVST x rising edge takes the first sample for each channel. The remaining seven samples for all channels are taken with an internally generated sampling signal. As the oversampling ratio is increased, the 3 dB frequency is reduced and the allowed sampling frequency is also reduced (see Table 9). The OS[2:0] pins should be configured to suit the filtering requirements of the application.

The CONVST A and CONVST B pins must be tied/driven together when oversampling is turned on. When the oversampling function is turned on, the BUSY high time for the conversion process extends. The actual BUSY high time depends on the oversampling rate that is selected: the higher the oversampling rate, the longer the BUSY high or total conversion time (see Table 3).

Figure 51 shows that the conversion time extends as the oversampling rate is increased. To achieve the fastest throughput rate possible when oversampling is turned on, the read can be performed during the BUSY high time. The falling edge of BUSY is used to update the output data registers with the new conversion data; therefore, the reading of conversion data should not occur on this edge.

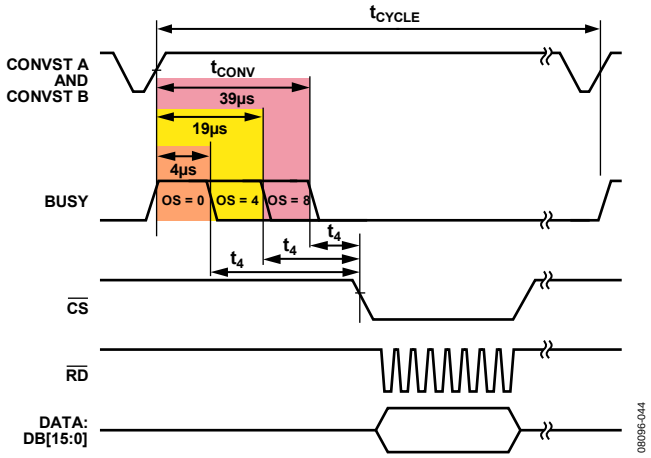


Figure 51. No Oversampling, Oversampling by 4, and Oversampling by 8 Using Read After Conversion

LAYOUT GUIDELINES

The printed circuit board that houses the AD7607 should be designed so that the analog and digital sections are separated and confined to different areas of the board.

At least one ground plane should be used. It can be common or split between the digital and analog sections. In the case of the split plane, the digital and analog ground planes should be joined in only one place, preferably as close as possible to the AD7607.

If the AD7607 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at only one point: a star ground point that should be established as close as possible to the AD7607. Good connections should be made to the ground plane. Avoid sharing one connection for multiple ground pins. Use individual vias or multiple vias to the ground plane for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. The analog ground plane should be allowed to run under the AD7607 to avoid noise coupling. Fast switching signals like CONVST A, CONVST B, or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and they should never run near analog signal paths. Avoid crossover of digital and analog signals. Traces on layers in close proximity on the board should run at right angles to each other to reduce the effect of feedthrough through the board.

The power supply lines to the AV_{CC} and V_{DRIVE} pins should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Where possible, use supply planes and make good connections between the AD7607 supply pins and the power tracks on the board. Use a single via or multiple vias for each supply pin.

Good decoupling is also important in lowering the supply impedance presented to the AD7607 and in reducing the magnitude of the supply spikes. The decoupling capacitors should be placed close to (ideally, right up against) these pins and their corresponding ground pins. Place the decoupling capacitors for the REFIN/REFOUT pin and the REFCAPA and REFCAPB pins as close as possible to their respective AD7607 pins; and, where possible, they should be placed on the same side of the board as the AD7607 device.

Figure 52 shows the recommended decoupling on the top layer of the AD7607 board. Figure 53 shows bottom layer decoupling, which is used for the four AV_{CC} pins and the V_{DRIVE} pin.

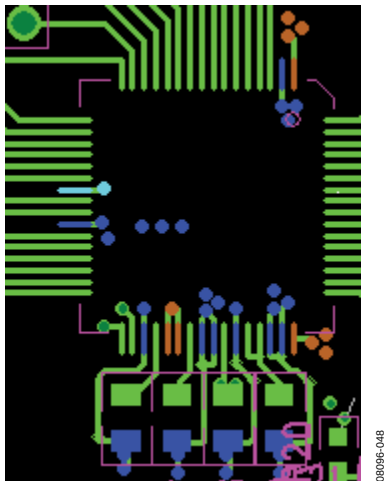


Figure 52. Top Layer Decoupling REFIN/REFOUT, REFCAPA, REFCAPB, and REGCAP Pins

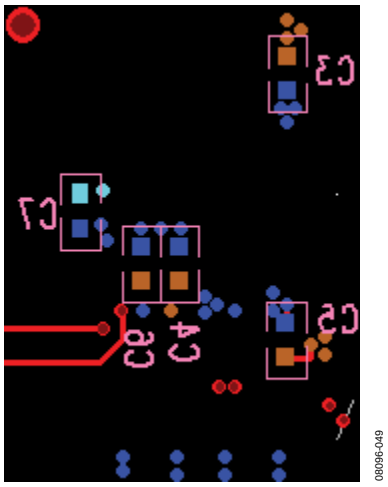


Figure 53. Bottom Layer Decoupling

To ensure good device-to-device performance matching in a system that contains multiple AD7607 devices, a symmetrical layout between the devices is important.

Figure 54 shows a layout with two AD7607 devices. The AV_{CC} supply plane runs to the right of both devices. The V_{DRIVE} supply track runs to the left of the two AD7607 devices. The reference chip is positioned between the two AD7607 devices, and the reference voltage track runs north to Pin 42 of U1 and south to Pin 42 of U2. A solid ground plane is used. These symmetrical layout principles can also be applied to a system that contains more than two AD7607 devices. The AD7607 devices can be placed in a north-south direction with the reference voltage located midway between the AD7607 devices and the reference track running in the north-south direction, similar to Figure 54.

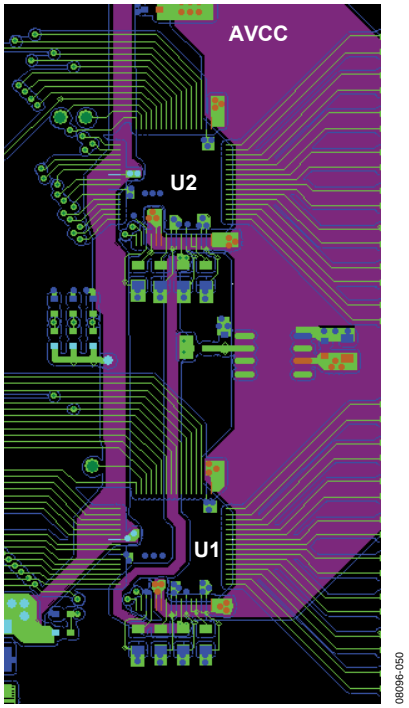


Figure 54. Layout for Multiple AD7607 Devices—Top Layer and Supply Plane Layer

OUTLINE DIMENSIONS

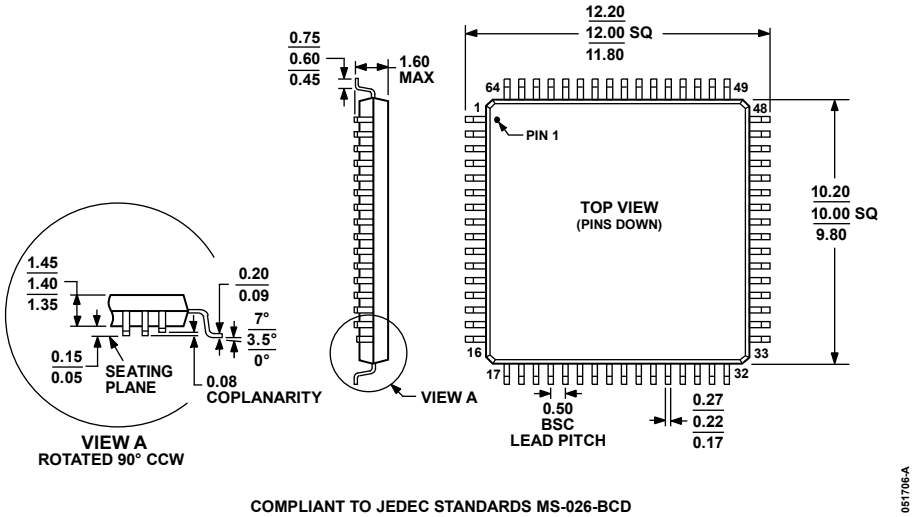


Figure 55. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7607BSTZ	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7607BSTZ-RL	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-AD7607EDZ	−40°C to +85°C	Evaluation Board	
CED1Z		Converter Evaluation Development	

[1] Z = RoHS Compliant Part.