4.8 kHz Ultra-Low Noise 24-Bit Sigma-Delta ADC with PGA

Preliminary Technical Data

AD7192

FEATURES

RMS Noise: 14 nV @ 7.5 Hz (gain = 128)
15.5 noise free bits @ 2.4 kHz (gain = 128)
Up to 22 noise free bits (gain = 1)
Offset drift: 5 nV/°C
Gain drift: 1 ppm/°C
Specified drift over time
Programmable gain (1 – 128)
Output data rate: 4.7 Hz to 4.8 kHz
Internal or external clock
Simultaneous 50 Hz/60 Hz rejection
Four general purpose digital outputs
Power supply: 3 V to 5.25 V
Current: 3.5 mA
Temperature range: –40°C to +105°C

INTERFACE

3-wire serial
SPI®, QSPI™, MICROWIRE™, and DSP compatible
Schmitt trigger on SCLK

APPLICATIONS

Weigh scales
Strain gauge transducers
Pressure measurement
Temperature measurement
Chromatography
PLC/DCS Analog Input Modules
Data Acquisition
Medical and Scientific instrumentation

GENERAL DESCRIPTION

The AD7192 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit Σ-Δ ADC. The on-chip low noise gain stage means that signals of small amplitude can be interfaced directly to the ADC.

The device can be configured to have two differential inputs or four pseudo-differential inputs. The device can be operated with either the internal clock or an external clock. The output data rate from the part can be varied from 4.7 Hz to 4.8 kHz.

The device can be operated with a $sinc^3$ or a $sinc^4$ digital filter. At the lower output data rates, the $sinc^3$ is useful to optimize the settling time. The benefit of the $sinc^4$ at low output data rates is the superior 50 Hz/60 Hz rejection. At the higher output data rates, the $sinc^4$ filter gives best noise performance. For applications that require all conversions to be settled, the AD7192 includes a zero-latency feature.

The part operates with a power supply from 3 V to 5.25 V. It consumes a current of 3.5 mA. It is housed in a 24-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM

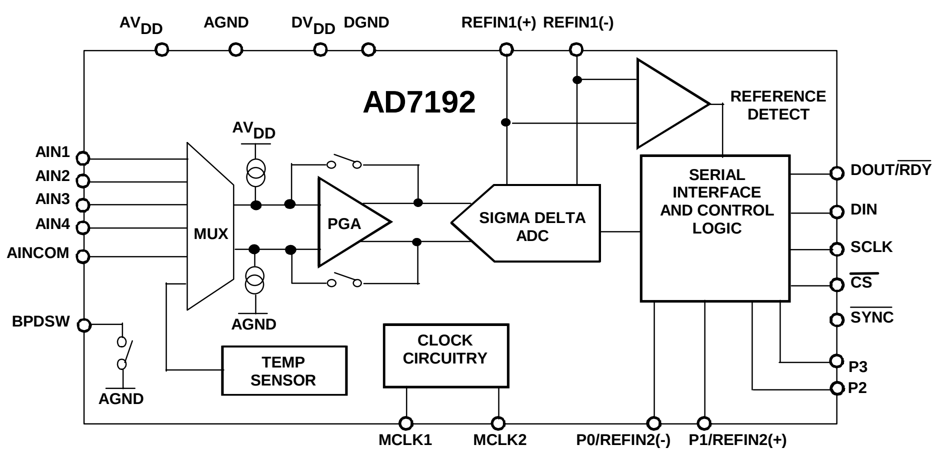

Figure 1.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

SPECIFICATIONS

AV_{DD} = 3 V to 5.25 V; DV_{DD} = 2.7 V to 5.25 V; GND = 0 V; REFIN1(+) = AV_{DD} ; REFIN1(-) = GND; MCLK = 4.9152 MHz; Sinc[4] filter selected; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	AD7192B	Unit	Test Conditions/Comments
Output Data Rate	4.7 to 4800	Hz nom	Chop Disabled
	1.17 to 1200	Hz nom	Chop Enabled
No Missing Codes[2]	24	Bits min	FS > 1
Resolution	See RMS Noise and Resolution Specifications		
RMS Noise and Update Rates	See RMS Noise and Resolution Specifications		
Integral Nonlinearity	±15	ppm of FSR max	
Offset Error[3]	±100/Gain	µV typ	Chop Disabled
	±0.5	µV typ	Chop Enabled
Offset Error Drift vs. Temperature[4]	±150/Gain	nV/°C typ	Gain = 1 to 16. Chop Disabled
	±10	nV/°C typ	Gain = 32 to 128. Chop Disabled
	±5	nV/°C typ	Chop Enabled
Offset Error Drift vs. Time	25	nV/1000 Hours typ	
Full-Scale Error[3, 5]	±10	µV typ	
Gain Drift vs. Temperature[4]	±1	ppm/°C typ	
Gain Drift vs. Time	10	ppm/1000 Hours typ	
Power Supply Rejection	100	dB min	V_{IN} = 1 V/Gain. 120 dB typical.
ANALOG INPUTS			
Differential Input Voltage Ranges	± V_{REF}/gain	V nom	V_{REF} = REFIN(+) − REFIN(−) , gain = 1 to 128
	± (AV_{DD} − 1V)/gain	V min/max	gain > 1
Absolute AIN Voltage Limits[2]			
Unbuffered Mode	GND − 50 mV	V min	
	AV_{DD} + 50 mV	V max	
Buffered Mode	GND + 200 mV	V min	
	AV_{DD} − 200 mV	V max	
Analog Input Current			
Buffered Mode			
Input Current[2]	±1	nA max	Gain = 1
	±3	nA typ	Gain > 1
Input Current Drift	±2	pA/°C typ	
Unbuffered Mode			
Input Current	±5	µA/V typ	Gain = 1. Input current varies with input voltage
	±1	µA/V typ	Gain > 1.
Input Current Drift	±50	pA/V/°C typ	
Normal Mode Rejection[2]			
@ 50 Hz, 60 Hz	98	dB min	10 Hz Output Date Rate, 50 ± 1 Hz, 60 ± 1 Hz
	TBD	dB min	50 Hz Output Date Rate, REJ60[6] = 1, 50 ± 1 Hz, 60 ± 1 Hz
@ 50 Hz	TBD	dB min	50 Hz Output Date Rate, 50 ± 1 Hz
@ 60 Hz	TBD	dB min	60 Hz Output Date Rate, 60 ± 1 Hz
Common-Mode Rejection			
@ DC	100	dB min	AIN = 1 V/gain
@ 50 Hz, 60 Hz[2]	100	dB min	10 Hz Output Date Rate, 50 ± 1 Hz, 60 ± 1 Hz
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz (50 Hz Output Date Rate), 60 ± 1 Hz (60 Hz Output Date Rate)
REFERENCE INPUT			

Parameter[1]	AD7192B	Unit	Test Conditions/Comments
REFIN Voltage	AV_{DD}	V nom	REFIN = REFIN(+) – REFIN(–)
Reference Voltage Range[2]	1	V min	
	AV_{DD}	V max	The differential input must be limited to ± (AV_{DD} – 1V)/gain when gain > 1
Absolute REFIN Voltage Limits[2]	GND – 50 mV	V min	
	AV_{DD} + 50 mV	V max	
Average Reference Input Current	6	µA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	
Normal Mode Rejection[2]	Same as for analog inputs		
Common-Mode Rejection	100	dB typ	
Reference Detect Levels	0.3	V min	
	0.5	V max	
TEMPERATURE SENSOR			
Accuracy	±2	°C typ	Applies after user-calibration at one temperature
Sensitivity	2800	codes/°C typ	
LOW SIDE POWER SWITCH			
R_{ON}	7	Ω max	AV_{DD} = 5 V
	9	Ω max	AV_{DD} = 3 V
Allowable Current[2]	30	mA max	Continuous Current
BURNOUT CURRENTS			
AIN Current	500	nA nom	
DIGITAL OUTPUTS (P0 – P3)			
V_{OH}, Output High Voltage[2]	AV_{DD} – 0.6	V min	AV_{DD} = 3V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	AV_{DD} = 3V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	AV_{DD} = 5V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	AV_{DD} = 5V, I_{SINK} = 800 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance	10	pF typ	
INTERNAL/EXTERNAL CLOCK			
Internal Clock			
Frequency	4.92 ± 4%	MHz min/max	
Duty Cycle	50:50	% typ	
External Clock/Crystal			
Frequency	4.9152	MHz nom	
	2.4576/5.12	MHz min/max	
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = 3 V
	3.5	V min	DV_{DD} = 5 V
Input Current	±10	µA max	MCLKIN = DV_{DD} or GND
LOGIC INPUTS			
$V_T(+)$	1.4/2	V min/V max	DV_{DD} = 5 V
$V_T(–)$	0.8/1.7	V min/V max	DV_{DD} = 5 V
$V_T(+) – V_T(–)$	0.1/0.17	V min/V max	DV_{DD} = 5 V
$V_T(+)$	0.9/2	V min/V max	DV_{DD} = 3 V
$V_T(–)$	0.4/1.35	V min/V max	DV_{DD} = 3 V
$V_T(+) – V_T(–)$	0.06/0.13	V min/V max	DV_{DD} = 3 V
Input Currents	±10	µA max	V_{IN} = DV_{DD} or GND
LOGIC OUTPUT (DOUT/$\overline{\text{RDY}}$)			
V_{OH}, Output High Voltage[2]	DV_{DD} – 0.6	V min	DV_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 3 V, I_{SINK} = 100 µA

Parameter[1]	AD7192B	Unit	Test Conditions/Comments
V_{OH}, Output High Voltage[2]	4	V min	DV_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset binary		
SYSTEM CALIBRATION[2]			
Full-Scale Calibration Limit	1.05 × FS	V max	
Zero-Scale Calibration Limit	−1.05 × FS	V min	
Input Span	0.8 × FS	V min	
	2.1 × FS	V max	
POWER REQUIREMENTS[7]			
Power Supply Voltage			
AV_{DD} − AGND	3/5.25	V min/max	
DV_{DD} − DGND	2.7/5.25	V min/max	
Power Supply Currents			
AI_{DD} Current	TBD	mA max	Gain = 1, Buffer off
	TBD	mA max	Gain = 8, Buffer off
	TBD	mA max	Gain = 8, Buffer on
	TBD	mA max	Gain = 16 – 128, Buffer off
	TBD	mA max	Gain = 16 – 128, Buffer on
DI_{DD} Current	TBD	mA max	DV_{DD} = 3 V
	1	mA max	DV_{DD} = 5 V
I_{DD} (Power-Down Mode)	1	µA max	

[1] Temperature range: −40°C to +105°C.
[2] Specification is not production tested but is supported by characterization data at initial product release.
[3] Following a calibration, this error will be in the order of the noise for the programmed gain and output data rate selected.
[4] Recalibration at any temperature will remove these errors.
[5] Full-scale error applies to both positive and negative full-scale and applies at the factory calibration conditions (AV_{DD} = 5 V, gain = 1, T_A = 25°C).
[6] REJ60 is a bit in the Mode Register. When the output data rate is set to 50 Hz, setting REJ60 to '1' places a notch at 60 Hz, allowing simultaneous 50 Hz/60 Hz rejection.
[7] Digital inputs equal to DV_{DD} or GND.

TIMING CHARACTERISTICS

AV_{DD} = 3 V to 5.25 V; DV_{DD} = 2.7 V to 5.25 V; GND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = DV_{DD}, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
t_3	100	ns min	SCLK high pulse width
t_4	100	ns min	SCLK low pulse width
Read Operation			
t_1	0	ns min	$\overline{\text{CS}}$ falling edge to DOUT/$\overline{\text{RDY}}$ active time
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_5[5, 6]	10	ns min	Bus relinquish time after $\overline{\text{CS}}$ inactive edge
	80	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{\text{CS}}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{\text{RDY}}$ high
Write Operation			
t_8	0	ns min	$\overline{\text{CS}}$ falling edge to SCLK active edge setup time[4]
t_9	30	ns min	Data valid to SCLK edge setup time
t_{10}	25	ns min	Data valid to SCLK edge hold time
t_{11}	0	ns min	$\overline{\text{CS}}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These numbers are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] SCLK active edge is falling edge of SCLK.
[5] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{\text{RDY}}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{\text{RDY}}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

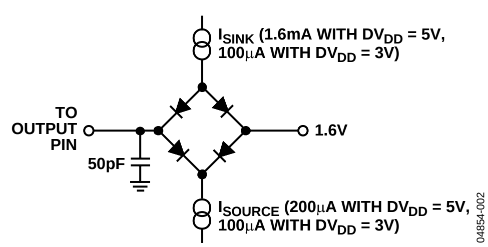

Figure 2. Load Circuit for Timing Characterization

TIMING DIAGRAMS

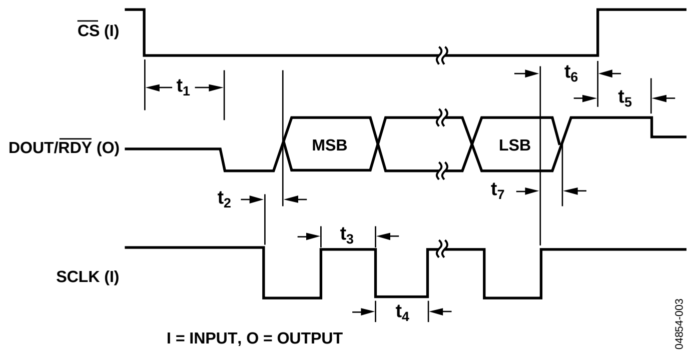

Figure 3. Read Cycle Timing Diagram

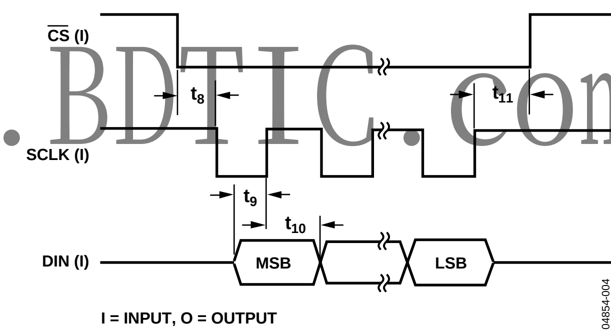

Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +6.5 V
DV_{DD} to GND	−0.3 V to +6.5 V
Analog Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
AIN/Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP	
θ_{JA} Thermal Impedance	97.9°C/W
θ_{JC} Thermal Impedance	14°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

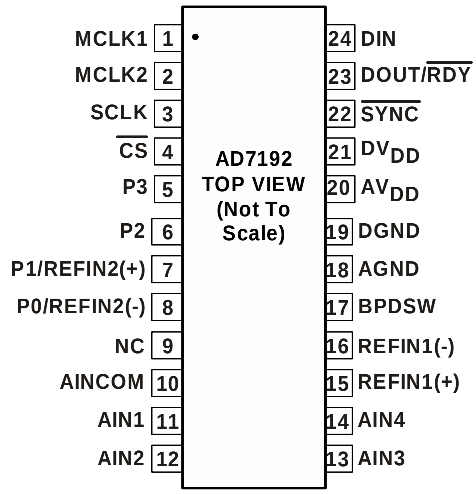

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MCLK1	When the master clock for the device is provided externally by a crystal, the crystal is connected between MCLK1 and MCLK2.
2	MCLK2	Master Clock signal for the device. The AD7192 has an internal 4.92 MHz clock. This internal clock can be made available on the MCLK2 pin. The clock for the AD7192 can be provided externally also in the form of a crystal or external clock. A crystal can be tied across the MCLK1 and MCLK2 pins. Alternatively, the MCLK2 pin can be driven with a CMOS-compatible clock and MCLK1 left unconnected.
3	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
4	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.
5	P3	Digital Output Pin. This pin can function as a general purpose output bit referenced between AV_{DD} and AGND.
6	P2	Digital Output Pin. This pin can function as a general purpose output bit referenced between AV_{DD} and AGND.
7	P1/REFIN2(+)	Digital Output Pin/Positive Reference Input. This pin functions as a general purpose output bit referenced between AV_{DD} and AGND. When REFSEL = 1, this pin functions as REFIN2(+). An external reference can be applied between REFIN2(+) and REFIN2(−). REFIN2(+) can lie anywhere between AV_{DD} and GND + 1 V. The nominal reference voltage, (REFIN2(+) − REFIN2(−)), is AV_{DD}, but the part functions with a reference from 1 V to AV_{DD}.
8	P0/REFIN2(-)	Digital Output Pin/Negative Reference Input. This pin functions as a general purpose output bit referenced between AV_{DD} and AGND. When REFSEL = 1, this pin functions as REFIN2(-). This reference input can lie anywhere between GND and AV_{DD} − 1 V.
9	NC	No Connect. This pin should be tied to AGND.
10	AINCOM	Analog inputs AIN1 to AIN4 are referenced to this input when configured for pseudo-differential operation.
11	AIN1	Analog Input. It can be configured as the positive input of a fully differential input pair when used with AIN2 or as a pseudo-differential input when used with AINCOM.
12	AIN2	Analog Input. It can be configured as the negative input of a fully differential input pair when used with AIN1 or as a pseudo-differential input when used with AINCOM.
13	AIN3	Analog Input. It can be configured as the positive input of a fully differential input pair when used with

Pin No.	Mnemonic	Description
		AIN4 or as a pseudo-differential input when used with AINCOM.
14	AIN4	Analog Input. It can be configured as the negative input of a fully differential input pair when used with AIN3 or as a pseudo-differential input when used with AINCOM.
15	REFIN1(+)	Positive Reference Input. An external reference can be applied between REFIN1(+) and REFIN1(−). REFIN1(+) can lie anywhere between AV_{DD} and GND + 1 V. The nominal reference voltage, (REFIN1(+) − REFIN1(−)), is AV_{DD}, but the part functions with a reference from 1 V to AV_{DD}.
16	REFIN1(−)	Negative Reference Input. This reference input can lie anywhere between GND and AV_{DD} − 1 V.
17	BPDSW	Low Side Power Switch to AGND.
18	AGND	Analog Ground Reference Point.
19	DGND	Digital Ground Reference Point.
20	AV_{DD}	Analog Supply Voltage, 3 V to 5.25 V. AV_{DD} is independent of DV_{DD}. Therefore DV_{DD} can be operated at 3 V with AV_{DD} at 5 V or vice versa.
21	DV_{DD}	Digital Supply Voltage, 2.7 V to 5.25 V. DV_{DD} is independent of AV_{DD}. Therefore AV_{DD} can be operated at 3 V with DV_{DD} at 5 V or vice versa.
22	$\overline{\text{SYNC}}$	Logic Input that allows for synchronization of the digital filters and analog modulators when using a number of AD7192 devices. While $\overline{\text{SYNC}}$ is low, the nodes of the digital filter, the filter control logic and the calibration control logic are reset and the analog modulator is also held in its reset state. $\overline{\text{SYNC}}$ does not affect the digital interface but does reset $\overline{\text{RDY}}$ to a high state if it is low. $\overline{\text{SYNC}}$ has a pull- up resistor internally to DV_{DD}.
23	DOUT/$\overline{\text{RDY}}$	Serial Data Output/Data Ready Output. DOUT/$\overline{\text{RDY}}$serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{\text{RDY}}$operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin will go high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{\text{RDY}}$ pin. With $\overline{\text{CS}}$ low, the data/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge.
24	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC, the register selection bits of the communications register identifying the appropriate register.

RMS NOISE AND RESOLUTION SPECIFICATIONS

The AD7192 can be operated with chop enabled or chop disabled. With chop enabled, the settling time is two times the conversion time. The offset is continuously removed by the ADC leading to low offset and low offset drift. With chop disabled, higher output data rates can be achieved from the ADC. The settling time is three times ($sinc^3$) or four times ($sinc^4$) the selected output data rate. With chop disabled, the offset is not removed by the ADC. The offset and offset drift is comparable between chop enabled and chop disabled for gains of 32 or higher. For lower gains, however, periodic offset calibrations may be required to remove offset due to drift.

SINC^4 FILTER

The $sinc^4$ filter optimizes the 50 Hz/60 Hz rejection. At the higher output data rates, it also gives better rms noise performance compared with the $sinc^3$ filter.

CHOP DISABLED

Table 5 shows the rms noise of the AD7192 for some of the output data rates and gain settings with chop disabled. The numbers given are for the bipolar input range with the external 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 6 shows the effective resolution while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there will be no code flicker. These numbers are typical and are rounded to the nearest half-LSB.

Table 5. RMS Noise (nV) vs. Gain and Output Data Rate(continuous conversion mode) Using a 5 V Reference - Chop Disabled

Filter Word (Decimal)	Output Data Rate(Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	**4.7**	851	350	50	30	18	13	11
640	**7.5**	533	410	60	36	22	16.5	14
480	**10**	400	460	70	40	24	19	17
96	**50**	80	1100	157	90	53	41	37
80	**60**	66.7	1400	183	100	64	46	40
32	**150**	26.7	2360	325	185	110	75	65
16	**300**	13.3	3000	430	240	145	105	93
5	**960**	4.17	4800	700	390	250	185	160
2	**2400**	1.67	7400	1100	640	400	300	260
1	**4800**	0.83	16200	2200	1200	680	465	387

Table 6. Typical Resolution (Bits) vs. Gain and Output Data Rate(continuous conversion mode) Using a 5 V Reference - Chop Disabled

Filter Word (Decimal)	Output Data Rate(Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	**4.7**	851	24 (22)	24 (22)	24 (21.5)	24 (21.5)	23.5 (21)	22.5 (20)
640	**7.5**	533	24 (22)	24 (21.5)	24 (21.5)	23.5 (21)	23 (20.5)	22 (19.5)
480	**10**	400	24 (21.5)	24 (21.5)	23.5 (21)	23.5 (21)	22.5 (20)	22 (19.5)
96	**50**	80	23 (20.5)	22.5 (20)	22.5 (20)	22.5 (20)	21.5 (19)	21 (18.5)
80	**60**	66.7	22.5 (20)	22.5 (20)	22.5 (20)	22 (19.5)	21.5 (19)	20.5 (18)
32	**150**	26.7	22 (19.5)	21.5 (19)	21.5 (19)	21 (18.5)	21 (18.5)	20 (17.5)
16	**300**	13.3	21.5 (19)	21 (18.5)	21 (18.5)	21 (18.5)	20.5 (18)	19.5 (17)
32	**960**	4.17	21 (18.5)	20.5 (18)	20.5 (18)	20 (17.5)	19.5 (17)	18.5 (16)
2	**2400**	1.67	20 (17.5)	20 (17.5)	19.5 (17)	19.5 (17)	19 (16.5)	18 (15.5)
1	**4800**	0.83	19 (16.5)	19 (16.5)	19 (16.5)	18.5 (16)	18 (15.5)	17.5 (15)

CHOP ENABLED

Table 7 shows the AD7192's rms noise for some of the update rates and gain settings. The numbers given are for the bipolar input range with an external 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 8 shows the effective resolution, while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there will be no code flicker. These numbers are typical and are rounded to the nearest half-LSB.

Table 7. RMS Noise (nV) vs. Gain and Output Data Rate(continuous conversion mode) Using a 5 V Reference - Chop Enabled

Filter Word (Decimal)	Output Data Rate(Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	**1.175**	1702	248	36	22	13	10	8
640	**1.875**	1067	290	43	26	16	12	10
480	**2.5**	800	326	50	29	17	14	12
96	**12.5**	160	778	111	64	38	29	27
80	**15**	133	990	130	71	46	33	29
32	**37.5**	53.3	1669	230	131	78	53	46
16	**75**	26.7	2122	304	170	103	75	66
5	**240**	8.33	3395	495	276	177	131	114
2	**600**	3.33	5233	778	453	283	213	184
1	**1200**	1.67	11456	1556	849	481	329	274

Table 8. Typical Resolution (Bits) vs. Gain and Output Data Rate(continuous conversion mode) Using a 5 V Reference - Chop Enabled

Filter Word (Decimal)	Output Data Rate(Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	**1.175**	1702	24 (22.5)	24 (22.5)	24 (22)	24 (22)	24 (21.5)	23 (20.5)
640	**1.875**	1067	24 (22.5)	24 (22)	24 (22)	24 (21.5)	23.5 (21)	22.5 (20)
480	**2.5**	800	24 (22)	24 (22)	24 (21.5)	24 (21.5)	23 (20.5)	22.5 (20)
96	**12.5**	160	23.5 (21)	23 (20.5)	23 (20.5)	23 (20.5)	22 (19.5)	21.5 (19)
80	**15**	133	23 (20.5)	23 (20.5)	23 (20.5)	22.5 (20)	22 (19.5)	21 (18.5)
32	**37.5**	53.3	22.5 (20)	22 (19.5)	22 (19.5)	21.5 (19)	21.5 (19)	20.5 (18)
16	**75**	26.7	22 (19.5)	21.5 (19)	21.5 (19)	21.5 (19)	21 (18.5)	20 (17.5)
5	**240**	8.33	21.5 (19)	21 (18.5)	21 (18.5)	20.5 (18)	20 (17.5)	19 (16.5)
2	**600**	3.33	20.5 (18)	20.5 (18)	20 (17.5)	20 (17.5)	19.5 (17)	18.5 (16)
1	**1200**	1.67	19.5 (17)	19.5 (17)	19.5 (17)	19 (16.5)	18.5 (16)	18 (15.5)

SINC^3 FILTER

For a given update rate, the sinc^3 filter has lower settling time than the sinc^3 filter. At low update rates, the rms noise is comparable between the sinc^3 filter and the sinc^4 filter. So, the user can optimize the settling time without compromising the rms noise. At high update rates, the sinc^4 filter is needed for optimum performance of the AD7192.

CHOP DISABLED

Table 9 shows the rms noise of the AD7192 for some of the update rates and gain settings with chop disabled. The numbers given are for the bipolar input range with the external 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 10 shows the effective resolution while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there will be no code flicker. These numbers are typical and are rounded to the nearest half-LSB.

Table 9. RMS Noise (nV) vs. Gain and Output Data Rate(continuous conversion mode) Using a 5 V Reference - Chop Disabled

Filter Word (Decimal)	Output Data Rate(Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	**4.7**	638	400	56	30	20	15	12
640	**7.5**	400	426	67	36	25	18	15
480	**10**	300	520	76	40	27	20	18
96	**50**	60	1300	176	100	61	47	40
80	**60**	50	1450	200	110	68	49	44
32	**150**	20	2450	348	198	116	81	68
16	**300**	10	3200	454	265	153	114	98
5	**960**	3.13	5600	800	455	275	199	175
2	**2400**	1.25	55800	7100	3600	1750	930	530
1	**4800**	0.625	443000	55400	27500	14000	7000	3500

Table 10. Typical Resolution (Bits) vs. Gain and Output Data Rate(continuous conversion mode) Using a 5 V Reference - Chop Disabled

Filter Word (Decimal)	Output Data Rate(Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	**4.7**	638	24 (22)	24 (21.5)	24 (21.5)	23.5 (21)	23 (20.5)	22.5 (20)
640	**7.5**	400	24 (22)	24 (21.5)	24 (21.5)	23.5 (21)	23 (20.5)	22 (19.5)
480	**10**	300	24 (21.5)	23.5 (21)	23.5 (21)	23 (20.5)	22.5 (20)	22 (19.5)
96	**50**	60	22.5 (20)	22.5 (20)	22.5 (20)	22 (19.5)	21.5 (19)	20.5 (18)
80	**60**	50	22.5 (20)	22.5 (20)	22 (19.5)	22 (19.5)	21.5 (19)	20.5 (18)
32	**150**	20	21.5 (19)	21.5 (19)	21.5 (19)	21 (18.5)	20.5 (18)	20 (17.5)
16	**300**	10	21.5 (19)	21.5 (19)	21 (18.5)	20.5 (18)	20 (17.5)	19.5 (17)
5	**960**	3.13	20.5 (18)	20.5 (18)	20 (17.5)	20 (17.5)	19.5 (17)	18.5 (16)
2	**2400**	1.25	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)	17 (14.5)
1	**4800**	0.625	14 (11.5)	14 (11.5)	14 (11.5)	14 (11.5)	14 (11.5)	14 (11.5)

CHOP ENABLED

Table 11 shows the AD7192's rms noise for some of the update rates and gain settings. The numbers given are for the bipolar input range with an external 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table **12** shows the effective resolution, while the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, while the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there will be no code flicker. These numbers are typical and are rounded to the nearest half-LSB.

Table 11. RMS Noise (nV) vs. Gain and Output Data Rate(continuous conversion mode) Using a 5 V Reference - Chop Enabled

Filter Word (Decimal)	Output Data Rate(Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	**1.56**	1282	283	40	22	15	11	8.5
640	**2.5**	800	302	48	26	18	13	11
480	**3.33**	600	368	54	29	19	15	13
96	**16.6**	120	920	125	71	44	34	29
80	**20**	100	1026	142	78	48	35	32
32	**50**	40	1733	246	140	82	58	48
16	**100**	20	2265	321	188	109	81	70
5	**320**	6.25	3960	566	322	195	141	124
2	**800**	2.5	39460	5100	2550	1240	658	375
1	**1600**	1.25	313300	39200	19500	9900	4950	2475

Table 12. Typical Resolution (Bits) vs. Gain and Output Data Rate(continuous conversion mode) Using a 5 V Reference - Chop Enabled

Filter Word (Decimal)	Output Data Rate(Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
1023	**1.56**	1282	24 (22.5)	24 (22)	24 (22)	24 (21.5)	23.5 (21)	23 (20.5)
640	**2.5**	800	24 (22.5)	24 (22)	24 (22)	24 (21.5)	23.5 (21)	22.5 (20)
480	**3.33**	600	24 (22)	24 (21.5)	24 (21.5)	23.5 (21)	23 (20.5)	22.5 (20)
96	**16.6**	120	23 (20.5)	23 (20.5)	23 (20.5)	22.5 (20)	22 (19.5)	21 (18.5)
80	**20**	100	23 (20.5)	23 (20.5)	22.5 (20)	22.5 (20)	22 (19.5)	21 (18.5)
32	**320**	40	22 (19.5)	22 (19.5)	22 (19.5)	21.5 (19)	21 (18.5)	20.5 (18)
16	**100**	20	22 (19.5)	22 (19.5)	21.5 (19)	21 (18.5)	20.5 (18)	20 (17.5)
5	**320**	6.25	21 (18.5)	21 (18.5)	20.5 (18)	20.5 (18)	20 (17.5)	19 (16.5)
2	**800**	2.5	17.5 (15)	17.5 (15)	17.5 (15)	17.5 (15)	17.5 (15)	17.5 (15)
1	**1600**	1.25	14.5 (12)	14.5 (12)	14.5 (12)	14.5 (12)	14.5 (12)	14.5 (12)

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 6.

Figure 9.

Figure 7.

Figure 10.

Figure 8.

Figure 11.

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise noted.

COMMUNICATIONS REGISTER

(RS2, RS1, RS0 = 0, 0, 0)

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 40 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 13 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	R/$\overline{\text{W}}$(0)	RS2(0)	RS1(0)	RS0(0)	CREAD(0)	0(0)	0(0)

Table 13. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the communications register.
CR6	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation will be a write to a specified register. A 1 in this position indicates that the next operation will be a read from the designated register.
CR5 to CR3	RS2 to RS0	Register Address Bits. These address bits are used to select which registers of the ADC are being selected during this serial interface communication. See Table 14.
CR2	CREAD	Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read, that is, the contents of the data register are automatically placed on the DOUT pin when the SCLK pulses are applied after the $\overline{\text{RDY}}$ pin goes low to indicate that a conversion is complete. The communications register does not have to be written to for subsequent data reads. To enable continuous read, the instruction 01011100 must be written to the communications register. To disable continuous read, the instruction 01011000 must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While continuous read is enabled, the ADC monitors activity on the DIN line so that it can receive the instruction to disable continuous read. Additionally, a reset will occur if 40 consecutive 1s are seen on DIN. Therefore, DIN should be held low until an instruction is to be written to the device.
CR1 to CR0	0	These bits must be programmed to Logic 0 for correct operation.

Table 14. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications Register During a Write Operation	8-bit
0	0	0	Status Register During a Read Operation	8-bit
0	0	1	Mode Register	24-bit
0	1	0	Configuration Register	24-bit
0	1	1	Data Register / Data Register + Status Information	24-bit / 32-bit
1	0	0	ID Register	8-bit
1	0	1	GPOCON Register	8-bit
1	1	0	Offset Register	24-bit
1	1	1	Full-Scale Register	24-bit

STATUS REGISTER

(RS2, RS1, RS0 = 0, 0, 0; Power-On/Reset = 0x80)

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load Bit RS2, Bit RS1, and Bit RS0 with 0. Table 15 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, SR denoting the bits are in the status register. SR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{\text{RDY}}$(1)	ERR(0)	NOREF(0)	PARITY(0)	CHD3(0)	CHD2(0)	CHD1(0)	CHD0(0)

Table 15. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{\text{RDY}}$	Ready Bit for ADC. *Cleared* when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is set automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also set when the part is placed in power-down mode, idle mode or when $\overline{\text{SYNC}}$ is taken low. The end of a conversion is also indicated by the DOUT/$\overline{\text{RDY}}$ pin. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC Error Bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. *Set* to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange, underrange, or the absence of a reference voltage. *Cleared* by a write operation to start a conversion.
SR5	NOREF	No External Reference Bit. *Set* to indicate that the selected reference (REFIN1 or REFIN2) is at a voltage that is below a specified threshold. When set, conversion results are clamped to all ones. *Cleared* to indicate that a valid reference is applied to the selected reference pins. The NOXREF bit is enabled by setting the REF_DET bit in the configuration register to 1. The ERR bit is also set if the voltage applied to the selected reference input is invalid.
SR4	PARITY	Parity Check of Data Register. If the ENPAR bit is set, the PARITY bit is set if there is an odd number of 1s in the data register. It is cleared if there is an even number of 1s in the data register. The DAT_STA bit should be set when the parity check is used. When the DAT_STA bit is set, the contents of the status register are transmitted along with the data for each data register read.
SR3 to SR0	CHD3 to CHD0	These bits indicate which channel corresponds to the data register contents. They do not indicate which channel is presently being converted but indicate which channel was selected when the conversion contained in the data register was being generated.

MODE REGISTER

(RS2, RS1, RS0 = 0, 0, 1; Power-On/Reset = 0x080060)

The mode register is a 24-bit register from which data can be read or to which data can be written. This register is used to select the operating mode, the update rate, and the clock source. Table 16 outlines the bit designations for the mode register. MR0 through MR23 indicate the bit locations, MR denoting the bits are in the mode register. MR23 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Any write to the mode register resets the modulator and filter and sets the $\overline{\text{RDY}}$ bit.

MR23	MR22	MR21	MR20	MR19	MR18	MR17	MR16
MD2(0)	MD1(0)	MD0(0)	DAT_STA(0)	CLK1(1)	CLK0(0)	0	0
MR15	**MR14**	**MR13**	**MR12**	**MR11**	**MR10**	**MR9**	**MR8**
SINC3(0)	0	ENPAR(0)	0	SINGLE(0)	REJ60(0)	FS9(0)	FS8(0)
MR7	**MR6**	**MR5**	**MR4**	**MR3**	**MR2**	**MR1**	**MR0**
FS7(0)	FS6(1)	FS5(1)	FS4(0)	FS3(0)	FS2(0)	FS1(0)	FS0(0)

Table 16. Mode Register Bit Designations

Bit Location	Bit Name	Description
MR23 to MR21	MD2 to MD0	Mode Select Bits. These bits select the operational mode of the AD7192 (see Table 17).
MR20	DAT_STA	Transmit status register contents after each data register read. When DAT_STA is set, the contents of the status register are transmitted along with each data register

<table>
<tr><th>Bit Location</th><th>Bit Name</th><th>Description</th></tr>
<tr><td></td><td></td><td>read. This function is useful when several channels are selected as the status register identifies the channel to which the data register value corresponds.</td></tr>
<tr><td>MR19 to MR18</td><td>CLK1 to CLK0</td><td>These bits are used to select the clock source for the AD7192. Either the on-chip 4.92 MHz clock can be used or an external clock can be used. The ability to use an external clock allows several AD7192 devices to be synchronized. Also, 50 Hz/60 Hz rejection is improved when an accurate external clock drives the AD7192.
<table>
<tr><th>CLK1</th><th>CLK0</th><th>ADC Clock Source</th></tr>
<tr><td>0</td><td>0</td><td>External crystal used. The external crystal is connected from MCLK1 to MCLK2.</td></tr>
<tr><td>0</td><td>1</td><td>External clock used. The external clock is applied to the MCLK2 pin.</td></tr>
<tr><td>1</td><td>0</td><td>Internal 4.92 MHz clock. Pin MCLK2 is tri-stated.</td></tr>
<tr><td>1</td><td>1</td><td>Internal 4.92 MHz clock. The internal clock is available on MCLK2.</td></tr>
</table></td></tr>
<tr><td>MR17 to MR16</td><td>0</td><td>These bits must be programmed with a Logic 0 for correct operation.</td></tr>
<tr><td>MR15</td><td>SINC3</td><td>Sinc3 Filter Select pin.
When this bit is cleared, the sinc^4 filter is used (default value).
When this bit is set, a sinc^3 filter is used.
The benefit of the sinc^3 filter compared to the sinc^4 filter is its lower settling time when chop is disabled. For a given output data rate f_{ADC}, the sinc^3 filter has a settling time of $f_{ADC}/3$ while the sinc^4 filter has a settling time of $f_{ADC}/4$. The sinc^4 filter, due to its deeper notches, gives better 50 Hz/60 Hz rejection.
At low update rates, both filters give similar rms noise and similar no missing codes for a given update rate. At higher update rates (FS values less than 5), the sinc^4 filter gives better performance than the sinc^3 filter for rms noise and no missing codes.</td></tr>
<tr><td>MR14</td><td>0</td><td>This bit must be programmed with a Logic 0 for correct operation.</td></tr>
<tr><td>MR13</td><td>ENPAR</td><td>Enable Parity bit.
When ENPAR is set, parity checking on the data register is enabled. The DAT_STA bit should be set when the parity check is used. When the DAT_STA bit is set, the contents of the status register are transmitted along with the data for each data register read.</td></tr>
<tr><td>MR12</td><td>0</td><td>This bit must be programmed with a Logic 0 for correct operation.</td></tr>
<tr><td>MR11</td><td>SINGLE</td><td>Single Cycle Conversion Enable Bit.
When this bit is set, the AD7192 allows the complete settling time to perform each conversion. So, the device functions as a zero-latency ADC.</td></tr>
<tr><td>MR10</td><td>REJ60</td><td>Enables a notch at 60 Hz when the output data rate is equal to 50 Hz.
When REJ60 is set, a filter notch is placed at 60 Hz when the output data rate selected is 50 Hz. This allows simultaneous 50 Hz/60 Hz rejection.</td></tr>
<tr><td>MR9 to MR0</td><td>FS9 to FS0</td><td>Filter Output Data Rate Select Bits.
The 10 bits of data programmed into these bits determine the filter cut-off frequency, the position of the first notch of the filter and the output data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device. When chop is disabled and continuous conversion mode is selected, the first notch of the filter occurs at a frequency determined by the relationship:
filter first notch frequency = (fmod/64)/FS
where FS is the decimal equivalent of the code in bits FS0 to FS9 and is in the range 1 to 1023 and fmod is the modulator frequency which is equal to MCLK/16. With the nominal MCLK of 4.92 MHz, this results in a first notch frequency range from 4.69 Hz to 4.8 kHz.
Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables 5 through 8 show the effect of the filter notch frequency and gain on the effective resolution of the AD7192. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1.2 kHz, a new word is available every 0.83 ms. The settling time of the filter to a full-scale step input change is worst case (N + 1)/(output data rate) where N = 3 when the sinc^3 filter is selected and N = 4 when the sinc^4 filter is selected. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 100 ms max when N = 4. This settling time can be reduced to N/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the $\overline{\text{SYNC}}$ input low, the settling time will be N/(output data rate) from when $\overline{\text{SYNC}}$ returns high. If a change of channel takes place, the settling time is N/(output data rate) regardless of the $\overline{\text{SYNC}}$ status as the part issues an internal reset command when requested to change channels.
The −3 dB frequency is determined by the programmed first notch frequency according to the</td></tr>
</table>

Bit Location	Bit Name	Description
		relationship: filter –3 dB frequency = 0.23 x filter first notch frequency. When chop is enabled, the output data rate equals Output data rate = (fmod/64)/(NxFS) where FS is the decimal equivalent of the code in bits FS0 to FS9 and is in the range 1 to 1023 and fmod is the modulator frequency which is equal to MCLK/16. With the nominal MCLK of 4.92 MHz, this results in an output data rate from 4.69/N Hz to 4.8/N kHz where N is the order of the sinc filter. The first notch in the frequency response is placed at output data rate/2. The settling time is equal to 2 x conversion time.

Table 17. Operating Modes

MD2	MD1	MD0	Mode
0	0	0	Continuous Conversion Mode (Default). In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. $\overline{RDY}$ goes low when a conversion is complete. The user can read these conversions by setting the CREAD bit in the communications register to '1' which enables continuous read. When continuous read is enabled, the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output each conversion by writing to the communications register. After power-on, a reset or a re-configuration of the ADC, the complete settling time of the filter is required to generate the first valid conversion. Subsequent conversions are available at the selected output data rate which is dependent on filter choice.
0	0	1	Single Conversion Mode. When single conversion mode is selected, the ADC powers up and performs a single conversion on the selected channel. The oscillator requires 1 ms to power up and settle. The ADC then performs the conversion which requires the complete settling time of the filter. The conversion result is placed in the data register, $\overline{RDY}$ goes low, and the ADC returns to power-down mode. The conversion remains in the data register and $\overline{RDY}$ remains active (low) until the data is read or another conversion is performed.
0	1	0	Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided.
0	1	1	Power-Down Mode. In power-down mode, all the AD7192 circuitry, except the power switch, is powered down. The power switch remains active as the user may need to power up the sensor prior to powering up the AD7192 for settling reasons. The external crystal, if present, is left active.
1	0	0	Internal Zero-Scale Calibration. An internal short is automatically connected to the input. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	0	1	Internal Full-Scale Calibration. A full-scale input voltage is automatically connected to the input for this calibration. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed to minimize the full-scale error.
1	1	0	System Zero-Scale Calibration. User should connect the system zero-scale input to the channel input pins as selected by the CH7 to CH0 bits. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured offset coefficient is placed in the offset register of the selected channel.
1	1	1	System Full-Scale Calibration. User should connect the system full-scale input to the channel input pins as selected by the CH7–CH0 bits. $\overline{RDY}$ goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is placed in idle mode following a calibration. The measured full-scale coefficient is placed in the full-scale register of the selected channel. A full-scale calibration is required each time the gain of a channel is changed.

CONFIGURATION REGISTER

(RS2, RS1, RS0 = 0, 1, 0; Power-On/Reset = 0x000117)

The configuration register is a 24-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode, enable or disable the buffer, enable or disable the burnout currents, select the gain, and select the analog input channel.

Table 18 outlines the bit designations for the filter register. CON0 through CON23 indicate the bit locations. CON denotes that the bits are in the configuration register. CON23 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

CON23	**CON22**	**CON21**	**CON20**	**CON19**	**CON18**	**CON17**	**CON16**
CHOP(0)	0(0)	0(0)	REFSEL(0)	0(0)	0(0)	0(0)	(0)
CON15	**CON14**	**CON13**	**CON12**	**CON11**	**CON10**	**CON9**	**CON8**
CH7(0)	CH6(0)	CH5(0)	CH4(0)	CH3(0)	CH2(0)	CH1(0)	CH0(1)
CON7	**CON6**	**CON5**	**CON4**	**CON3**	**CON2**	**CON1**	**CON0**
BURN(0)	REFDET(0)	0(0)	BUF(1)	$U/\overline{B}$ (0)	GN2(1)	GN1(1)	GN0(1)

Table 18. Configuration Register Bit Designations

Bit Location	Bit Name	Description
CON23	CHOP	Chop Enable Bit. When CHOP is cleared, chop is disabled. When CHOP is set, chop is disabled. When chop is enabled, the offset and offset drift is continuously removed by the ADC. However, it increases the conversion time and settling time of the ADC. For example, when FS = 96 decimal and the $sinc^4$ filter is selected, the conversion time with chop enabled equals 80 ms and the settling time equals 160 ms. With chop disabled, higher conversion rates are allowed. For an SF word of 96 decimal and the $sinc^4$ filter selected, the conversion time is 20 ms and the settling time is 80 ms. However, at low gains, periodic calibrations may be required to remove the offset and offset drift.
CON22, CON21	0	These bits must be programmed with a Logic 0 for correct operation.
CON20	REFSEL	Reference Select Bits. The reference source for the ADC is selected using these bits.
		REFSEL — **Reference Voltage** 0 — External reference applied between REFIN1(+) and REFIN1(−) 1 — External reference applied between the P1 and P0 pins.
CON19 to CON16	0	These bits must be programmed with a Logic 0 for correct operation.
CON15 to CON8	CH7 to CH0	Channel Select Bits. These bits are used to select which channels are enabled on the AD7192. See Table 19. Several channels can be selected and the AD7192 will automatically sequence between them. The conversion on each channel will require the complete settling time.
CON7	BURN	When this bit is set to 1 by the user, the 500 nA current sources in the signal path are enabled. When BURN = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer is active.
CON6	REFDET	Enables the Reference Detect Function. When *set*, the NOXREF bit in the status register indicates when the external reference being used by the ADC is open circuit or less than 0.5 V.
CON5	0	This bit must be programmed with a Logic 0 for correct operation.
CON4	BUF	Configures the ADC for buffered or unbuffered mode of operation. If *cleared*, the ADC operates in unbuffered mode, lowering the power consumption of the device. If *set*, the ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system. With the buffer disabled, the voltage on the analog input pins can be from 50 mV below GND to 50 mV above AV_{DD}. When the buffer is enabled, it requires some headroom so the voltage on any input pin must be limited to 200 mV within the power supply rails.

Bit Location	Bit Name	Description
CON3	U/$\overline{\text{B}}$	Polarity Select bit. When this bit is set, unipolar operation is selected. When this but is cleared, bipolar operation is selected.
CON2 to CON0	G2 to G0	Gain Select Bits. Written by the user to select the ADC input range as follows:

G2	G1	G0	Gain	ADC Input Range (5 V Reference)
0	0	0	1	5 V
0	0	1	Reserved	
0	1	0	Reserved	
0	1	1	8	625 mV
1	0	0	16	312.5 mV
1	0	1	32	156.2 mV
1	1	0	64	78.125 mV
1	1	1	128	39.06 mV

Table 19. Channel Selection

CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	Channel	CHD[3:0]	Calibration Pair
X	X	X	X	X	X	X	1	AIN1 – AIN2	0000	0
X	X	X	X	X	X	1	X	AIN3 – AIN4	0001	1
X	X	X	X	X	1	X	X	Temp Sensor	0010	None
X	X	X	X	1	X	X	X	AIN2 – AIN2	0011	0
X	X	X	1	X	X	X	X	AIN1 – AINCOM	0100	0
X	X	1	X	X	X	X	X	AIN2 – AINCOM	0101	1
X	1	X	X	X	X	X	X	AIN3 – AINCOM	0110	2
1	X	X	X	X	X	X	X	AIN4 – AINCOM	0111	3

DATA REGISTER

(RS2, RS1, RS0 = 0, 1, 1; Power-On/Reset = 0x000000)

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the $\overline{\text{RDY}}$ bit/pin is set. The AD7192 can be configured for 24-bit transfers or 32-bit transfers. When 24-bit transfers are selected, the 24-bit data conversion is transmitted. When 32-bit transfers are selected, the 24-bit conversion is followed by the contents of the status register. When several channels are enabled, the ADC will automatically step between channels. So, 32-bit transmissions are required so that the user can identify the channel from which the conversions originated.

GPOCON REGISTER

(RS2, RS1, RS0 = 1, 0, 1; Power-On/Reset = 0x00)

The GPOCON register is an 8-bit register from which data can be read or to which data can be written. This register is used to enable the general purpose digital outputs.

Table 20 outlines the bit designations for the GPOCON register. GP0 through GP7 indicate the bit locations. GP denotes that the bits are in the GPOCON register. GP7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
0(0)	BPDSW(0)	GP32EN(0)	GP10EN(0)	P3DAT(0)	P2DAT(0)	P1DAT(0)	P0DAT(0)

Table 20. Register Bit Designations

Bit Location	Bit Name	Description
GP7	0	This bit must be programmed with a Logic 0 for correct operation.
GP 6	BPDSW	Power Switch Control Bit. *Set* by user to close the power switch BPDSW to AGND. The power switch can sink up to 30 mA. *Cleared* by user to open the power switch. When the ADC is placed in power-down mode, the power switch remains active.
GP5	GP32EN	Digital Outputs P3 and P2 Enable. When GP32EN is set, the digital outputs P3 and P2 are active. When GP32EN is cleared, the pins P3 and P2 are tri-stated and bits P3DAT and P2DAT are ignored.
GP4	GP10EN	Digital Outputs P1 and P0 Enable. When GP10EN is set, the digital outputs P1 and P0 are active. When GP10EN is cleared, the P1 and P0 outputs are tri-stated and bits P1DAT and P0DAT are ignored. The pins P1 and P0 can be used as a reference input REFIN2 when bit REFSEL in the configuration register is set to 1.
GP3	P3DAT	Digital Output P3. When GP32EN is *set*, the P3DAT bit sets the value of the general purpose output pin P3. When P3DAT is high, the output P3 is high. When P3DAT is low, the output P3 is low.
GP2	P2DAT	Digital Output P2. When GP32EN is *set*, the P2DAT bit sets the value of the general purpose output pin P2. When P2DAT is high, the output P2 is high. When P2DAT is low, the output P2 is low.
GP1	P1DAT	Digital Output P1. When GP10EN is *set*, the P1DAT bit sets the value of the general purpose output pin P1. When P1DAT is high, the output P1 is high. When P1DAT is low, the output P1 is low.
GP0	P0DAT	Digital Output P0. When GP10EN is *set*, the P0DAT bit sets the value of the general purpose output pin P0. When P0DAT is high, the output P0 is high. When P0DAT is low, the output P0 is low.

OFFSET REGISTER

(RS2, RS1, RS0 = 1, 1, 0; Power-On/Reset = 0x800000)

The offset register holds the offset calibration coefficient for the ADC. The power-on reset value of the offset register is 0x800000. The AD7192 has four offset registers so each channel has a dedicated offset register. Each of these registers is a 24-bit read/write register. This register is used in conjunction with its associated full-scale register to form a register pair. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user. The AD7192 must be placed in power-down mode or idle mode when writing to the offset register.

FULL-SCALE REGISTER

(RS2, RS1, RS0 = 1, 1, 1; Power-On/Reset = 0x5XXXX0)

The full-scale register is a 24-bit register that holds the full-scale calibration coefficient for the ADC. The AD7192 has 4 full-scale registers so each channel has a dedicated full-scale register. The full-scale registers are read/write registers. However, when writing to the full-scale registers, the ADC must be placed in power-down mode or idle mode. These registers are configured on power-on with factory-calibrated full-scale calibration coefficients, the calibration being performed at gain = 1. Therefore, every device will have different default coefficients. The default value will be automatically overwritten if an internal or system full-scale calibration is initiated by the user or the full-scale register is written to.