System Management IC with Programmable Quad Voltage Monitoring and Supervisory Functions

AD5100

FEATURES

- 2 device-enabling outputs with 6 programmable monitoring inputs (see Table 1)
- Two 30 V monitoring inputs with shutdown control of external devices
  - Programmable overvoltage, undervoltage, turn-on and turn-off thresholds, and shutdown timings
  - Shutdown warning with fault detection
  - Reset control of external devices
- 5 V and 7.96 V monitoring inputs with reset control of external devices
  - Programmable reset thresholds and hold time
- eMOST-compatible inputs
  - Diagnostic application using V_{2MON} and V_{4MON}
- Two supervisory functions
  - Watchdog reset controller with programmable timeout and selectable floating input
  - Manual reset control for external devices
- Digital interface and programmability
  - I²C-compatible interface
  - OTP[1] for permanent threshold and timing settings
  - OTP can be overwritten for dynamic adjustments
  - Power-up by edge triggered signal
  - Power-down over I²C bus
- Operating range
  - Supply voltage: 6.0 V to 30 V
  - Temperature range: −40°C to +125°C
- Shutdown current: 5 µA max
- Operating current: 2 mA max
- High voltage input antimigration shielding pinouts

APPLICATIONS

- Automotive systems
- Network equipment
- Computers, controllers, and embedded systems

[1] One-time programmable EPROM with unlimited adjustment before OTP execution.

GENERAL DESCRIPTION

The AD5100 is a programmable system management IC that combines four channels of voltage monitoring and watchdog supervision. The AD5100 can be used to shut down external supplies, reset processors, or disable any other system electronics when the system malfunctions. The AD5100 can also be used to protect systems from improper device power-up sequencing. The AD5100, a robust watchdog reset controller, can monitor two 30 V inputs with shutdown and reset controls, one 2.3 V to 5.0 V input, and one 1.6 V to 7.96 V input. Most monitoring input thresholds and timing settings can be programmed on-the-fly or permanently set with the OTP memory feature.

The AD5100 is versatile for system monitoring applications where critical microprocessor, DSP, and embedded systems operate under harsh conditions, such as automotive, industrial, or communications network environments.

The AD5100 is available in a compact 16-lead QSOP package and can operate in an extended automotive temperature range from −40°C to +125°C.

Table 1. AD5100 General Input and Output Information

Input	Monitoring Range[1]	Shutdown Control	Reset Control	Fault Detection
V_{1MON}	6 V to 28.29 V	Yes	Yes	Yes
V_{2MON}	3 V to 24.75 V	Yes	Yes	Yes
V_{3MON}	2.32 V to 4.97 V	No	Yes	Yes
V_{4MON}	1.67 V to 7.96 V	No	Yes	Yes
WDI	0 V to 5 V	Yes	Yes	No
$\overline{MR}$	0 V to 5 V	No	Yes	No

[1] With programmable threshold and programmable delay.

Rev. 0

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REVISION HISTORY

9/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

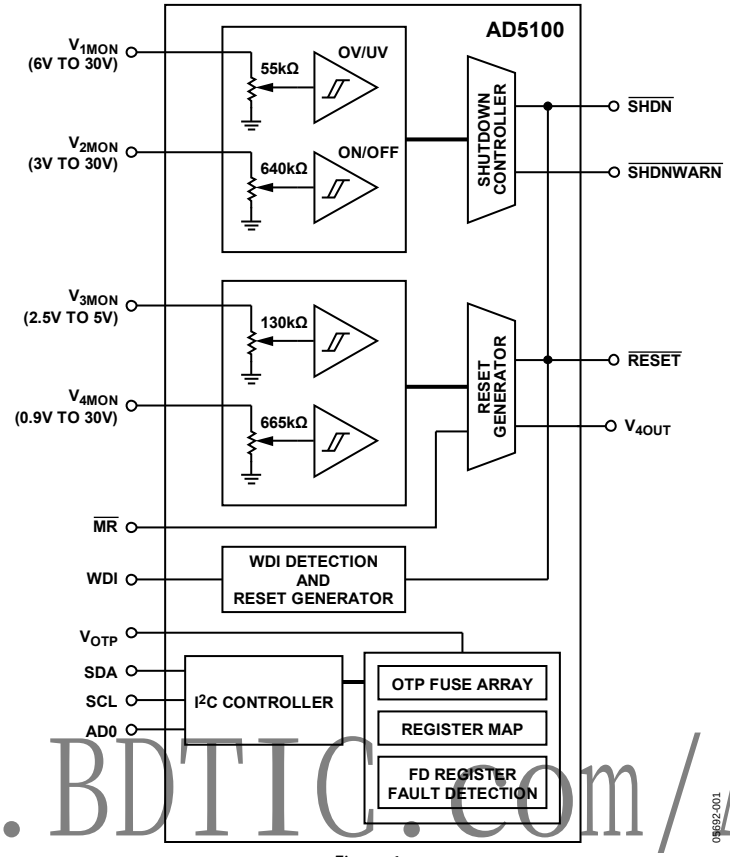


Figure 1.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

6 V ≤ V_{1MON} ≤ 30 V and 3 V ≤ V_{2MON} ≤ 30 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
HIGH VOLTAGE MONITORING INPUTS						
V_{1MON}						
Voltage Range	V_{1MON}		6		30	V
Input Resistance	R_{IN_V1MON}		36	55	70	kΩ
OV, UV Threshold Tolerance (See Figure 7 and Table 6)	ΔOV, ΔUV	T_A = 25°C	−1.6		+1.6	%
		T_A = −40°C to +85°C	−1.8		+1.8	%
		T_A = −40°C to +125°C	−2		+2	%
Hysteresis				1.5		%
Programmable Shutdown Hold Time Tolerance (See Figure 7 and Table 8)	Δt_{1SD_HOLD}	T_A = 25°C; does not apply to Code 0x7	−10		+10	%
Programmable Shutdown Delay Tolerance (See Figure 7 and Table 8)	Δt_{1SD_DELAY}	T_A = 25°C; does not apply to Code 0x7	−10		+10	%
		T_A = −40°C to +125°C; does not apply to Code 0x7	−17		+17	%
Fault Detection Delay	t_{FD_DELAY}			60		µs
Glitch Immune Time	t_{GLITCH}	Guaranteed by evaluation		45		µs
V_{2MON}						
Input Voltage	V_{2MON}	Minimum voltage on V_{2MON} to ensure AD5100 V_{REG} power-up	2.2			V
Voltage Range[2]	V_{2MON}		3		30	V
Input Resistance	R_{IN_V2MON}		500	640	760	kΩ
On, Off Threshold Tolerance[3] (See Figure 7 and Table 6)	ΔOn, ΔOff	T_A = 25°C	−2		+2	%
		T_A = −40°C to +85°C	−2.4		+2.4	%
		T_A = −40°C to +125°C	−2.5		+2.5	%
Hysteresis				1.5		%
Turn-On Programmable $\overline{SHDN}$ Hold Time Tolerance (See Figure 7 and Table 8)	Δt_{2SD_HOLD}	T_A = 25°C; does not apply to Code 0x7	−10		+10	%
Turn-Off Programmable $\overline{SHDN}$ Delay Time Tolerance (See Figure 7 and Table 8)	Δt_{2SD_DELAY}	T_A = 25°C; does not apply to Code 0x07	−10		+10	%
		T_A = −40°C to +125°C; does not apply to Code 0x7	−17		+17	%
Fault Detection Delay	t_{FD_DELAY}	V_{2MON_OFF} only		60		µs
Glitch Immune Time	t_{GLITCH}			45		µs
$\overline{SHDN}$						
$\overline{SHDN}$ Output High	V_{OH}	V_{RAIL} = V_{REG}, I_{SOURCE} = 40 µA	2.4			V
		V_{RAIL} = V_{1MON}, I_{SOURCE} = 600 µA	V_{1MON} − 0.5			V
$\overline{SHDN}$ Output Low	V_{OL}	I_{SINK} = 1.6 mA			0.4	V
		V_{1MON} = 12 V, I_{SINK} = 40 mA		1.5	3	V
$\overline{SHDN}$ Sink Current	I_{SINK}	V_{1MON} = 12 V, $\overline{SHDN}$ forced to 12 V		10	13.5	mA
$\overline{SHDNWARN}$ (Open-Drain Output)						
$\overline{SHDNWARN}$ Inactive Leakage Current	$I_{OH\_SHDNWARN}$			0.9		µA
$\overline{SHDNWARN}$ Active	$V_{OL\_SHDNWARN}$	I_{SINK} = 3 mA			0.4	V

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
LOW VOLTAGE MONITORING INPUTS						
V_{3MON}, V_{4MON}						
V_{3MON} Voltage Range	V_{3MON}		2.0		5.5	V
Input Resistance	R_{IN_V3MON}		110	130	155	kΩ
V_{3MON} Threshold Tolerance (See Figure 10 and Table 6)	ΔV_{3MON}	T_A = 25°C	−2.5		+2.5	%
		T_A = −40°C to +85°C	−2.75		+2.75	%
		T_A = −40°C to +125°C	−3		+3	%
V_{3MON} Hysteresis	$V_{3\_HYSTERESIS}$			1.2		%
V_{4MON} Voltage Range[4]	V_{4MON}		0.9		30	V
Input Resistance	R_{IN_V4MON}		580	665	775	kΩ
V_{4MON} Threshold Tolerance (See Figure 12 and Table 6)	ΔV_{4MON}	T_A = 25°C	−2.5		+2.5	%
		T_A = −40°C to +85°C	−2.75		+2.75	%
		T_A = −40°C to +125°C	−3		+3	%
V_{4MON} Hysteresis	$V_{4\_HYSTERESIS}$			5		%
$\overline{RESET}$						
$\overline{RESET}$ Hold Time Tolerance (See Figure 10, Figure 12, and Table 8)	Δt_{RS_HOLD}	T_A = 25°C; does not apply to Code 0x6 and Code 0x7	−10		+10	%
		T_A = −40°C to +125°C; does not apply to Code 0x6 and Code 0x7	−17		+17	%
V_{3MON}/V_{4MON}-to-$\overline{RESET}$ Delay	t_{RS_DELAY}			60		µs
$\overline{RESET}$ Output Voltage High	V_{OH}	$V_{3MON} \geq 4.38$ V, I_{SOURCE} = 120 µA	V_{3MON} − 1.5			V
		2.7 V < $V_{3MON} \leq 4.38$ V, I_{SOURCE} = 30 µA	0.8 × V_{3MON}			V
		2.3 V < $V_{3MON} \leq 2.7$ V, I_{SOURCE} = 20 µA	0.8 × V_{3MON}			V
		1.8 V ≤ $V_{3MON} \leq 2.3$ V, I_{SOURCE} = 8 µA	0.8 × V_{3MON}			V
$\overline{RESET}$ Output Voltage Low	V_{OL}	V_{3MON} > 4.38 V, I_{SINK} = 3.2 mA			0.4	V
		V_{3MON} < 4.38 V, I_{SINK} = 1.2 mA			0.3	V
$\overline{RESET}$ Output Short-Circuit Current[5]	I_{SOURCE}	$\overline{RESET}$ = 0, V_{3MON} = 5.5 V			825	µA
		$\overline{RESET}$ = 0, V_{3MON} = 3.6 V			400	µA
Glitch Immune Time	t_{GLITCH}			50		µs
V_{4OUT} Maximum Output	V_{4OUT_MAX}	Open drain			5.5	V
V_{4OUT} Propagation Delay	t_{V4OUT_DELAY}			70		µs
V_{4OUT} Maximum Frequency	f_{V4OUT}	Applies to $\overline{RESET}$ disabled only		10		kHz
WDI (WATCHDOG INPUT)						
WDI Programmable Timeout Tolerance (see Figure 13 and Table 8)	Δt_{WD}	T_A = 25°C	−10		+10	%
		T_A = −40°C to +125°C	−17		+17	%
WDI Pulse Width	t_{WDI}		50			ns
Watchdog Initiated $\overline{RESET}$ Pulse Width	t_{WDR}	When no WDI		t_{WD}/50		ms
Watchdog Initiated $\overline{SHDN}$	t_{WD_SHDN}	When no WDI activity > 4 t_{WD}		1		sec
WDI Input Voltage Low	V_{IL_WD}				0.3 × V_{3MON}	V
WDI Input Voltage High	V_{IH_WD}		0.7 × V_{3MON}			V
WDI Input Current		WDI = V_{3MON}			160	µA
		WDI = 0	−20			µA

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
$\overline{MR}$ (MANUAL RESET) INPUT						
$\overline{MR}$ Input Voltage Low	V_{IL_MR}				$0.3 \times V_{3MON}$	V
$\overline{MR}$ Input Voltage High	V_{IH_MR}		$0.7 \times V_{3MON}$			V
Input Current					1	µA
$\overline{MR}$ Pulse Width	t_{MR}		1			µs
$\overline{MR}$ Deglitching	t_{MR_GLITCH}			100		ns
$\overline{MR}$-to-$\overline{RESET}$ Delay	t_{MR_DELAY}			1		µs
$\overline{MR}$ Pull-Up Resistance (Internal to V_{3MON})			50	60	75	kΩ
$\overline{RESET}$ Hold Time Tolerance (see Figure 12 and Table 8)	Δt_{RS_HOLD}	T_A = 25°C; does not apply to Code 0x6 and Code 0x7	−10		+10	%
		T_A = −40°C to +125°C; does not apply to Code 0x06 and Code 0x7	−17		+17	%
SERIAL INTERFACES						
Input Logic High (SCL, SDA)[6]	V_{IH}	External $R_{PULL-UP}$ = 2.2 kΩ	2.0		5.5	V
Input Logic Low (SCL, SDA)	V_{IL}	External $R_{PULL-UP}$ = 2.2 kΩ	0		0.8	V
Output Logic High (SDA)	V_{OH}	V_{RAIL} = 2 V to 5.5 V	$0.7 \times V_{RAIL}$			V
Output Logic Low (SDA)	V_{OL}	I_{OL} = 3 mA	0		0.4	V
Input Current		V_{IN} = 0 V to 5.5 V			1	µA
Input Capacitance	C_I			5		pF
POWER SUPPLY						
Supply Voltage Range	V_{1MON}		6.0		30	V
Sleep Mode Supply Current	I_{SLEEP_V1MON}	V_{2MON} = 0 V			5	µA
Active Mode Supply Current	I_{POWER_V1MON}	V_{2MON} = 1.2 V			2	mA
		V_{2MON} edge triggered mode selected			2	mA
Device Power-On Threshold	$V_{2MON, IH}$		2.2			V
	$V_{2MON, IL}$				0.4	V
Device Power-Up V_{2MON}, Minimum Pulse Width	t_{V2MON_PW}		4			ms
Device Power-Down Delay	$T_{VREG\_OFF\_DELAY}$	V_{2MON} < 0.4 V (normal mode)		2		sec
		I^2C-initiated power-down		10		µs
OTP Supply Voltage[7]	V_{OTP}	For OTP only		5.5		V
OTP Supply Current[8]	I_{VOTP}	For OTP only		84		mA
OTP Settling Time[9]	t_{S_OTP}			12		ms

[1] Represent typical values at 25°C, V_{1MON} = 12 V, and V_{2MON} = 12 V.
[2] Initial V_{2MON} turn-on minimum remains as 2.2 V but the 3 V to 30 V specifications apply afterward.
[3] Does not apply if V_{2MON} is a digital signal.
[4] V_{4MON} threshold limits (see Table 6) are designed to primarily allow V_{4MON} to monitor low voltage inputs. The V_{4MON} input pin is capable of withstanding voltages up to 30 V. One application where this 30 V capability is useful is electronic media-oriented systems transport (eMOST) diagnostic circuits.
[5] The $\overline{RESET}$ short-circuit current is the maximum pull-up current when $\overline{RESET}$ is driven low by a microprocessor bidirectional reset pin.
[6] It is typical for the SCL and SDA to have resistors pulled up to V_{3MON}. However, care must be taken to ensure that the minimum V_{IH} is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.
[7] V_{OTP} can be furnished by an external 5.5 V power supply, rather than an on-board power supply, when performing factory programming. A 10 µF tantalum capacitor is required on V_{OTP} during operation regardless of whether the OTP fuses are programmed.
[8] The OTP supply source must be capable of supplying a minimum of 100 mA because some AD5100 parts require a current slightly greater than the typical value of 84 mA.
[9] The OTP settling time occurs only once if the OTP function is used.

TIMING SPECIFICATIONS

Table 3.

Parameter	Description	Min	Typ	Max	Unit
I^2C INTERFACE TIMING CHARACTERISTICS[1, 2]					
f_{SCL}	SCL clock frequency			400	kHz
t_1	t_{BUF}, bus free time between start and stop	1.3			µs
t_2	$t_{HD;STA}$, hold time after (repeated) start condition; after this period, the first clock is generated	0.6			µs
t_3	t_{LOW}, low period of SCL clock	1.3			µs
t_4	t_{HIGH}, high period of SCL clock	0.6		50	µs
t_5	$t_{SU;STA}$, setup time for start condition	0.6			µs
t_6	$t_{HD;DAT}$, data hold time			0.9	µs
t_7	$t_{SU;DAT}$, data setup time	0.1			µs
t_8	t_F, fall time of both SDA and SCL signals			0.3	µs
t_9	t_R, rise time of both SDA and SCL signals			0.3	µs
t_{10}	$t_{SU;STO}$, setup time for stop condition	0.6			µs

[1] Guaranteed by design and not subject to production test.
[2] See Figure 2.

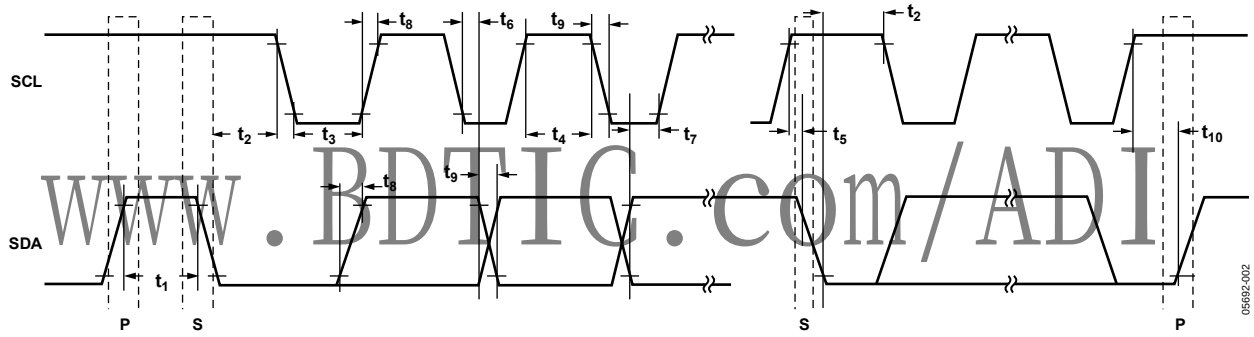


Figure 2. Digital Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{1MON} to GND	−0.3 V, +33 V
V_{2MON} to GND	−0.3 V, +33 V
V_{3MON} to GND	−0.3 V, +7 V
V_{4MON} to GND	−0.3 V, +33 V
V_{OTP} to GND	−0.3 V, +7 V
Digital Input Voltage to GND ($\overline{MR}$, WDI, SCL, SDA, AD0)	0 V, +7 V
Digital Output Voltage to GND ($\overline{RESET}$, V_{4OUT}, $\overline{SHDN}$WARN)	0 V, +7 V
Digital Output Voltage to GND ($\overline{SHDN}$)	0 V, +33 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
ESD Rating (HBM)	3.5 kV
Maximum Junction Temperature (T_{Jmax})	150°C
Power Dissipation[1]	$(T_{Jmax} - T_A{}^2)/\theta_{JA}$
Thermal Impedance[3]	
θ_{JA} Junction-to-Ambient	105.44°C/W
θ_{JC} Junction-to-Case	38.8°C/W
IR Reflow Soldering (RoHS-Compliant Package)	
Peak Temperature	260°C (+0°C)
Time at Peak Temperature	20 sec to 40 sec
Ramp-Up Rate	3°C/sec max
Ramp-Down Rate	−6°C/sec max
Time from 25°C to Peak Temperature	8 minutes max

[1] Values relate to the package being used on a 4-layer board.
[2] T_A = ambient temperature.
[3] Junction-to-case resistance is applicable to components featuring a preferential flow direction, for example, components mounted on a heat sink. Junction-to-ambient resistance is more useful for air-cooled PCB-mounted components.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

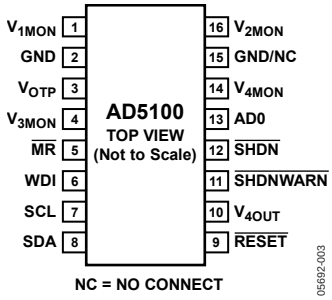


Figure 3. Pin Configuration

Table 5. AD5100 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{1MON}	High Voltage Monitoring Input. AD5100 internal supply is derived from V_{1MON}. There must be a 10 µF electrolytic capacitor between this pin and GND, placed as close as possible to the V_{1MON} pin.
2	GND	Ground.
3	V_{OTP}	One-Time Programmable Supply Voltage for EPROM. A 10 µF decoupling capacitor (low ESR) to GND is required when not fuse programming.
4	V_{3MON}	Low Voltage Monitoring Input.
5	$\overline{MR}$	Manual Reset Input. Active low.
6	WDI	Watchdog Input.
7	SCL	I^2C Serial Input Register Clock. Open-drain input. If it is driven directly from a logic driver without the pull-up resistor, ensure that the V_{IH} minimum is 3.3 V.
8	SDA	I^2C Serial Data Input/Output. Open-drain input/output. If it is driven directly from a logic driver without the pull-up resistor, ensure that the V_{IH} minimum is 3.3 V.
9	$\overline{RESET}$	Reset. Push-pull output with rail voltage of V_{3MON}.
10	V_{4OUT}	Open-Drain Output. Triggered by V_{4MON}.
11	$\overline{SHDNWARN}$	Shutdown Warning. Active low, open-drain output.
12	$\overline{SHDN}$	Shutdown Output. Push-pull output with selectable rail voltage of V_{1MON} or V_{REG}, the AD5100 internal power (30 V maximum).
13	AD0	I^2C Slave Address Configuration. If tied high, this pin can only be tied to 3.3 V maximum.
14	V_{4MON}	Low Voltage Monitoring Input. Capable of withstanding 30 V.
15	GND/NC	Ground/No Connect. Can be grounded or left floating but do not connect to any other potentials.
16	V_{2MON}	High Voltage Monitoring Input. It is also the internal supply voltage enabling input.

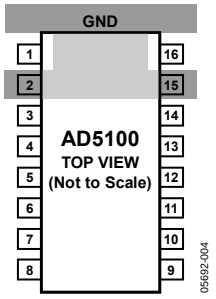


Figure 4. Recommended PCB Layout for Shielded High Voltage Inputs

ONE-TIME PROGRAMMABLE (OTP) OPTIONS

All values are typical ratings; see Table 2 for tolerances.

Table 6. Available Programmable Thresholds at T_A = 25°C

V_{1MON} OV Threshold	V_{1MON} UV Threshold	V_{2MON} On Threshold	V_{2MON} Off Threshold	V_{3MON} Threshold	V_{4MON} Threshold
7.92 V	6.00 V	3.00 V	3.00 V	2.32 V	1.67 V
9.00 V	6.49 V	3.5 V	3.5 V	2.64 V	2.31 V
9.90 V	6.95 V	4.00 V	4.00 V	2.93 V[1]	3.05 V
11.00 V	7.47 V	4.77 V	4.77 V	3.10 V	4.62 V
12.00 V	7.92 V	6.00 V	6.00 V	4.36 V	6.51 V
13.20 V	8.43 V[1]	6.49 V	6.49 V	4.65 V	7.16 V
14.14 V	9.00 V	6.95 V	6.95 V[1]	4.75 V	7.54 V[1]
15.23 V	9.43 V	7.47 V[1]	7.47 V	4.97 V	7.96 V
15.84 V	9.90 V	7.92 V	7.92 V	Reserved	Reserved
17.22 V	10.42 V	8.43 V	8.43 V	Reserved	Reserved
18.00 V[1]	11.00 V	9.00 V	9.00 V	Reserved	Reserved
18.86 V	11.65 V	9.43 V	9.43 V	Reserved	Reserved
19.80 V	12.00 V	9.90 V	9.90 V	Reserved	Reserved
22.00 V	12.38 V	15.23 V	15.23 V	Reserved	Reserved
24.75 V	13.20 V	19.80 V	19.80 V	Reserved	Reserved
28.29 V	13.66 V	24.75 V	Rising edge triggered wake-up mode	Reserved	Reserved

[1] Default. V_{1MON_OV} must be > V_{1MON_UV}. V_{2MON_OFF} is ignored if > V_{2MON_ON} but V_{2MON_OFF} cannot be = V_{2MON_ON}.

Table 7. Look-Up Table of Programming Code vs. Typical Thresholds Shown in Table 6

Code	V_{1MON} OV Threshold	V_{1MON} UV Threshold	V_{2MON} On Threshold	V_{2MON} Off Threshold	V_{3MON} Threshold	V_{4MON} Threshold
0000	18.00 V[1]	8.43 V[1]	7.47 V[1]	6.95 V[1]	2.93 V[1]	7.54 V[1]
0001	18.86 V	7.92 V	6.95 V	7.47 V	4.65 V	1.67 V
0010	15.84 V	9.43 V	6.49 V	6.00 V	4.75 V	2.31 V
0011	17.22 V	9.00 V	6.00 V	6.49 V	4.97 V	3.05 V
0100	24.75 V	6.49 V	4.77 V	4.00 V	2.32 V	4.62 V
0101	28.29 V	6.00 V	4.00 V	4.77 V	2.64 V	6.51 V
0110	19.80 V	7.47 V	3.50 V	3.00 V	4.36 V	7.16 V
0111	22.00 V	6.95 V	3.00 V	3.50 V	3.10 V	7.96 V
1000	9.90 V	12.38 V	24.75 V	19.80 V	Reserved	Reserved
1001	11.00 V	12.00 V	19.80 V	Rising edge triggered wake-up mode	Reserved	Reserved
1010	7.92 V	13.66 V	15.23 V	9.90 V	Reserved	Reserved
1011	9.00 V	13.20 V	9.90 V	15.23 V	Reserved	Reserved
1100	14.14 V	10.42 V	9.43 V	9.00 V	Reserved	Reserved
1101	15.23 V	9.90 V	9.00 V	9.43 V	Reserved	Reserved
1110	12.00 V	11.65 V	8.43 V	7.92 V	Reserved	Reserved
1111	13.20 V	11.00 V	7.92 V	8.43 V	Reserved	Reserved

[1] Default.

Table 8. Available Programmable Hold Time and Delay

t_{1SD_HOLD}	t_{1SD_DELAY}	t_{2SD_HOLD}	t_{2SD_DELAY}	t_{RS_HOLD}	t_{WD}
0.07 ms	0.07 ms	0.07 ms	0.07 ms	0.1 ms	100 ms
20 ms	50 ms	10 ms[1]	50 ms	1 ms	250 ms
40 ms	100 ms	20 ms	100 ms[1]	15 ms	500 ms
60 ms	200 ms	30 ms	200 ms	30 ms	750 ms
80 ms	400 ms	40 ms	400 ms	50 ms	1000 ms
100 ms	800 ms	50 ms	800 ms	100 ms	1250 ms
150 ms	1000 ms	100 ms	1000 ms	150 ms	1500 ms[1]
200 ms[1]	1200 ms[1]	200 ms	1200 ms	200 ms[1]	2000 ms

[1] Default.

Table 9. Look-Up Table of Programming Code vs. Typical Timings Shown in Table 8

Code	t_{1SD_HOLD}	t_{1SD_DELAY}	t_{2SD_HOLD}	t_{2SD_DELAY}	t_{RS_HOLD}	t_{WD}
000	200 ms[1]	1200 ms[1]	10 ms[1]	100 ms[1]	200 ms[1]	1500 ms[1]
001	150 ms	1000 ms	20 ms	50 ms	150 ms	2000 ms
010	100 ms	800 ms	30 ms	200 ms	100 ms	1250 ms
011	80 ms	400 ms	40 ms	400 ms	50 ms	1000 ms
100	60 ms	200 ms	50 ms	800 ms	30 ms	750 ms
101	40 ms	100 ms	100 ms	1000 ms	15 ms	500 ms
110	20 ms	50 ms	200 ms	1200 ms	1 ms	250 ms
111	0.07 ms	0.07 ms	0.07 ms	0.07 ms	0.1 ms	100 ms

[1] Default.

THEORY OF OPERATION

The AD5100 is a programmable system management IC that has four channels of monitoring inputs. Three inputs have high voltage (30 V) capability. For example, if the AD5100 is used in an automotive application, V_{1MON} (Monitoring Input 1) can be connected to the battery and the V_{2MON} can be connected to the ignition switch, a rising edge trigger wake-up signal, or the media-oriented systems transport (MOST) wake-up signal (V_{4MON} is connected to V_{2MON} for MOST applications). Two other inputs, V_{3MON} and V_{4MON}, are designed for low voltage monitoring, with programmable thresholds from 2.93 V to 7.96 V. The two high voltage monitoring inputs control the shutdown signal, $\overline{SHDN}$ and reset signal, $\overline{RESET}$, while the two low voltage monitoring inputs control the reset signal, $\overline{RESET}$. $\overline{SHDN}$ and $\overline{RESET}$ are both disabling signals for external devices. The differences between these two outputs are in output level and driving capabilities, as described in the Outputs section. The WDI (watchdog) and $\overline{MR}$ (manual reset) inputs also control the $\overline{RESET}$ output, for use with an external digital processor. Figure 5 shows the general flow chart and Table 10 summarizes the AD5100 functions and features.

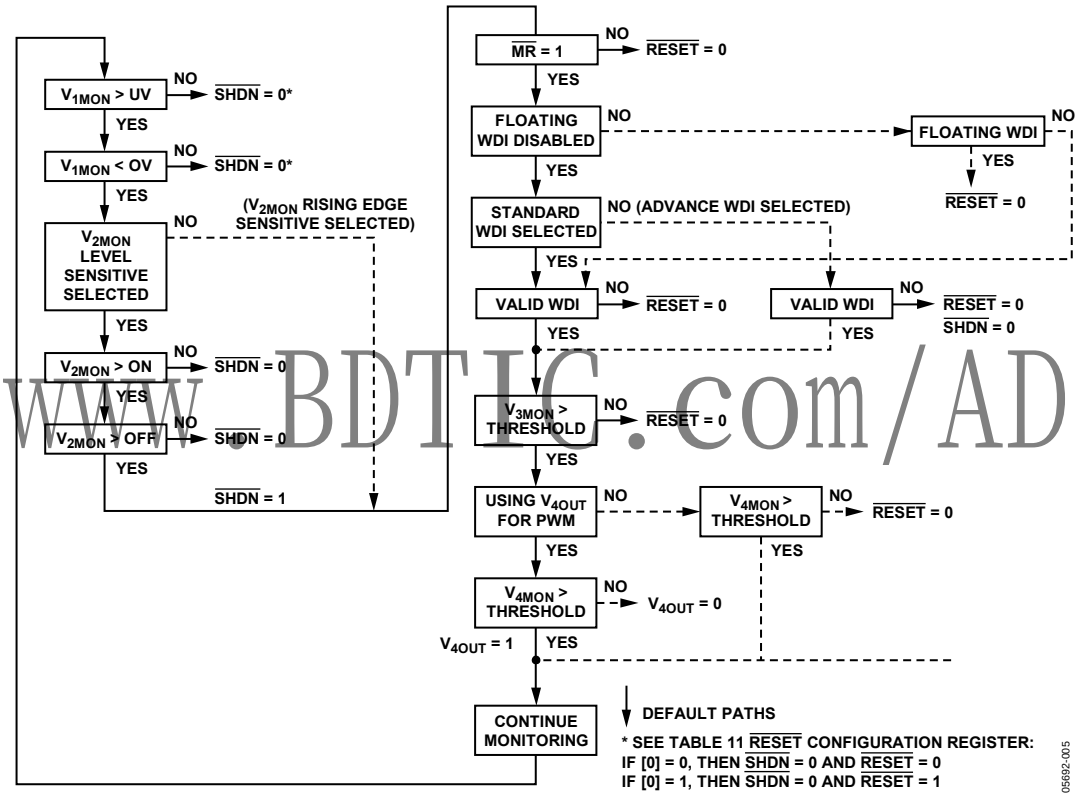


Figure 5. General Flow Chart

Table 10. AD5100 Functions and Features

Input	Monitoring Range	Shutdown Control	Reset Control	Fault Detection	Functions and Features	If Not Used
V_{1MON}	6 V to 28.29 V	Yes	Yes	Yes	Overvoltage/undervoltage thresholds	Does not apply
V_{2MON}	3 V to 24.75 V	Yes	Yes	Yes	On/off voltage thresholds; pseudo rising edge triggered, wake-up selectable; MOST wake-up signal (V_{2MON} connected to V_{4MON})	Connect to V_{1MON}, minimum input 6 V
V_{3MON}	2.32 V to 4.97 V	No	Yes	Yes		Connect to V_{OTP} and set threshold to minimum
V_{4MON}	1.67 V to 7.96 V	No	Yes	Yes	Additional output	Connect to GND
WDI	0 V to 5 V	Yes	Yes	No	Standard, advance, or floating; watchdog selectable	Leave floating
$\overline{MR}$	0 V to 5 V	Yes	Yes	No	Highest priority on $\overline{RESET}$ over other inputs	Leave floating

MONITORING INPUTS

V_{1MON}

V_{1MON} is a high voltage monitoring input that controls the $\overline{SHDN}$ and $\overline{RESET}$ functions of the external devices. In addition, it provides a shutdown warning to the system. V_{1MON} monitors inputs from 6 V to 30 V.

The V_{1MON} pin is monitored by two comparators, one for overvoltage and one for undervoltage detection. Both are designed with 1.5% hysteresis.

When the V_{1MON} input goes above the programmed overvoltage (OV) threshold, the comparator becomes active immediately, indicating that an OV condition has occurred. Due to hysteresis, the V_{1MON} input must be brought below the programmed OV threshold by 1.5% before the comparator becomes inactive, indicating that the OV condition has gone away (see Figure 6).

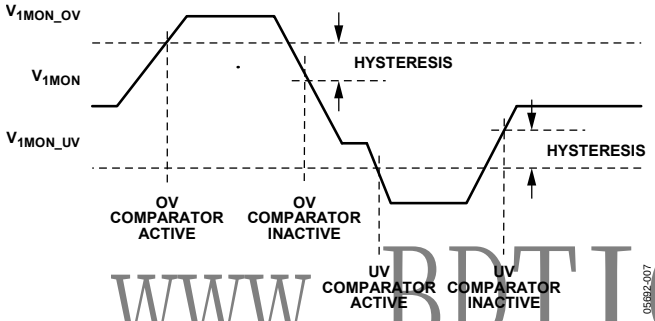


Figure 6. V_{1MON} Hysteresis

When the V_{1MON} input drops below the programmed undervoltage (UV) threshold, the comparator becomes active immediately, indicating that a UV condition has occurred. Similarly, due to hysteresis, the V_{1MON} input must be brought above the programmed UV threshold by 1.5% before the comparator becomes inactive, indicating that the UV condition has gone away.

Both V_{1MON} comparators are used (in conjunction with hold and delay timers) to control the $\overline{SHDN}$ and $\overline{RESET}$ pins.

V_{1MON} has a 16-level programmable OV threshold (Register 0x01) and UV threshold (Register 0x02) with an 8-step 0.07 ms to 200 ms shutdown hold time (t_{1SD_HOLD}) and 0.07 ms to 1200 ms shutdown delay (t_{1SD_DELAY}). The shutdown hold time means that the $\overline{SHDN}$ signal is held low for t_{1SD_HOLD} after V_{1MON} returns within its UV and OV thresholds. The shutdown delay means that the $\overline{SHDN}$ signal activation is delayed until the programmed t_{1SD_DELAY} has elapsed. $\overline{SHDN}$ activates once the voltage on V_{1MON} is outside the OV or UV threshold for a time longer than t_{GLITCH}. $\overline{RESET}$ follows $\overline{SHDN}$ delay and hold timings when triggered by V_{IMON}.

The OV threshold chosen must be greater than the UV threshold. When the shutdown is triggered, either because the input has reached the OV or UV threshold, such fault conditions are temporarily recorded in the fault detection register.

The $\overline{SHDNWARN}$ output transitions low for signaling before the shutdown output, $\overline{SHDN}$, activates. The timing of the $\overline{SHDN}$ output is dependent on how long the shutdown-programmed delay (t_{1SD_DELAY}) is set relative to the $\overline{SHDNWARN}$ propagation delay (t_{FD_DELAY}). This feature attempts to allow the system to finish any critical housekeeping tasks before shutting down the external device.

The V_{1MON}, shutdown, and shutdown warning timing diagrams are shown in Figure 7.

The ranges of OV and UV thresholds are shown in Table 6, and the programming codes for the selected thresholds are found in Table 7. The defaulted OV threshold is 18.00 V and, for UV threshold, it is 8.43 V. Similarly, the ranges of shutdown hold and delay times are shown in Table 8, and the programming codes for the selected timings are shown in Table 9. The default shutdown hold time is 200 ms; for shutdown delay time, it is 1200 ms.

V_{1MON} exhibits typical input resistance of 55 kΩ that users should take into account for loading effect.

The voltage at V_{1MON} provides the power for the AD5100, but a valid signal on V_{2MON} must be present before the internal power rail, V_{REG}, starts operation. Details are explained in the Power Requirements section.

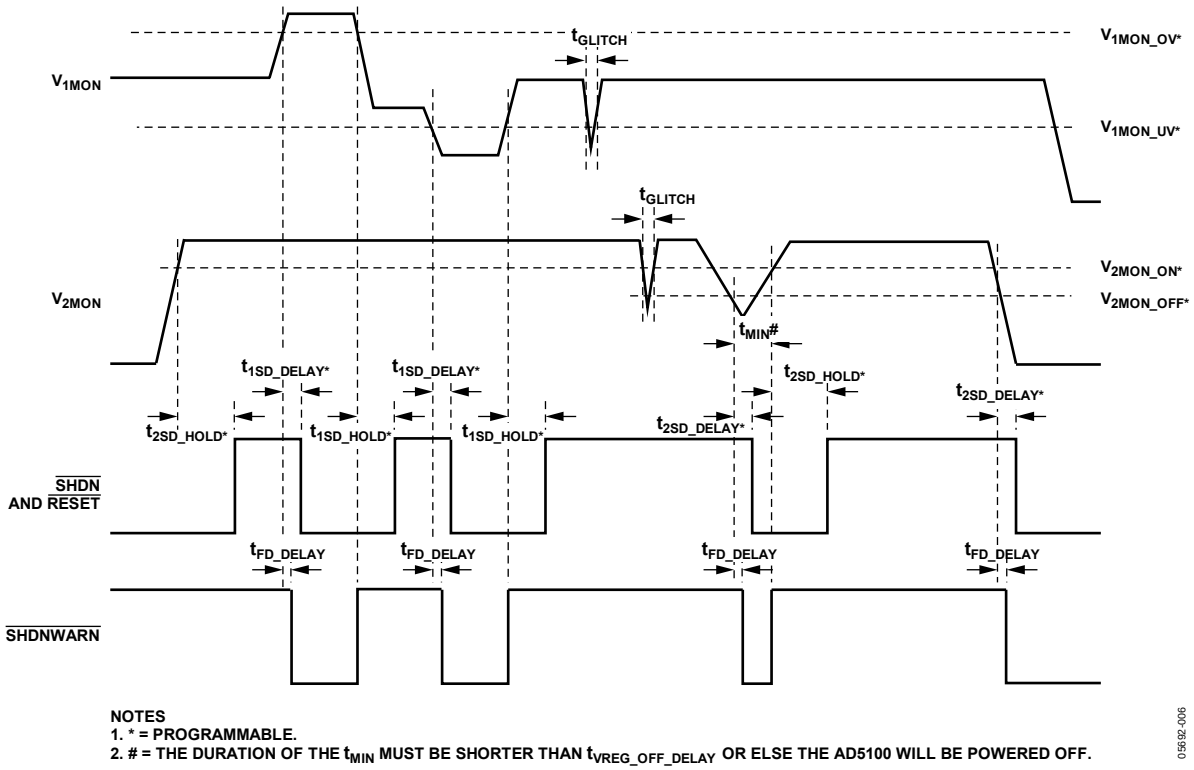


Figure 7. V_{1MON} and V_{2MON} Shutdown Timing Diagrams in Level-Sensitive Mode (Note that $\overline{RESET}$ Follows $\overline{SHDN}$)

V_{2MON}

V_{2MON} is a high voltage monitoring input that controls the $\overline{SHDN}$ and $\overline{RESET}$ functions of the external devices. V_{2MON} monitors inputs from 3 V to 30 V. It has a 16-level programmable turn-on and turn-off (on, off) hysteresis thresholds (Register 0x03 and Register 0x04), with an 8-step 0.07 ms to 200 ms shutdown hold time (t_{2SD_HOLD}) and 0.07 ms to 1200 ms shutdown delay (t_{2SD_DELAY}).

The V_{2MON} pin is monitored by two comparators, one for turn-on and one for turn-off detection, in the level-sensitive power-up mode. Both are designed with 1.5% hysteresis. Only the turn-on monitoring comparator is used if the rising edge triggered wake-up mode is selected.

When the V_{2MON} input goes above the programmed V_{2MON} on threshold, the comparator becomes active immediately, indicating that an on condition has occurred. Due to hysteresis, the V_{2MON} input must be brought below the programmed threshold by 1.5% before the comparator becomes inactive, indicating that the on condition has gone away (see Figure 8).

When the V_{2MON} input drops below the programmed threshold, the comparator becomes active immediately, indicating that a V_{2MON} off condition has occurred. Similarly, due to hysteresis, the V_{2MON} input must be brought above the programmed threshold by 1.5% before the comparator becomes inactive, indicating that the off condition has gone away.

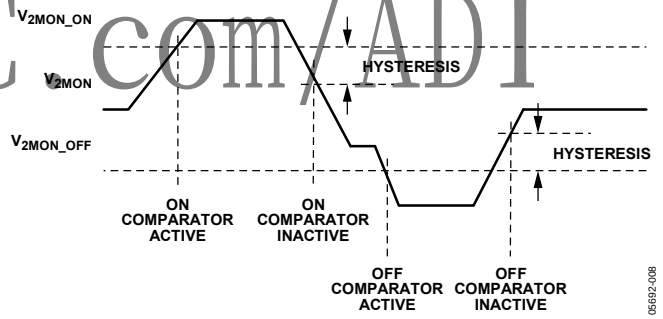


Figure 8. V_{2MON} Hysteresis

By default, V_{2MON} is level sensitive and the on and off thresholds are both monitored. The on threshold chosen must be greater than the off threshold.

When the $\overline{SHDN}$ output is activated by the input reaching the V_{2MON_OFF} threshold, such fault condition is temporarily recorded in the fault detection register. The $\overline{SHDNWARN}$ output transitions low for signaling before the shutdown output, $\overline{SHDN}$, activates. The timing of the $\overline{SHDN}$ output is dependent on how long the shutdown programmed delay (t_{2SD_DELAY}) is set relative to the $\overline{SHDNWARN}$ propagation delay (t_{FD_DELAY}). This feature allows the system to finish any critical housekeeping tasks before shutting down the external device. $\overline{SHDN}$ activates once the voltage on V_{2MON} is outside the threshold for a time longer than t_{GLITCH}. $\overline{RESET}$ follows $\overline{SHDN}$ delay and hold timings when triggered by V_{2MON}.

The V_{2MON}, shutdown, and shutdown warning timing diagrams are shown in Figure 7.

The ranges of on and off thresholds are shown in Table 6 and the programming codes for the selected-thresholds are found in Table 7. The default on threshold is 7.47 V and off threshold is 6.95 V. Similarly, the ranges of shutdown hold and delay times are shown in Table 8, and the programming codes of the selected timings are found in Table 9. The default shutdown hold time is 10 ms and the delay time is 100 ms.

V_{2MON_OFF} is ignored if V_{2MON_OFF} is greater than V_{2MON_ON} but V_{2MON_OFF} cannot equal V_{2MON_ON}.

If V_{2MON} is selected with rising edge triggered wake-up mode, only the on threshold is monitored and the off threshold is ignored. V_{2MON} is put into rising edge triggered mode by setting V_{2MON} off threshold, Register 0x04[3:0] to 1001

The voltage at V_{1MON} provides the power for the AD5100, but a valid signal on V_{2MON} must be present before the internal V_{REG} starts operating. Details are explained in the Power Requirements section.

V_{2MON} exhibits typical input resistance of 640 kΩ that users should take into account for loading effect.

V_{3MON}

V_{3MON} is a low voltage monitoring input that controls the $\overline{RESET}$ function of an external device.

The V_{3MON} pin is monitored by a comparator to detect an undervoltage condition. It is designed with 1.5% hysteresis. When the V_{3MON} input drops below the programmed UV threshold, the comparator becomes active immediately, indicating that a UV condition has occurred. Due to hysteresis, the V_{3MON} input must be brought above the programmed UV threshold by 1.5% before the comparator becomes inactive, indicating that the UV condition has gone away (see Figure 9).

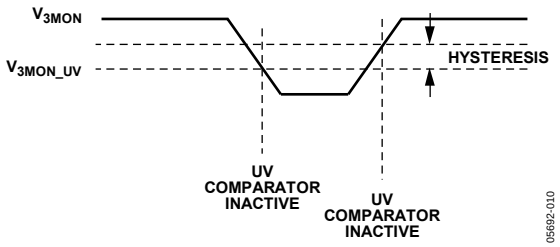


Figure 9. V_{3MON} Hysteresis

The V_{3MON} comparator is used (in conjunction with a hold timer) to control the $\overline{RESET}$ pin.

V_{3MON} monitors inputs from 2.0 V to 5.5 V. It has an 8-step programmable reset threshold (Register 0x05) with an 8-step 0.1 ms to 200 ms reset hold time (t_{RS_HOLD}). The reset hold time means that the $\overline{RESET}$ output remains activate when V_{3MON} goes above its UV threshold, until t_{RS_HOLD} has elapsed. This allows the reset of an external device to be held until the programmed time is reached.

The V_{3MON} and $\overline{RESET}$ timing diagrams are shown in Figure 10. The range of thresholds is shown in Table 6 and the programming code for the selected threshold is found in Table 7. The default monitoring threshold is 2.93 V. The range of reset hold times is shown in Table 8 and the programming code of the selected timing is found in Table 9. The default $\overline{RESET}$ hold time is 200 ms.

V_{3MON} exhibits typical input resistance of 130 kΩ that users should take into account for loading effect.

The $\overline{MR}$ input has an internal resistor pull-up toV_{3MON}. The $\overline{RESET}$ output is push-pull, between V_{3MON} and GND.

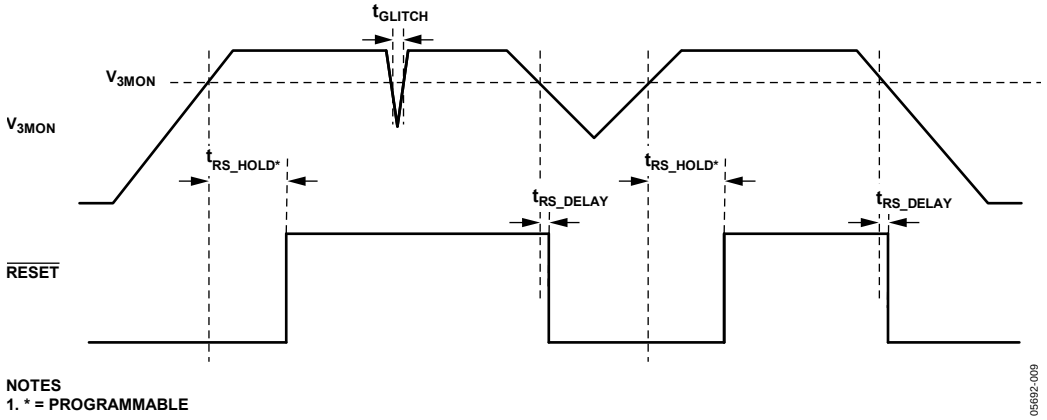


Figure 10. V_{3MON}, $\overline{RESET}$ Timing Diagrams

V_{4MON}

V_{4MON} is a low voltage monitoring input that controls the $\overline{RESET}$ function of an external device or provides a comparator output, V_{4OUT}. The V_{4MON} pin is monitored by a comparator to detect an undervoltage condition. It is designed with 5% hysteresis.

When the V_{4MON} input drops below the programmed UV threshold, the comparator becomes active immediately, indicating that a UV condition has occurred. Due to hysteresis, the V_{4MON} input must be brought above the programmed UV threshold by 5% before the comparator becomes inactive, indicating that the UV condition has gone away (see Figure 11).

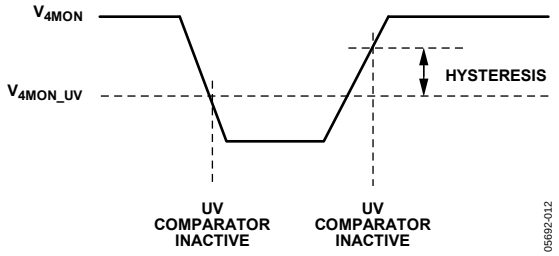


Figure 11. V_{4MON} Hysteresis

The V_{4MON} comparator is used to control the V_{4OUT} pin and (in conjunction with a hold timer) to control the $\overline{RESET}$ pin. To configure V_{4MON} to control the $\overline{RESET}$ pin, set Register 0x0D[3] to 0. Setting this bit to 1 prevents V_{4MON} from causing $\overline{RESET}$ to activate.

V_{4MON} input voltage range is up to 30 V. It has an 8-step programmable reset threshold (Register 0x06) from 1.67 V to 7.96 V, with an 8-step 0.1 ms to 200 ms reset hold time (t_{RS_HOLD}).

The V_{4MON}, $\overline{RESET}$, and V_{4OUT} timing diagrams are shown in Figure 12. The range of thresholds is shown in Table 6, and the programming code for the selected threshold is found in Table 8. The default monitoring threshold is 7.54 V. Similarly, the range of reset hold time is shown in Table 8, and the programming code of the selected timing is found in Table 9.

V_{4MON} exhibits typical input resistance of 665 kΩ that users should take into account for loading effect.

WATCHDOG INPUT

The watchdog input (WDI) circuit attempts to reset the system to a known good state if a software or hardware glitch renders the system processor inactive for a duration that is longer than the timeout period. The timeout period, t_{WD}, is programmable in eight steps from 100 ms to 2000 ms. The watchdog circuit is independent of any CPU clock that the watchdog is monitoring.

The range of watchdog timeout is shown in Table 8, and the programming code of the selected timeout is found in Table 9. The default timeout is 1500 ms.

The watchdog is disabled during power-up. WDI starts monitoring once $\overline{RESET}$ is high. The AD5100 provides a standard or advanced watchdog monitoring function. Register 0x0F[3] sets the watchdog function to either standard or advanced mode.

- Register 0x0F[3] = 0: standard watchdog mode
- Register 0x0F[3[= 1: advanced watchdog mode

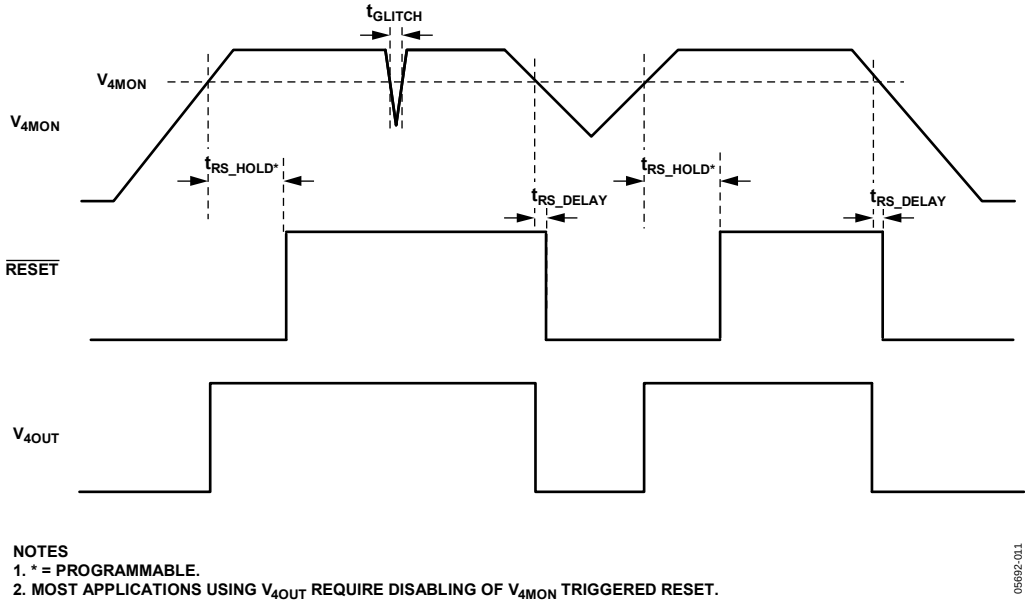


Figure 12. V_{4MON}, $\overline{RESET}$, and V_{4OUT} Timing Diagrams

Standard Watchdog Mode

In the default standard watchdog mode, if WDI remains either high or low for longer than the timeout period, t_{WD}, a $\overline{\text{RESET}}$ pulse is generated in an attempt to allow the system processor to re-establish the WDI signal. The $\overline{\text{RESET}}$ pulses continue indefinitely until a valid watchdog signal, a rising or falling edge signal at the WDI, is received. The internal watchdog timer clears whenever a reset is asserted. The standard WDI and $\overline{\text{RESET}}$ timing diagrams are shown in Figure 13.

Advanced Watchdog Mode

The AD5100 can be programmed into an advanced watchdog mode. In this mode, if WDI remains either high or low for longer than the timeout period, t_{WD}, a $\overline{\text{RESET}}$ pulse is generated, as per standard mode. However, if the WDI input remains inactive after three such $\overline{\text{RESET}}$ pulses, concurrent with the fourth $\overline{\text{RESET}}$ pulse, $\overline{\text{SHDN}}$ is also asserted. $\overline{\text{SHDN}}$ is released after 1 second. These actions repeat indefinitely (unless action is taken by the user), if the processor is not responding. The advanced WDI and $\overline{\text{RESET}}$ timing diagrams are shown in Figure 14.

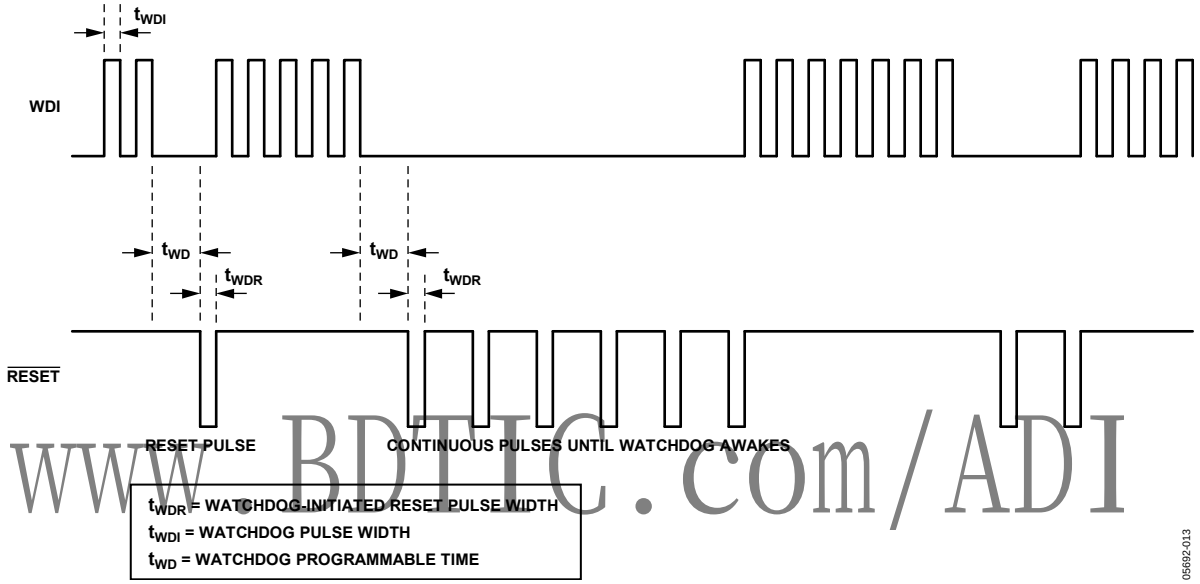


Figure 13. Standard Watchdog—Pulsing Reset Until Watchdog Awakes

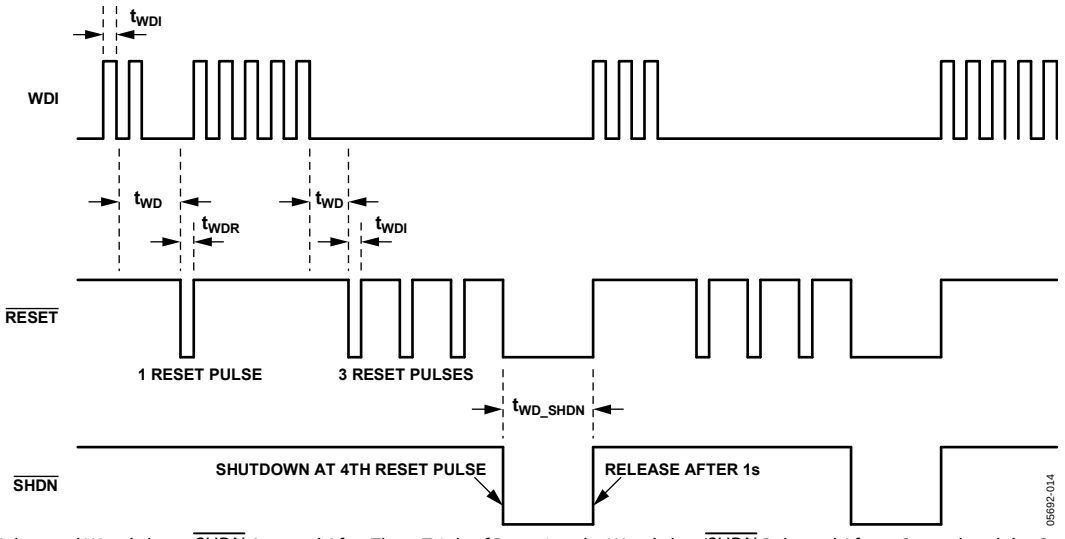


Figure 14. Advanced Watchdog—$\overline{\text{SHDN}}$ Asserted After Three Trials of Resetting the Watchdog ($\overline{\text{SHDN}}$ Released After 1 Second and the Cycle Repeats)

Floating WDI Input

If the WDI pin is floating, the watchdog function is disabled by default. However, floating watchdog can be enabled in the $\overline{\text{RESET}}$ configuration register such that a broken WDI connection or any unusual condition that makes WDI float triggers the reset.

- Register 0x0D[3] = 0: floating WDI input activates $\overline{\text{RESET}}$
- Register 0x0D[3] = 1: floating WDI input does not activate $\overline{\text{RESET}}$

Enabling or disabling the floating WDI feature can be changed dynamically, provided that the OTP fuse of the $\overline{\text{RESET}}$ configuration register is not blown or that the OTP overridden function is selected.

MANUAL RESET INPUT

Manual reset ($\overline{\text{MR}}$) is an active low input to the AD5100 and has an internal pull-up resistor to V_{3MON}. If the input signal on the $\overline{\text{MR}}$ pin goes low, $\overline{\text{RESET}}$ is activated. $\overline{\text{MR}}$ can be driven from a CMOS logic signal.

The $\overline{\text{MR}}$ and $\overline{\text{RESET}}$ timing diagrams are shown in Figure 15. Note that $\overline{\text{RESET}}$ is activated after t_{MR_DELAY} and is held for t_{RS_HOLD} after the $\overline{\text{MR}}$ signal has gone high again.

$\overline{\text{MR}}$ has the highest priority in triggering the $\overline{\text{RESET}}$ over any other monitoring inputs.

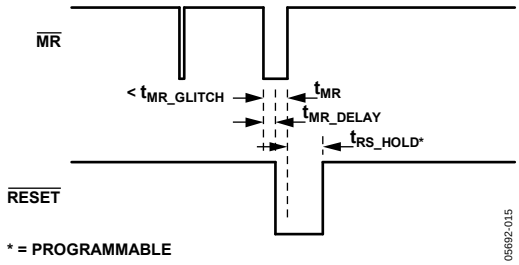


Figure 15. Manual Reset ($\overline{\text{MR}}$) Timing Diagram

OUTPUTS

SHUTDOWN OUTPUT, $\overline{\text{SHDN}}$

The shutdown output, $\overline{\text{SHDN}}$, is triggered by V_{1MON} or V_{2MON} over- or underthreshold values, or as the result of a failed watchdog input. $\overline{\text{SHDN}}$ can also be asserted low at any time by writing to certain registers on the AD5100.

The shutdown generator asserts a logic low $\overline{\text{SHDN}}$ signal based on the following conditions:

- During power-up
- When V_{1MON} goes over or under the threshold (see Figure 7)
- When V_{2MON} is below the turn-on threshold during the rising edge or the turn-off threshold during the falling edge in level-sensitive mode (see Figure 7)
- When the external monitoring processor cannot issue the necessary WDI signal and advanced WDI mode is selected (see Figure 10 and Figure 9)
- I²C® programmed shutdown

To activate $\overline{\text{SHDN}}$ by writing to the part, the user must first enable this feature by writing to Register 0x18[4].

- Register 0x18[4] = 0: enable software control of $\overline{\text{SHDN}}$
- Register 0x18[4] = 1: disable software control of $\overline{\text{SHDN}}$

Once the feature is enabled, control of $\overline{\text{SHDN}}$ is achieved by writing to Register 0x16[2].

- Register 0x16[2] = 0: $\overline{\text{SHDN}}$ output not controlled by software
- Register 0x16[2] = 1: $\overline{\text{SHDN}}$ output is pulled low

The $\overline{\text{SHDN}}$ signal is released after the programmable hold time, t_{SD_HOLD}. The $\overline{\text{SHDN}}$ output is push-pull configured with an I²C-selectable rail voltage of either V_{1MON} in default or internal V_{REG}. Register 0x0E controls the voltage rail for $\overline{\text{SHDN}}$.

- Register 0x0E[3] = 0: $\overline{\text{SHDN}}$ uses V_{1MON} rail
- Register 0x0E[3] =1: $\overline{\text{SHDN}}$ uses V_{REG} rail

Figure 16 shows the $\overline{\text{SHDN}}$ output configuration. Pull-down Resistor R1 ensures that $\overline{\text{SHDN}}$ is pulled to ground when the AD5100 is not powered. When AD5100 is powered, M2a and M2b are both on. M2a has relatively lower impedance than M2b and R1 so the $\overline{\text{SHDN}}$ remains low at shutdown. When the AD5100 settles, SW1 is turned on. M1 is stronger than M2a so $\overline{\text{SHDN}}$ is pulled to the rail, which takes AD5100 out of the shutdown mode.

In some applications, the AD5100 may monitor and control power regulators where the input and enable pins are next to each other in a fine pitch. This may pose reliability concerns under some abnormal conditions. To prevent errors from happening, the AD5100 shutdown output features smart-load detection to ensure that the shutdown responds. For example, if the car battery has not started for a long time, a resistive dendrite may have formed across the $\overline{\text{SHDN}}$ pin and the battery terminal (V_{1MON}). The dendrite is blown immediately because M2a is designed with adequate current sinking capability and remains in the on position to offer such protection. In another situation, if the $\overline{\text{SHDN}}$ pin is hard-shorted to the 12 V battery, the short-circuit detector opens SW2 and limits the current by the high impedance M2b.

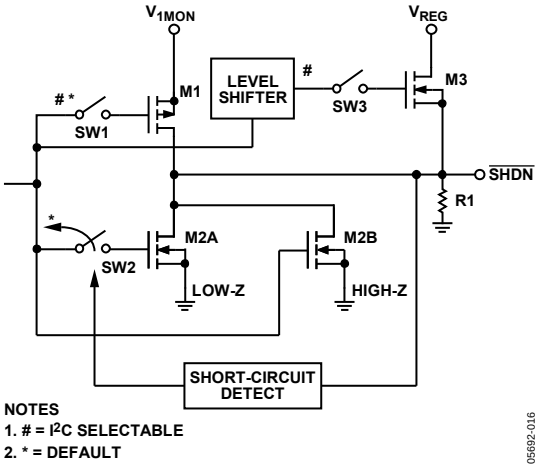


Figure 16. Shutdown Output

RESET OUTPUT, $\overline{\text{RESET}}$

The reset output, $\overline{\text{RESET}}$, is triggered by V_{3MON} or V_{4MON} underthreshold values. $\overline{\text{RESET}}$ activation can also be the result of the processor not generating the proper watchdog signal, if $\overline{\text{MR}}$ input is triggered, or if $\overline{\text{SHDN}}$ is activated.

The reset generator asserts the $\overline{\text{RESET}}$ signal based on the following conditions:

- During power-up
- When V_{3MON} drops below the threshold (see Figure 10)
- When V_{4MON} drops below the threshold (see Figure 12)
- When $\overline{\text{SHDN}}$ output is asserted (see Figure 7 and Figure 14); $\overline{\text{RESET}}$ follows $\overline{\text{SHDN}}$ hold and delay timings if triggered by the $\overline{\text{SHDN}}$ output
- When the external monitoring processor cannot issue the necessary WDI signal (see Figure 13 and Figure 14)
- When $\overline{\text{MR}}$ is asserted (see Figure 15)

$\overline{\text{RESET}}$ is active low by default, but can be configured for active high operation. Register 0x0D[1] controls the activation polarity of $\overline{\text{RESET}}$.

- Register 0x0D[1] = 0: $\overline{\text{RESET}}$ is active low
- Register 0x0D[1] = 1: $\overline{\text{RESET}}$ is active high

The $\overline{\text{RESET}}$ signal is asserted and maintained except when it is triggered by the WDI, which is described in the Watchdog Input section. The $\overline{\text{RESET}}$ signal is released after the programmable hold time, t_{RS_HOLD}.

As shown in Figure 17, the $\overline{\text{RESET}}$ output is push-pull configured with the rail voltage of V_{3MON}.

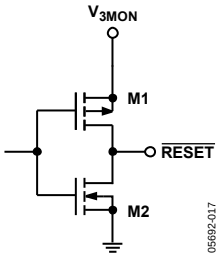


Figure 17. Reset Output

SHUTDOWN WARNING, $\overline{\text{SHDNWARN}}$

An early shutdown warning is available for the system processor to identify the source of failure and take appropriate action before shutting down the external devices. Whenever the voltage at V_{1MON} is detected as overvoltage or undervoltage, or the voltage at V_{2MON} falls below the threshold, $\overline{\text{SHDNWARN}}$ outputs a Logic 0. If the processor sees a logic low on this pin, the processor may issue an I^2C read command to identify the cause of failure reported in the fault detect/status register, at Address 0x19. The processor may store the information in external EEPROM as a record of failure history.

V_{4OUT} OUTPUT

V_{4OUT} is an open-drain output triggered by V_{4MON} with a minimum propagation delay, t_{V4OUT_DELAY}. V_{4OUT} can be used as a PWM control over an external device or used as a monitoring signal.

Most applications using V_{4OUT} require disabling of the V_{4MON} triggered reset function. This function is disabled by writing to Register 0x0D[2].

- Register 0x0D[2] = 0: enables V_{4MON} under threshold to activate $\overline{\text{RESET}}$
- Register 0x0D[2] = 1: prevents V_{4MON} under threshold from activating $\overline{\text{RESET}}$

POWER REQUIREMENTS

INTERNAL POWER, V_{REG}

The AD5100 internal power, V_{REG}, is derived from V_{1MON} and becomes active when V_{2MON} reaches 2.2 V. V_{2MON} is used to turn AD5100 on and off with a different behavior depending on the V_{2MON} monitoring mode selection.

By default, the AD5100 turns on when the voltage at V_{2MON} rises above the logic threshold, V_{2MON_ON}. When V_{2MON} falls below the logic threshold, V_{2MON_OFF}, AD5100 turns off 2 seconds after $\overline{SHDN}$ is deasserted. Note that AD5100 requires 5 µs to start up and that V_{1MON} must be applied before V_{2MON}. Extension of the AD5100 turn-off allows the system to complete any housekeeping tasks before the system is powered off. Figure 19 shows the default V_{2MON} and V_{REG} waveforms.

Rising Edge Triggered Wake-Up Mode

If rising edge triggered wake-up V_{2MON} mode is selected instead, the AD5100 does not turn off when V_{2MON} returns to a logic low. To configure the part into rising edge triggered mode, set the V_{2MON} off threshold register, Register 0x04[3:1], to 1001.

In this mode, once the part is powered on, it can only be powered down by an I^2C power-down instruction or by removing the supply on the V_{1MON} pin. To power down the part over the I^2C bus while in rising edge triggered mode, the user must first ensure that the software power down feature is enabled.

- Register 0x18[3] = 0: enable software power-down feature
- Register 0x18[3] =1: disable software power-down feature

The user must then write to Register 0x17[0], to actually power down the AD5100.

- Register 0x17[0] = 0: AD5100 not in software power-down
- Register 0x17[0] = 1: power down AD5100

This feature is for applications that use a wake-up signal.

V_{OTP}

A 5.5 V supply voltage is needed only during OTP fuse programming. This voltage should be provided by an external source during factory programming and should have 5.5 V/100 mA driving capability. The OTP programming takes a maximum of 12 ms for each register. V_{OTP} is not required for normal operation. The V_{OTP} has dual functions; it is used for programming the nonvolatile memory fuse arrays, as well as serving as a compensation network for internal power stability. As a result, a bypass capacitor must be connected at the V_{OTP} pin at all times. A low ESR 10 µF tantalum capacitor is recommended.

AD5100 achieves the OTP function through blowing internal fuses. Users should always apply the 5.5 V one-time programmable voltage at the first fuse programming attempt. Failure to comply with this requirement may lead to a change in the fuse structures, rendering programming inoperable.

Poor PCB layout introduces parasitic inductance that may affect the fuse programming voltage. Therefore, it is mandatory that a 10 µF tantalum capacitor be placed as close as possible to the V_{OTP} pin. The value and the type of C2 are important. It should provide both a fast response and large supply current handling with minimum supply droop during programming (see Figure 18).

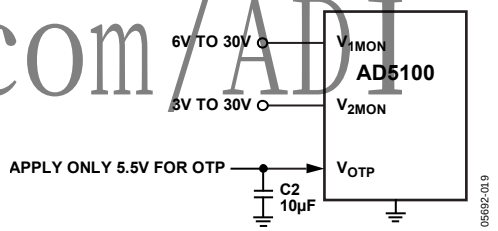


Figure 18. Power Supply Requirement

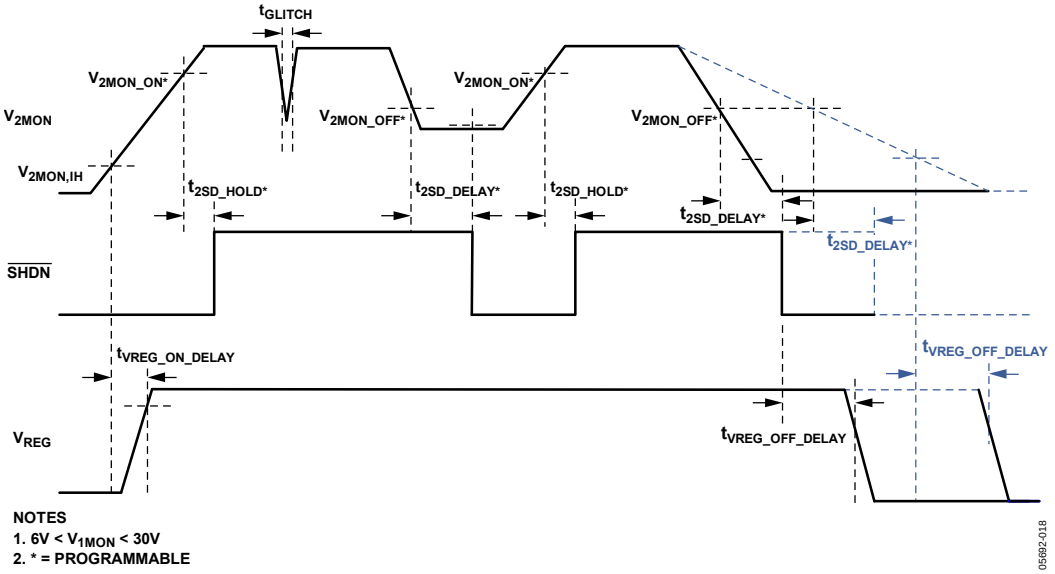


Figure 19. Internal Power V_{REG} vs. V_{2MON} Timing Diagrams (Default)

PROTECTION

For automotive applications, proper external protections on the AD5100 are needed to ensure reliable operation. The V_{1MON} is likely to be used for battery monitoring. The V_{2MON} is likely to be used for ignition switch or other critical inputs. As a result, these inputs may need additional protections such as EMI, load dump, and ESD protections. In addition, battery input requires reverse battery protection and short-circuit fuse protection (see Figure 20).

Overcurrent Protection

If the V_{1MON} is shorted internally in the AD5100 to GND, the short-circuit protection kicks in and limits subsequent current to 150 mA in normal operation or 50 mA when the V_{OTP} is executed.

Thermal Shutdown

When the AD5100 junction temperature is near the junction temperature limit, it automatically shuts down and cuts out the power from V_{1MON}. The part resumes operation when the device junction temperature returns to normal.

ESD Protection

It is common to require a contact rating of ±8 kV and a no contact or air rating of ±15 kV ESD protection for the automotive electronics. As a result, an ESD-rated protection device must be used, such as MMBZ27VCL, a dual 40 W transient voltage suppressor (TVS) at the V_{1MON} and V_{2MON}.

Load Dump Protection

A load dump is a severe overvoltage surge that occurs when the car battery is being disconnected from a spinning alternator and a resulting long duration, high voltage surge is introduced into the supply line. Therefore, external load dump protection is recommended. Typically, the load dump overvoltage lasts for a few hundred milliseconds and peaks at around 40 V to 70 V, while current can be as high as 1 A. As a result, a load dump-rated TVS D1 and D2, such as SMCJ17, are used to handle the surge energy. A series resistor is an inline current limiting resistor; it should be adequate to limit the current without significant drop and yet small enough to not affect the input monitoring accuracy.

Reverse Battery Protection

Reverse battery protection can be provided by a regular diode if the battery monitoring accuracy can be relaxed. Otherwise, a 60 V P-channel power MOSFET, like the NDT2955, can be used. Because of the MOSFET internal diode, the battery first conducts through the P1 body diode as soon as the voltage reaches its source terminal. The voltage divider provides adequate gate-to-source voltage to turn on P1, and the voltage drop across the FET is negligible. The resistor divider values are chosen such that the maximum V_{GS} of the P1 is not violated and the current drawn through the battery is only a few microamps.

EMI Protection

For EMI protection, a ferrite bead or EMC rated inductor, such as DR331-7-103, can be used.

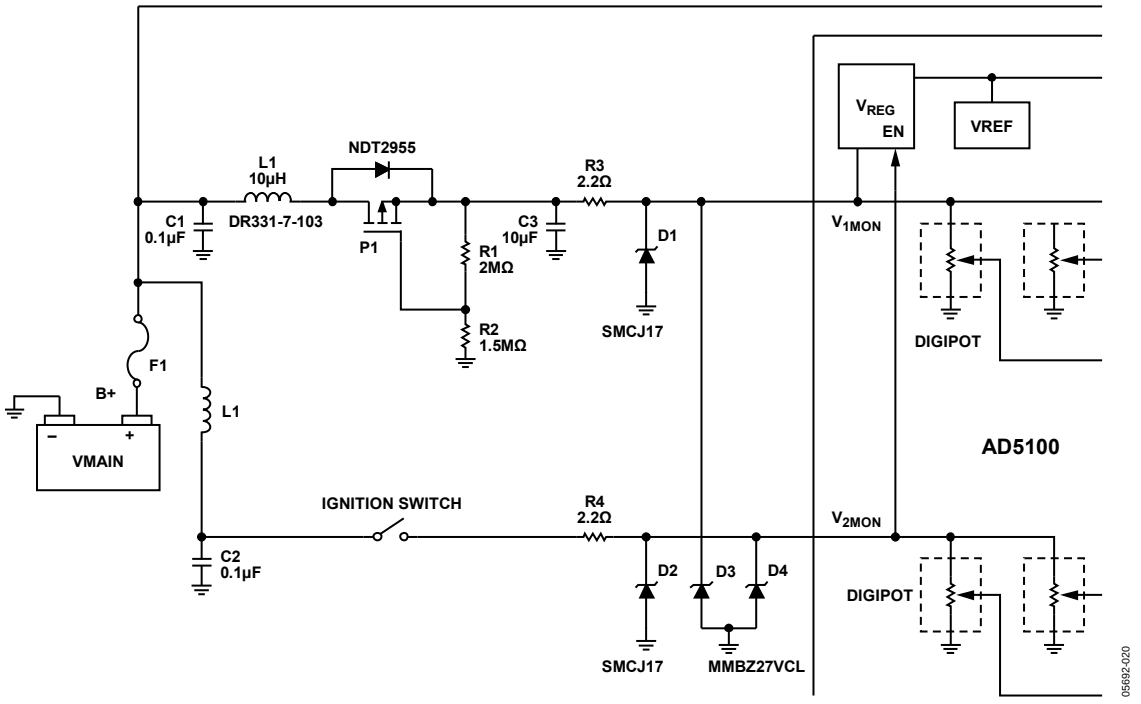


Figure 20. Protection Circuits

AD5100 REGISTER MAP

Table 11 outlines the AD5100 register map, used to configure and control all parameters and functions in the AD5100, and indicates whether registers are writable, readable, or permanently settable. All registers have the same address for read and write operations.

The AD5100 ships from its manufacturing factory with default power-up values as listed in the last column. The user can experiment with different settings in the various threshold, delay, and configuration registers. Once evaluation is complete, the user's own power-up default values can be programmed via a one-time program (OTP) feature. When all desired settings have been programmed (or the user is satisfied with the manufacturer's defaults), a lock-out bit can be programmed (via OTP) to prevent further/erroneous settings from being programmed. The lockout bit is Register 0x15[3].

Some users may use the AD5100 as a set-and-forget device, that is, program some default values and never need to change these over the life of the application. However, some users may require on-the-fly flexibility, that is, the ability to change settings to values other than those they choose as their defaults. An additional feature of the AD5100 is the ability to temporarily override the OTP executed settings and still allow users to program the parts dynamically in the field. All override values revert to OTP-executed settings once the AD5100 is power cycled.

Register writing, reading, OTP, and override are explained in the I²C Serial Interface section.

Table 11. AD5100 Register Map

Register Address	Read/ Write	Permanently Settable	Register Name and Bit Description		Pre-OTP Power-On Default[1]
0x01	R/W	Yes	V_{1MON} overvoltage threshold		0x00 (18.00 V)
			Bit No.	**Description**	
			[3:0]	Four bits used to program V_{1MON} OV threshold	
			[7:4]	Reserved	
0x02	R/W	Yes	V_{1MON} undervoltage threshold		0x00 (8.43 V)
			Bit No.	**Description**	
			[3:0]	Four bits used to program V_{1MON} UV threshold	
			[7:4]	Reserved	
0x03	R/W	Yes	V_{2MON} turn-on threshold		0x00 (7.47 V)
			Bit No.	**Description**	
			[3:0]	Four bits used to program V_{2MON} on threshold	
			[7:4]	Reserved	
0x04	R/W	Yes	V_{2MON} turn-off threshold		0x00 (6.95 V)
			Bit No.	**Description**	
			[3:0]	Four bits used to program V_{2MON} off threshold	
			[7:4]	Reserved	
0x05	R/W	Yes	V_{3MON} $\overline{\text{RESET}}$ Threshold		0x00 (2.93 V)
			Bit No.	**Description**	
			[2:0]	Three bits used to program V_{3MON} $\overline{\text{RESET}}$ threshold	
			[7:3]	Reserved	
0x06	R/W	Yes	V_{4MON} $\overline{\text{RESET}}$ threshold		0x00 (7.54 V)
			Bit No.	**Description**	
			[2:0]	Three bits used to program V_{4MON} $\overline{\text{RESET}}$ threshold	
			[7:3]	Reserved	
0x07	R/W	Yes	V_{1MON} OV/UV triggered $\overline{\text{SHDN}}$ hold (t_{1SD_HOLD})		0x00 (200 ms)
			Bit No.	**Description**	
			[2:0]	Three bits used to program V_{1MON} OV/UV triggered $\overline{\text{SHDN}}$ hold time	
			[7:3]	Reserved	

Register Address	Read/ Write	Permanently Settable	Register Name and Bit Description		Pre-OTP Power-On Default[1]
0x08	R/W	Yes	V_{1MON} OV/UV triggered $\overline{SHDN}$ delay (t_{1SD_DELAY})		0x00 (1200 ms)
			Bit No.	**Description**	
			[2:0]	Three bits used to program V1MON OV/UV triggered $\overline{SHDN}$ delay time	
			[7:3]	Reserved	
0x09	R/W	Yes	V_{2MON} turn-on triggered $\overline{SHDN}$ hold (t_{2SD_HOLD})		0x00 (10 ms)
			Bit No.	**Description**	
			[2:0]	Three bits used to program V_{2MON} t_{ON} triggered $\overline{SHDN}$ hold time	
			[7:3]	Reserved	
0x0A	R/W	Yes	V_{2MON} turn-off triggered $\overline{SHDN}$ delay (t_{2SD_DELAY})		0x00 (100 ms)
			Bit No.	**Description**	
			[2:0]	Three bits used to program V_{2MON} t_{OFF} triggered $\overline{SHDN}$ delay time	
			[7:3]	Reserved	
0x0B	R/W	Yes	$\overline{RESET}$ hold (t_{RS_HOLD})		0x00 (200 ms)
			Bit No.	**Description**	
			[2:0]	Three bits used to program $\overline{RESET}$ hold time	
			[7:3]	Reserved	
0x0C	R/W	Yes	Watchdog timeout (t_{WD})		0x00 (1500 ms)
			Bit No.	**Description**	
			[2:0]	Three bits used to program watchdog timeout time	
			[7:3]	Reserved	
0x0D	R/W	Yes	$\overline{RESET}$ configuration		0x00
			Bit No.	**Description**	
			[0]	0: $\overline{RESET}$ is active when $\overline{SHDN}$ is active 1: $\overline{RESET}$ is not active when $\overline{SHDN}$ is active	
			[1]	0: $\overline{RESET}$ active low 1: $\overline{RESET}$ active high	
			[2]	0: enables V_{4MON} under threshold, causing $\overline{RESET}$ 1: prevents V_{4MON} under threshold from causing $\overline{RESET}$ (for V_{4OUT} applications)	
			[3]	0: floating WDI does not activate $\overline{RESET}$ 1: floating WDI activates $\overline{RESET}$	
			[7:4]	Reserved	
0x0E	R/W	Yes	$\overline{SHDN}$ rail voltage configuration		0x00
			Bit No.	**Description**	
			[2:0]	Reserved	
			[3]	0: $\overline{SHDN}$ rail = V_{1MON} 1: $\overline{SHDN}$ rail = V_{REG}	
			[7:4]	Reserved	
0x0F	R/W	Yes	Watchdog mode		0x00
			Bit No.	**Description**	
			[2:0]	Reserved	
			[3]	0: standard mode 1: advanced mode	
			[7:4]	Reserved	

Register Address	Read/ Write	Permanently Settable	Register Name and Bit Description		Pre-OTP Power-On Default[1]
0x15	R/W	Yes	Program lock (inhibit further programming)		0x00
			Bit No.	**Description**	
			[2:0]	Reserved	
			[3]	0: further fuse programming allowed 1: further fuse programming disabled (note that this bit is OTP only)	
			[7:4]	Reserved	
0x16	R/W	No	Special function 1		0x00
			Bit No.	**Description**	
			[0]	0: OTP enables 5 µA fuse readback sense current 1: OTP enables 0.55 µA fuse readback sense current	
			[1]	0: OTP disables blowing fuses 1: OTP enables blowing fuses	
			[2]	0: software assertion of $\overline{\text{SHDN}}$ pin is inactive 1: pulls $\overline{\text{SHDN}}$ pin low	
			[3]	0: override of permanent settings inactive 1: override of permanent settings active	
			[7:4]	Reserved	
0x17	R/W	No	Special function 2		0x00
			Bit No.	**Description**	
			[0]	0: software power-down of AD5100 inactive 1: software power-down of AD5100 active[2]	
			[7:1]	Reserved	
0x18	R/W	No	Disable special functions[3]		0x00
			Bit No.	**Description**	
			[0]	0: allows override of any of the registers in memory except Register 0x16 Bit[2:0] and Register 0x17 Bit[0] 1: disables override of any of the registers in memory except Register 0x16 Bit[2:0] and Register 0x17 Bit[0]	
			[1]	0: allows OTP function 1: disables OTP function	
			[2]	Reserved	
			[3]	0: allows software power-down function 1: disables software power-down function	
			[4]	0: allows software assertion of $\overline{\text{SHDN}}$ pin 1: disables software assertion of $\overline{\text{SHDN}}$ pin	
			[7:5]	Reserved	

Register Address	Read/ Write	Permanently Settable	Register Name and Bit Description		Pre-OTP Power-On Default[1]
0x19	Read-only	No	Fault detect and status (Bits[3:0] are level triggered bits that indicate the current state of the comparators monitoring the V_{1MON} and V_{2MON} input pins; Bits[6:4] are edge triggered fault detection bits that indicate what error conditions were present when a $\overline{SHDN}$ event occurred)		0x40
			Bit No.	**Description**	
			[0]	1 = V_{2MON} input < V_{2MON} off threshold	
			[1]	1 = V_{2MON} input > V_{2MON} on threshold	
			[2]	1 = V_{1MON} input < V_{1MON} UV threshold	
			[3]	1 = V_{1MON} input > V_{1MON} OV threshold	
			[6:4]	000: none	
				001: V_{1MON} UV only	
				010: V_{1MON} OV only	
				011: never occurred	
				100: V_{2MON} below off only (default)	
				101: V_{1MON} UV and V_{2MON} below off both occurred	
				110: V_{1MON} OV and V_{2MON} below off both occurred	
				111: never occurred	
			[7]	Reserved	

[1] Default settings of AD5100 when shipped from manufacturer's factory.
[2] V_{2MON} must be 0 V (that is, V_{2MON} must be configured in edge sensitive mode) for software power-down.
[3] These register bits are set only. To clear them, the AD5100 must be power cycled. In some cases, the AD5100 can be connected to an I^2C bus with lots of activity. Setting these bits is an added means of ensuring that any erroneous activity on the bus does not cause AD5100 special functions to become active.

I²C SERIAL INTERFACE

Control of the AD5100 is accomplished via an I²C-compatible serial bus. The AD5100 is connected to this bus as a slave device (the AD5100 has no master capabilities).

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which occurs when SDA goes from high to low while SCL is high. The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit that determines whether data is read from or written to the slave device
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In the read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse and high during the 10th clock pulse to establish a stop condition.

For the AD5100, write operations contain either one or two bytes, while read operations contain one byte. The AD5100 makes use of an address pointer register. This address pointer sets up one of the other registers for the second byte of the write operation or for a subsequent read operation. Table 12 shows the structure of the address pointer register. Bits [6:0] signify the address of the register that is to be written to or read from. Bit 7 is used when OTP mode is invoked (use of this bit is explained in the One-Time Programmable (OTP) Options section) and should be 0 for normal write/read operations.

Table 12. Address Pointer Register Structure

Bit Number	Function
7	OTP enable
6	Address Bit 6
5	Address Bit 5
4	Address Bit 4
3	Address Bit 3
2	Address Bit 2
1	Address Bit 1
0	Address Bit 0 (LSB)

SCL

The serial input register clock pin shifts in one bit at a time on positive clock edges. An external 2.2 kΩ to 10 kΩ pull-up resistor is needed. The pull-up resistor should be tied to V_{3MON}, provided V_{3MON} is sub-5 V.

SDA

The serial data input/output pin shifts in one bit at a time on positive clock edges, with the MSB loaded first. An external 2.2 kΩ to 10 kΩ pull-up resistor is needed. The pull-up resistor should be tied to V_{3MON} , provided V_{3MON} is sub-5 V.

AD0

The AD5100 has a 7-bit slave address. The six MSBs are 010111, and the LSB is determined by the state of the AD0 pin. When the I²C slave address pin, AD0, is low, the 7-bit AD5100 slave address is 0101110. When AD0 is high, the 7-bit AD5100 slave address is 0101111 (pulled up to 3.3 V maximum).

The AD0 pin allows the user to connect two AD5100 devices to the same I²C bus . Table 13 and Figure 21 show an example of two AD5100 devices operating on the same serial bus independently.

Table 13. Slave Address Decoding Scheme

AD0 Programming Bit	AD0 Device Pin	Device Addressed
0	0 V	0x2E (U1)
1	3.3 V max	0x2F (U2)

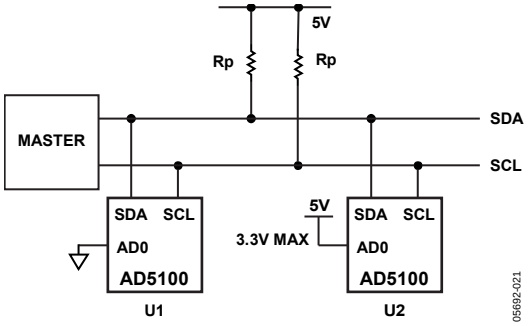


Figure 21. Two AD5100 Devices on One Bus

WRITING DATA TO AD5100

When writing data to the AD5100, the user begins by writing an address byte followed by the R/$\overline{W}$ bit set to 0. The AD5100 acknowledges (if the correct address byte is used) by pulling the SDA line low during the ninth clock pulse. The user then follows with two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second byte is the data to be written to the internal data register. After each byte, the AD5100 acknowledges by pulling the SDA line low during the ninth clock pulse. Figure 22 illustrates this operation.

READING DATA FROM AD5100

When reading data from an AD5100 register, there are two possibilities.

- If the AD5100 address pointer register value is unknown or not at the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the AD5100, but only a value containing the register address is sent because data is not to be written to the register. This is shown in Figure 23. A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte from the data register. This is shown in Figure 24.
- If the address pointer is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register.

Table 14 shows the readback data byte structure. Bits[6:0] contain the data from the register just read. Bit 7 only has significance when OTP mode is being used, and should be ignored for normal read operations. The majority of AD5100 registers are four bits wide, with only the fault detect and status register and disable special functions register at seven bits and five bits wide, respectively.

Table 14. Readback Data Byte Structure

Bit Number	Function
7	OTP Okay
6	D6
5	D5
4	D4
3	D3
2	D2
1	D1
0	D0 (LSB)

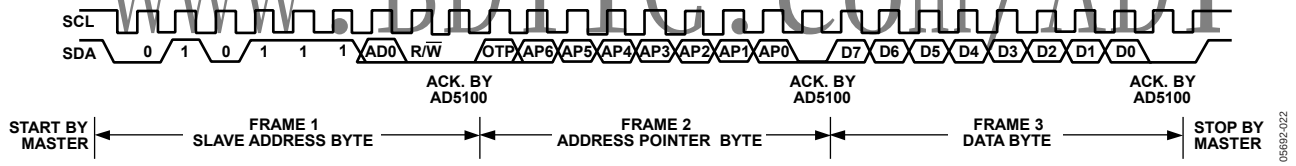


Figure 22. Writing a Register Address to the Address Pointer Register, Then Writing Data to the Selected Register

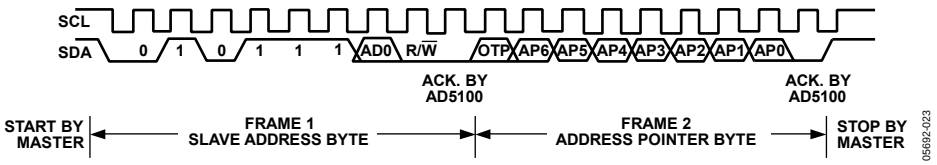


Figure 23. Dummy Write to Set Proper Address Pointer

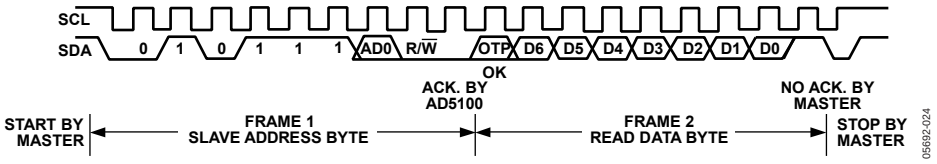


Figure 24. Read Data from the Address Pointer Register

PERMANENT SETTING OF AD5100 REGISTERS (OTP FUNCTION)

When the user wants to permanently program settings to the AD5100, the one-time program (OTP) function is invoked (note the requirements for the capacitor on the V_{OTP} pin in the Power Requirements section). To complete a permanent program cycle for a particular register, the following sequence should be used:

1. Set Bit 0 = 1 in Register 0x16 using a normal write operation.
2. Set Bit 1 = 1 in Register 0x16 using a normal write operation.
3. Apply a 5.5 V (100 mA) voltage source to the OTP pin. This provides the current for the programming cycle.
4. Write the desired permanent data to the register of choice, using a write operation with the OTP bit set to 1 in the address pointer byte.
5. Wait a period of 12 ms for the AD5100 to perform the permanent setting of the internal register.

The user has the opportunity to check whether the AD5100 is programmed correctly by performing a read instruction with the OTP bit set to 1 in the address pointer byte (for example, set the address pointer to 0x81 to check $V_{1MON-OV}$) and monitoring the state of Bit 7 (OTP okay) in the read back data byte.

- OTP okay = 1 indicates that the AD5100 is programmed correctly
- OTP okay = 0 indicates that the AD5100 is programmed incorrectly

Note that read back of the OTP okay bit is available only for the read cycle following immediately after the program cycle. If a write or read of a different register is done immediately after the program cycle, the opportunity for verifying whether the programming was successful will have been missed. Figure 25 shows the recommended way of executing a program, then reading back and verifying the V_{1MON} overvoltage threshold register (assuming that Step 1 to Step 3 have already been completed).

When all default registers have been programmed, the lock bit should be set. User-programmed defaults do not become active until the lock bit is programmed. Programming the lock bit is done in exactly the same manner as all other registers in Table 11. The lock bit is Register 0x15, Bit 3.

TEMPORARY OVERRIDE OF DEFAULT SETTINGS

Even with the lock bit set, it is possible to temporarily override the default values of any of the permanently programmable registers. To override a permanent setting in a particular register (when the lock bit is programmed), the following sequence should be used:

1. Set Bit 3 = 1 in Register 0x16 (special function 1).
2. Write the desired temporary data to the register of choice.

While the override bit (Bit 3) is set in Register 0x16, the user can override any registers by simply writing to them with new data.

To reset an overridden register to its default setting, the following sequence should be used:

1. Set Bit 3 = 0 in Register 0x16.
2. Write a dummy byte to the register of choice.

Clearing the override bit in Register 0x16 does not cause all overridden registers to revert to their defaults at the same time. For example, imagine that the user overrides Register 0x01, Register 0x02, and Register 0x03. If the user subsequently clears the override bit in Register 0x16 and writes a dummy byte to Register 0x01, Register 0x01 reverts to its default value. However, Register 0x02 and Register 0x03 still contain their override data. To revert both registers to their default values, the user must write dummy data to each register individually.

Power cycling the AD5100 also resets all registers to their programmed defaults.

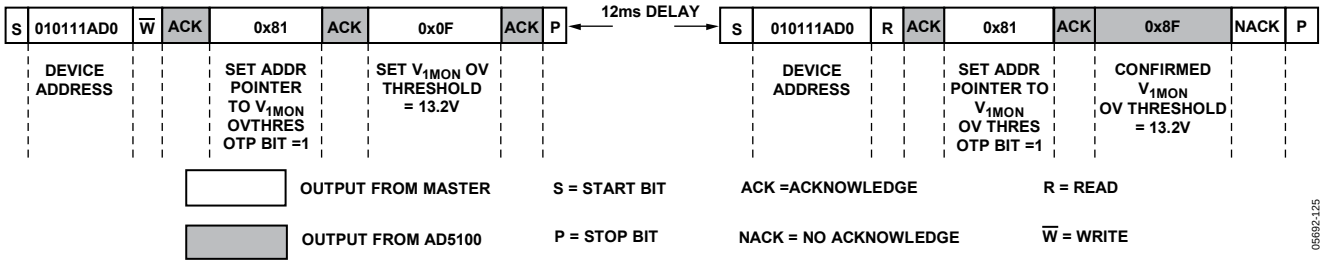


Figure 25. Setting and Validating OTP Register Setting

APPLICATIONS INFORMATION

CAR BATTERY AND INFOTAINMENT SYSTEM SUPPLY MONITORING

The AD5100 has two high voltage monitoring inputs with shutdown and reset controls over external devices. For example, the V_{1MON} and V_{2MON} can be used to monitor the signals from a car battery and an ignition key in an automobile, respectively (see Figure 26). The shutdown output can be connected to the shutdown pin of an external regulator to prevent false conditions such as a weak battery or overcharging of a battery by an alternator. The reset output can be used to reset the processor in the event of a hardware or software malfunction. An example of the input and output responses of this circuit is shown in Figure 27.

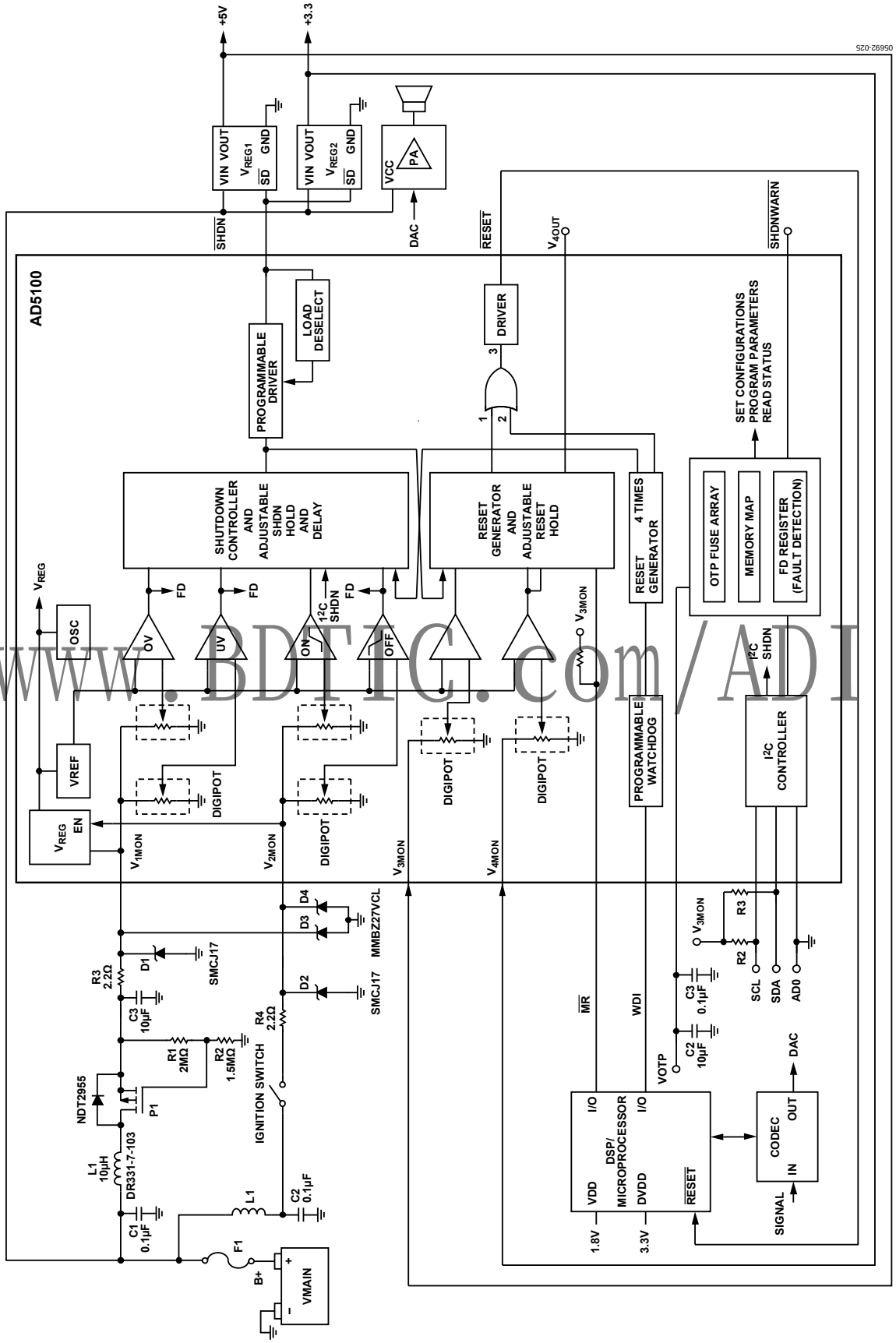


Figure 26. Typical DSP in Car Infotainment Application

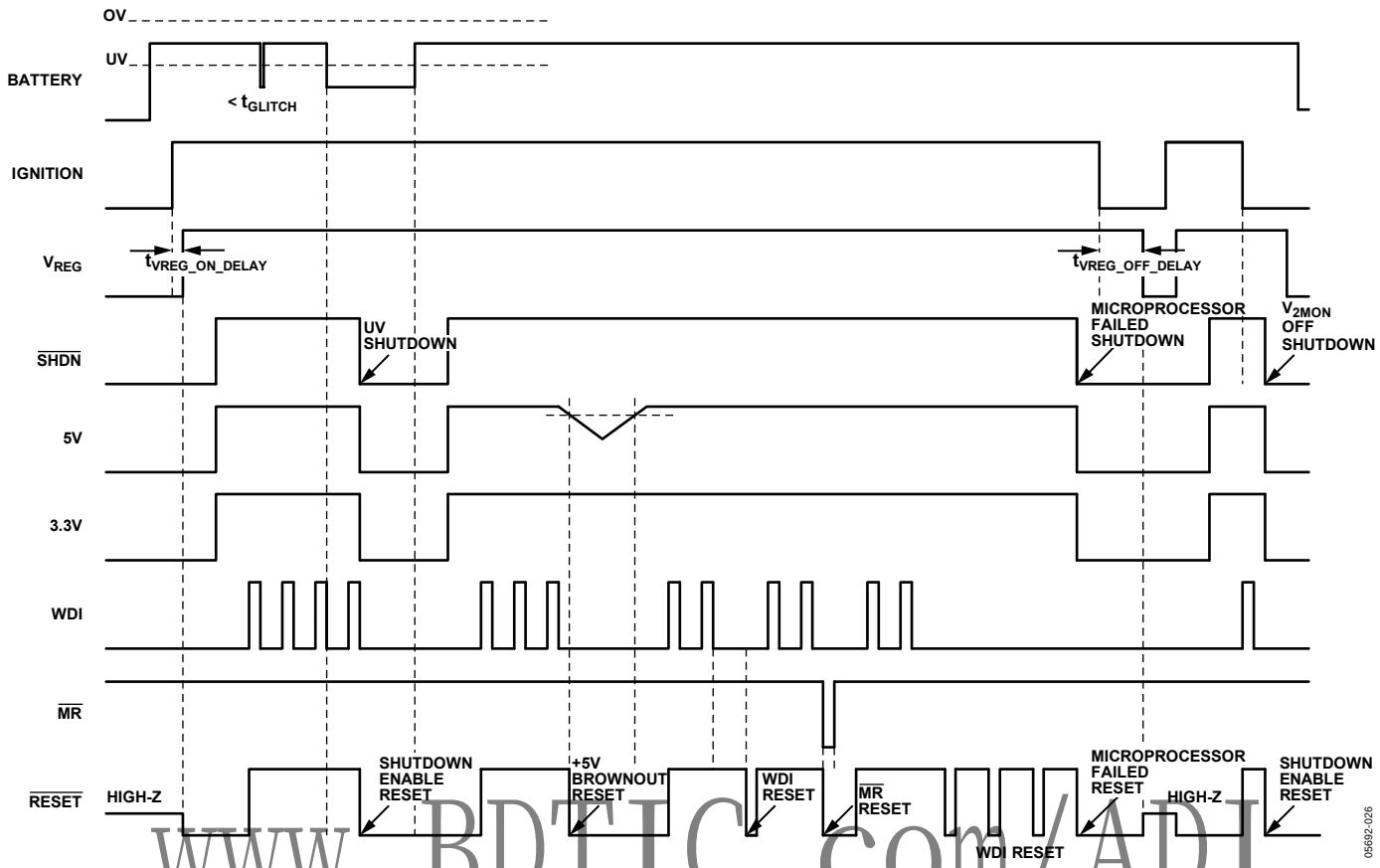


Figure 27. Example of SHDN and RESET Responses of Circuit Shown in Figure 26

BATTERY MONITORING WITH FAN CONTROL

V_{4MON} can be used with V_{4OUT} in tandem to form a simple PWM control circuit. For example, as shown in Figure 28, when a temperature sensor output connects to the V_{4MON} input, with the proper threshold level set, V_{4OUT} outputs high whenever the temperature goes above the threshold. This turns on the FET switch, which activates the fan. When V_{TEMP} drops below the threshold, V_{4OUT} decreases, which turns off the fan.

BATTERY STATE OF CHARGE INDICATOR AND SHUTDOWN EARLY WARNING MONITORING

In the automotive application, the system designer may set the battery threshold to the lowest level to allow an automobile to start at the worst-case condition. If the battery remains at the low voltage level, it is indeed a poor battery. However, there is no way to warn the driver. As a result, the system designer can use V_{4OUT} as the battery warning indicator. By stepping down the battery voltage monitored at V_{4MON}, the LED is lit, which gives a battery replacement warning. The circuit is shown in Figure 30.

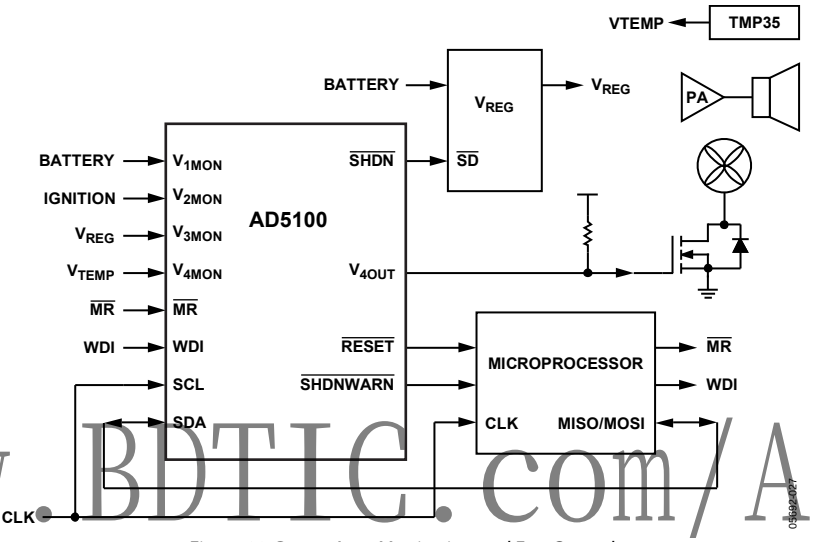


Figure 28. Power Amp Monitoring and Fan Control

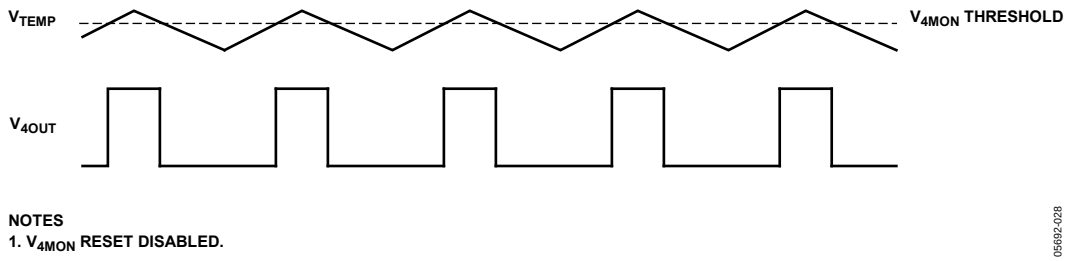


Figure 29. V_{4OUT} with Respect to V_{TEMP}, with V_{4MON} $\overline{RESET}$ Disabled in Circuit Shown in Figure 28

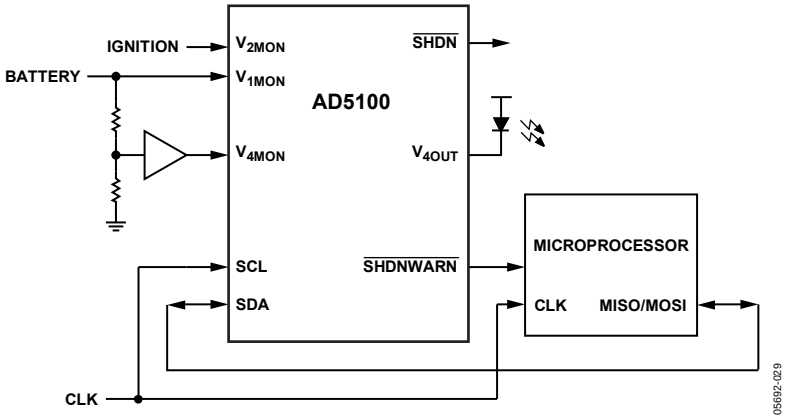


Figure 30. Battery State of Charge Indication

RISING EDGE TRIGGERED WAKE-UP MODE

As indicated in Figure 31, the microprocessor can control its own power-down sequence using the rising edge triggered wake-up signal. The operator must select the rising edge triggered wake-up mode setting for the V_{2MON} turn-off threshold value, as shown in Table 6, by setting Register 0x04[3:1] = 1001.

When the rising edge wake-up signal is detected by V_{2MON}, the AD5100 is powered up with the $\overline{SHDN}$ pin pulled high. The external regulator is turned on to supply power to the microprocessor. A reset pulse train is generated at the reset output if there is no watchdog activity. The pulse continues until the correct watchdog signal appears at the AD5100 WDI pin. The shutdown pin remains high as long as the AD5100 continues to receive the correct watchdog signal.

When the microprocessor finishes its housekeeping tasks or powers down the software routine, it stops sending a watchdog signal. In response, the AD5100 generates a reset. The shutdown pin is pulled low 2 seconds after, and the regulator output drops to 0 V, which shuts down the microprocessor. At that point, the AD5100 enters sleep mode.

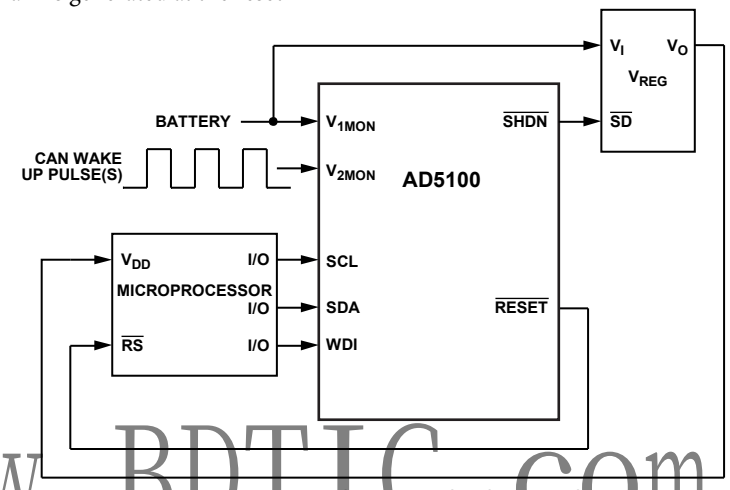


Figure 31. Rising Edge Triggered Wake-Up Mode

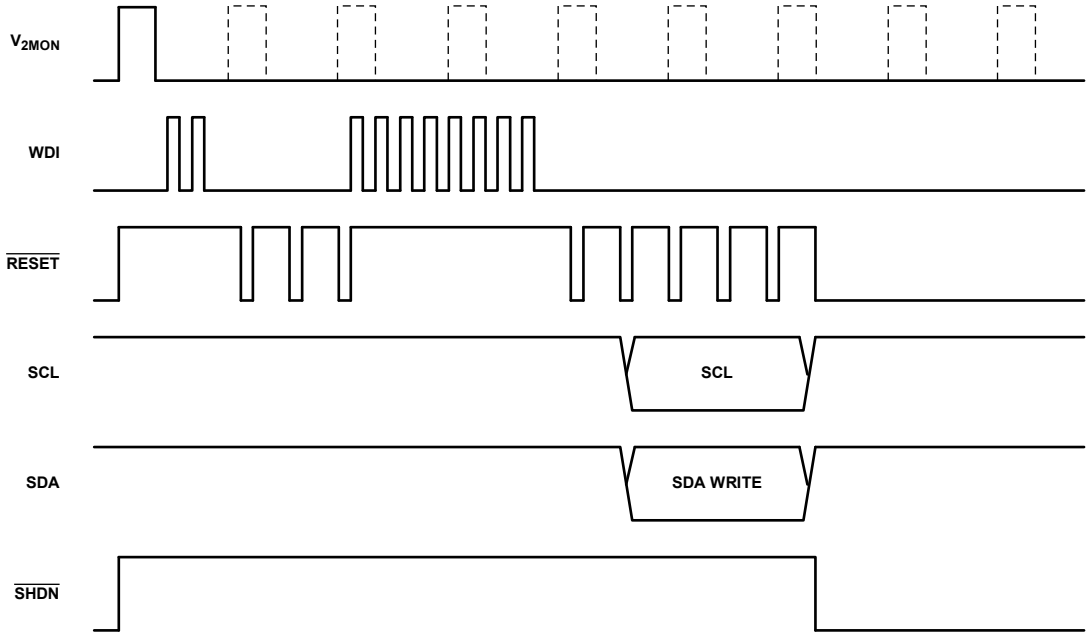
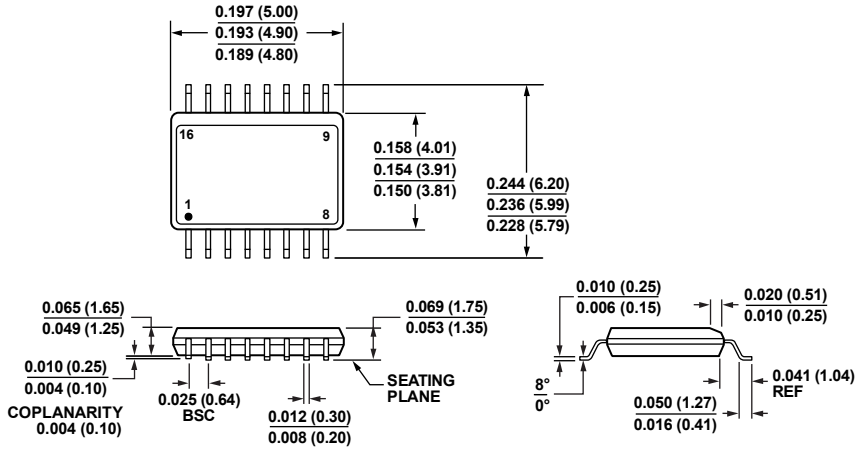


Figure 32. Rising Edge Triggered Operation of Circuit Shown in Figure 31

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012808-A

Figure 33. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD5100YRQZ-RL7[1]	−40°C to +125°C	16-Lead QSOP	RQ-16	1,000
AD5100YRQZ[1]	−40°C to +125°C	16-Lead QSOP	RQ-16	9,800

[1] Z = RoHS Compliant Part.

NOTES