ZARLINK SEMICONDUCTOR

Design Conversion Guide

Switching from 5.0 V QSLAC™ Devices (Am79Qxxx) to 3.3 V QLSLAC™ Devices (Le58QLxxx) in Existing Designs

Application Note

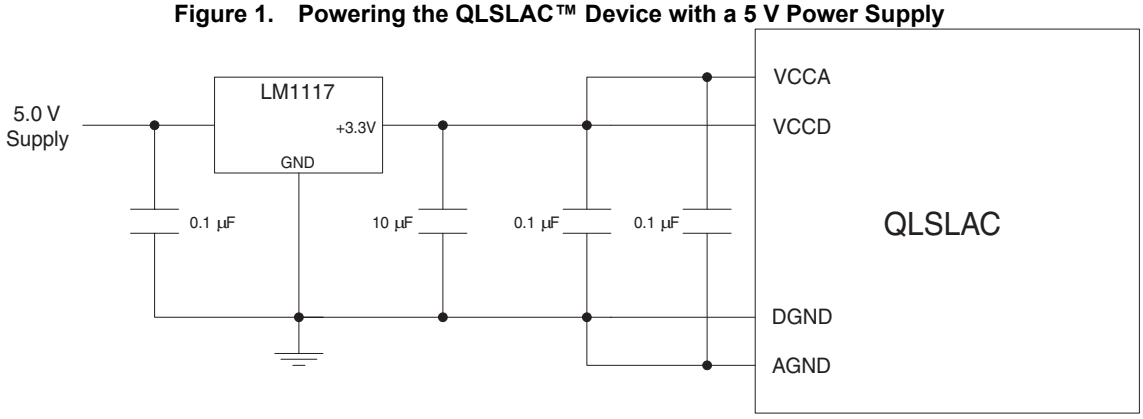
This document is a guide for converting existing linecard designs using Zarlink's QSLAC™ devices to designs using the newer QLSLAC™ devices with a minimal amount of rework. The QLSLAC device is a low voltage and low power replacement for the QSLAC device. Because of the lower voltage, the analog output voltage is reduced compared to the QSLAC device, resulting in lower receive gains. Lower receive levels may be easily compensated in the Subscriber Line Interface Circuit. Zarlink recommends steps in this document that will allow full software compatibility with existing QSLAC device designs with only minor hardware modifications.

1.0 POWER SUPPLY CONSIDERATIONS

While the QSLAC device requires +5.0 V digital and analog power supplies with ±5% tolerances, the QLSLAC device requires +3.3 V supplies. Some back planes may provide both a 5.0 V and a 3.3 V supply, in which case conversion to the QLSLAC device is straightforward. In cases where only a 5.0 V supply is available, a 5.0 V to 3.3 V voltage regulator must be added to the linecard. The voltage regulator should be able to drive at least 55 mA per QLSLAC device.

One such voltage regulator is National Semiconductor's LM1117-3.3, which costs $0.32 per regulator and can source up to 800 mA of current. A single LM1117-3.3 regulator is sufficient to handle the power supply requirements of a 32 channel linecard with an amortized cost of $0.01 per channel. Figure 1 shows a schematic of the voltage regulator connected to the QLSLAC device. Other possible voltage regulators include Analog Devices Inc.'s ADP3335 (www.analog.com; Rev 0, 04/00), National Semiconductor Corp.'s LM2931 (www.national.com; DS005254), and Maxim Integrated Product's MAX8867 (www.maxim-ic.com; 19-1302, Rev 2, 03/01). Most of these voltage regulators require at least 10 µF of capacitance at the output. The LM1117, for instance, requires at least a 10 µF tantalum capacitor with low equivalent series resistance (ESR). Kemet Corporation (www.kemet.com, F-3102F-TA) supplies tantalum capacitors that can be used in this type of application.

Figure 1. Powering the QLSLAC™ Device with a 5 V Power Supply



2.0 INTERFACE CONSIDERATIONS

Interface specifications for the MPI, the PCM, master clock (MCLK), and SLIC control outputs/inputs are virtually identical between the two SLAC™ devices to maximize compatibility.

2.1 Microprocessor Interface

The MPI for the QLSLAC device is almost identical to the MPI of the QSLAC device, including 5.0 V tolerant inputs, similar timing requirements, and the same logic thresholds for data clock, chip select, and data I/O inputs. One difference is that the maximum data clock (DCLK) rate increased from 4.096 MHz for the QSLAC device to 8.192 MHz for the QLSLAC device. Due to this difference, the minimum DCLK low pulse is halved, and the chip select set-up time was decreased from 70 ns to 30 ns. The only other difference is that the output voltage for the data I/O reaches 3.3 V rather than 5.0 V. An MPI interface clocked at 4.096 MHz or less is completely compatible with both the QSLAC device and QLSLAC devices.

All MPI commands are equivalent for the two devices, with the exception of the most significant bit of the AISN and Analog Gains Register (Command 50/51h). For the QSLAC device, this bit is designated as reserved, but effectively acts as a “don’t care”. For the QLSLAC device, this bit selects between two different gain stages of the Vin analog input. The default gain (MSB = “0”) is 0.6438, but may be set to a gain of 1 if the most significant bit of the AISN register is set to “1”. This default attenuation factor is useful for achieving software compatibility in systems using Zarlink’s 5 volt SLIC device’s.

2.2 PCM Interface

For the most part, the PCM interface is the same for both the QSLAC and QLSLAC devices, including 5.0 V tolerant inputs. Frame synchronization (FS) pulse train must be provided to both the QSLAC and QLSLAC devices at an accurate 8 kHz rate. In addition, the PCM clock (PCLK) has the same timing requirements and logic thresholds for both SLACs and must be synchronous with FS in each case.

The timing requirements for the PCM receive data (DRA/DRB), transmit data (DXA/DXB) and time slot control (TSCA/TSCB) outputs are also consistent between SLAC devices. When converting from an existing QSLAC device design to a design using the QLSLAC device, the TSCA and TSCB pins can still be pulled up to the 5 volt supply, which will allow the design to maintain the same pull-up resistor values. If running at an 8.192 MHz clock and pulling up to the smaller 3.3 V supply, the value of the TSCA and TSCB pull-up resistors should decrease from 360 Ω to 240 Ω in order to maintain approximately the same rise-time to the logic threshold. Note that if running at clock speeds lower than 8.192 MHz, the value of TSCA and TSCB pull-up resistors may be proportionately larger.

2.3 Master Clock

The MCLK circuitry of the QLSLAC device is identical to that of the QSLAC device, and may be either synchronous or asynchronous to FS. However, if MCLK and FS are asynchronous, voice signals will suffer occasional phase jumps which are incompatible with V.90 modems. The implication is this: if MCLK is provided as an input (as opposed to being derived internally from PCLK) and modem performance is a concern, then the system should be capable of synchronizing MCLK to FS.

2.4 SLIC Control/Data Lines

Both the QSLAC device and the QLSLAC device have up to five TTL compatible input/output ports for controlling the SLIC, relays, LEDs or other devices. These ports are software programmable to be either inputs or outputs. As inputs, the CD1 and CD2 may be debounced, filtered, and/or demultiplexed by the QSLAC or QLSLAC device in order to provide information from the SLIC, such as off-hook or ground key detection. In general, no software or hardware modifications are necessary for SLIC control or monitoring.

As inputs, the CD pins are high impedance with leakage currents smaller than ±15µA. The active low and active high outputs are clamped to V_{CCD} and digital ground respectively for both the QLSLAC and the QSLAC chips. Consequently, the active low output level of the CD pins is lower for QLSLAC device than for the QSLAC device. The CD pins of the QLSLAC may be pulled-up to a 5 volt supply, or some other non-standard voltage, by loading the output data as a logic low, then changing the I/O direction of the pin from an output to an input. If the CD pins are used to drive light emitting diodes or opto-couplers, for example, active low outputs can be pulled up to 5 volts by switching the I/O configuration to an input. The leakage current of the I/O input state should be sufficiently small to avoid a soft turn-on. For active

high outputs (sourcing current), the value of the current limiting resistor will need to be changed to provide the same current drive. There are two additional outputs per channel, CD6 and CD7, available on the Le58QL063 device. Because these pins can not be programmed as inputs, it is not possible to pull these pins to 5 volts.

3.0 SUBSCRIBER LINE INTERFACE CIRCUIT CONSIDERATIONS

The full range of the analog output, V_{OUT}, has changed from ±1.584 Vpk for the QSLAC device to ±1.02 Vpk for the QLSLAC device. The range of the analog input, V_{IN}, is the same for both the QSLAC and QLSLAC devices at ±1.584 Vpk with respect to the reference voltage. The analog input range is unchanged in the QLSLAC device because of the addition of an internal attenuator which diminishes the V_{IN} signal by a factor of 0.6436. The attenuator may be disabled which effectively changes the full-scale analog input range to ±1.02 Vpk. Disabling the gain block of the analog input is accomplished by the DGIN bit (bit 7) of the AISN and Analog Gain Register. Whether or not a particular design uses a Zarlink SLIC device or transformer, the 4-to-2 wire gain of the SLIC circuit must be modified by +3.82 dB when converting to the QLSLAC device in order to acheive the same relative receive levels. The 2-to-4 wire gain should remain the same, unless DGIN is selected, in which case it must also be modified by –3.82 dB, in order to maintain the same relative transmit levels.

3.1 Receive Path Gain

In most cases, subscriber line interface circuits that use Zarlink SLIC devices with external components can be readily modified to increase their 4-to-2 wire gain by +3.82 dB by scaling the Z_{RX} impedance by a factor of 1.02/1.584. As an example, consider a design with Zarlink's QSLAC device, an Am7920 SLIC device and a 124 kΩ resistor as its Z_{RX} network in the receive path as shown in Figure 2. When converting the design to a QLSLAC device, the R_{RX} resistor should be changed to approximately 80.6 kΩ in order for the received signal levels to remain nearly unchanged at Tip-Ring. In this case, the value of 80.6 kΩ does not provide the precise scaling, but it is the closest standard E96 component value available to provide the necessary gain. Limiting the Z_{RX} resistance to standard resistor values may introduce a small amount of error into the receive path gain. Using E96 values, the gain error can be kept within 0.1 dB nominal. Using E192 series values, the error will be less than 0.05 dB.

The afore mentioned reference design also has a 0.1µF filtering capacitor, C_{VRX}, in the receive path. If the impedance of the C_{VRX} capacitor becomes significant, with respect to R_{RX}, at low frequencies, the capacitor must be increased to maintain voice performance at the lower end of the voice band. Considering a C_{VRX} of 0.1µF, changing R_{RX} from 124 kΩ to 80.6 kΩ moves the corner frequency from approximately 13 Hz to 20 Hz, which affects the receive path gain by a mere 0.02 dB at 300 Hz. This small error allows C_{VRX} to remain unchanged in this example without adverse consequences. In general, if $1/(2 \bullet \Pi \bullet R_{RX} \bullet C_{VRX}) < 40$ Hz, the DC filter will not significantly impact voice performance at low frequencies. Otherwise the C_{VRX} capacitor should be increased to at least meet the 40 Hz requirement.

SLIC device designs using transformers also require a +3.82 dB increase in the 4-to-2 wire gain. If the QSLAC device/transformer linecard design already uses operational amplifiers to drive the 4-wire side of the transformer, changing the SLIC gain may simply be a matter of modifying the operational amplifier gain. This can be accomplished by changing a resistor value as long as the operational amplifier has sufficient gain-bandwidth product to handle the additional gain. It is important to recognize that while the gain required of the operational amplifier circuit depends on the receive level requirements and the codec output, the actual range of the voltage swing required at the output of the operational amplifiers is independent of the QSLAC and QLSLAC devices. Therefore, if the voltage swing of the operational amplifier circuit is sufficient for the QSLAC device design, it will be sufficient for the QLSLAC device design.

In the case of direct drive transformer designs, it is unlikely that the QLSLAC device would have sufficient voltage swing to meet most requirements without extra gain from the SLIC circuit. Assuming VOUT has sufficient voltage swing and current drive to directly drive the transformer, the filter coefficients could be recomputed to increase the receive path gain from the QSLAC device to the QLSLAC device.

Typically the 4-to-2 wire gain of the SLIC will have to be increased when converting from the QSLAC device to the QLSLAC device. Whether extra gain is needed or not, redesigning the SLIC circuit to

include an extra 3.82 dB of gain in the receive path might avert having to change the SLAC software. The gain could be increased using a single-ended or push-pull operational amplifier design depending on voltage swing requirements. Consult Zarlink's *Transformer Interface Requirements Application Note* (www.zarlink.com; order# 080332) for further details on designing transformer SLICs with Zarlink SLAC devices.

3.2 Transmit Path Gain

Because the full-scale input range of VIN is the same for the QLSLAC and QSLAC devices, the internal attenuator of the QLSLAC device must be enabled (DGIN = 0) to achieve equivalent transmit path gains for the same SLIC design. Alternatively, the attenuator could be disabled by setting the DGIN bit to 1, as long as the two-to-four wire gain (G24) of the SLIC circuitry is adjusted for the QLSLAC design to include the proper attenuation factor. The source impedance from the SLIC must be less than 300 Ω (unless using the Le58QL063 device) in order to avoid potential cross talk issues. If the SLIC has an output attenuator of greater than 300 Ω, an Le58QL063 device must be used. Note that protection diodes to ground and V_{CCA} on the input of VIN could cause clipping of the transmit signal of the QLSLAC device at smaller voltage levels than for the QSLAC device.

Figure 2 provides an example of a design with a QSLAC device and Am7920 device compared to the same design with the QLSLAC device where receive gain is adjusted appropriately by modifying the value of RRX and the transmit gain is modified by using the internal attenuator of the QLSLAC device. Figure 3 shows a similar example comparing a QSLAC device design with the QLSLAC device design using the Am79R79 device for an integrated access device (IAD) application.

Figure 2. Am7920 Device with QSLAC™ Device vs. Am7920 Device with QLSLAC™ Device

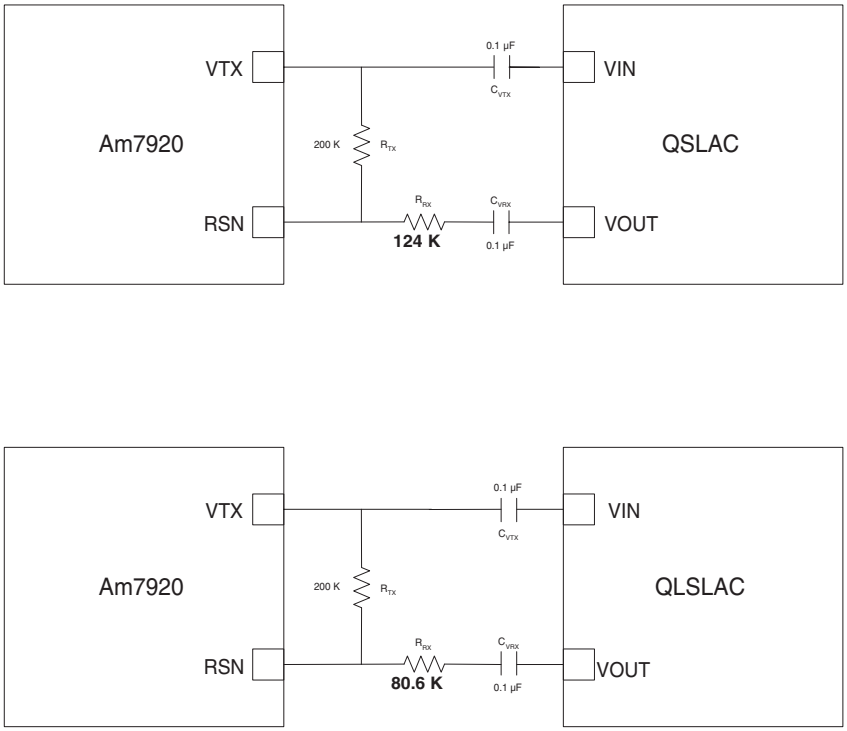
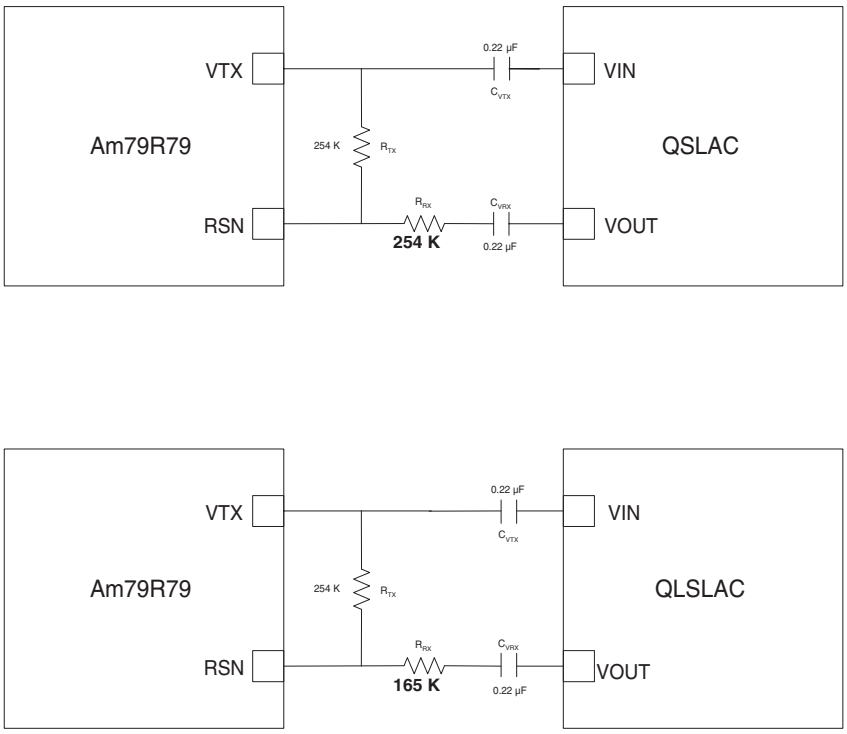


Figure 3. Am79R79 Device with QSLAC™ Device vs. Am79R79 Device with QLSLAC™ Device



Considering a transformer design, the 2-to-4 wire gain may be attenuated with GIN or with an external voltage divider as long as the transmit signal is buffered at the input to the divider. Alternatively, if an operational amplifier circuit is used to detect the transmit path, the gain of the amplifier may be adjusted to achieve the desired signal level at VIN with the internal attenuator disabled (DGIN = 1).

4.0 SLAC COEFFICIENTS

Assuming that the SLIC four-to-two wire gain has been modified by the required amount, all filter coefficients developed for the QSLAC device design may be used directly for the QLSLAC device design. As long as the DGIN bit in the AISN and Analog Gain Register (write/read command 50/51h) is set to “0” in the QSLAC device firmware, no software changes are required for conversion to the QLSLAC chip. System level performance, including transmit and receive levels and return losses should be approximately the same for each design. If the recommended SLIC modifications can not be made, new software coefficients will have to be developed.

Constraints on standard resistor values can have an affect on performance. Figure 4 shows WinSLAC™ performance predictions for the QSLAC chip reference design compared with the performance of the QLSLAC chip design using the Am7920 SLIC device and external components as shown in Figure 2. Similarly, Figure 5 shows WinSLAC™ performance predictions for the QSLAC chip reference design compared with the performance of the QLSLAC chip design using the Am79R79 SLIC device and external components as shown in Figure 3. The graphs shows predicted 2-wire and 4-wire return loss magnitudes over frequency, as well as receive and transmit attenuation distortion. Green circles represent predicted values for the QSLAC device, while red triangles represent predicted values for the QLSLAC device.

Performance differences, particularly apparent in the four wire return loss, are due to errors in the transmit and receive gains as a result of choosing a standard R_{RX} resistor value. The receive and transmit attenuation distortion curves overlay almost exactly, making the two curves indistinguishable. From Figure 4 it is seen that the receive level decreased by 0.159 dB, while the transmit level is reduced by 0.133 dB. Overall, simulations indicate that performance can be largely maintained by using the same filter coefficients if Z_{RX} is properly selected. The WinSLAC software, which can be ordered from the Zarlink website at www.zarlnk.com, can be used to verify that the gain adjustments are correct, as demonstrated in these examples. A supplemental applications note discussing how to use WinSLAC revision 1.2d to recreate these simulations is also available.[7]

Figure 4. WinSLAC™ Performance Comparison: QSLAC™ and QLSLAC™ Devices with the Am7920 Device

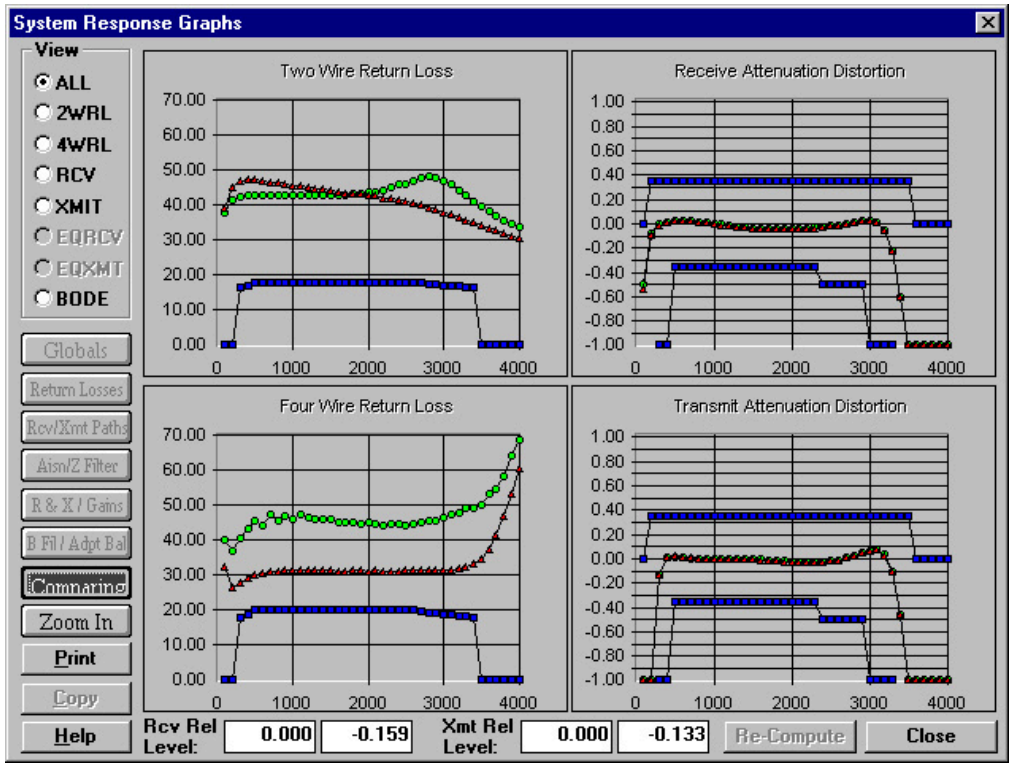
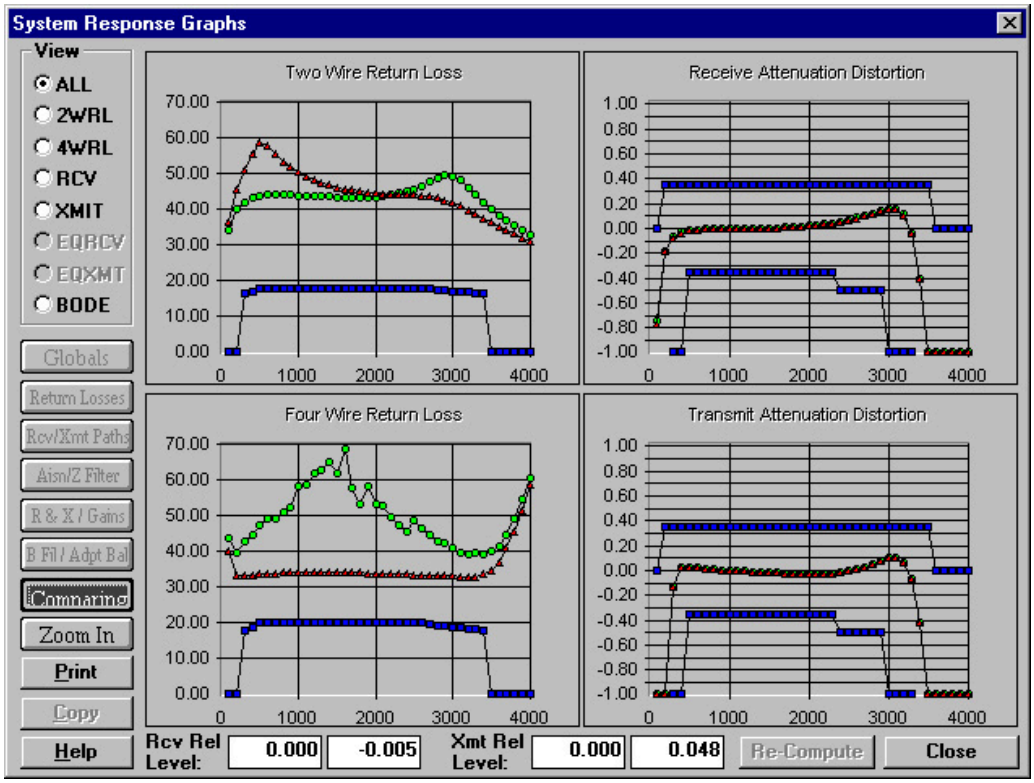


Figure 5. WinSLAC™ Performance Comparison: QSLAC™ and QLSLAC™ Devices with the Am79R79 Device



5.0 COMPARATIVE TRANSMISSION PERFORMANCE

Device and system level testing indicate that the QSLAC and QLSLAC devices exhibit nearly identical performance. Using the example designs of figures 2 and 3, it is possible to directly compare the performance of a QSLAC design verses a QLSLAC design with the same set of filter coefficients. Using the WinSLAC software tools, filter coefficients were determined for a QSLAC/Am7920 design with a 600 Ω terminating impedance. With the coefficients loaded into the QSLAC, various system level transmission measurements were performed. Similar measurements were taken for the QLSLAC/ Am7920 design by making the necessary hardware changes while using the same filter coefficients, the same Am7920 device, and the same terminating load.

Figure 6 contains plots showing measured transmission performance data for the QSLAC and QLSLAC devices with an Am7920 SLIC device. The measurements, which include two wire and four wire return loss and attenuation distortion in both the receive and transmit directions, were taken with Wandel and Goltermann's PCM-4 test equipment and a 600 Ω load. Green circles represent data taken for the QSLAC device design, while the red "x" symbols represent data taken for the QLSLAC device design. Figure 7 and Figure 8 show comparisons of gain tracking and signal to distortion measurements respectively for the same QSLAC and QLSLAC device designs with an Am7920 chip.

Figure 6. Transmission Performance with Am7920 SLIC Device

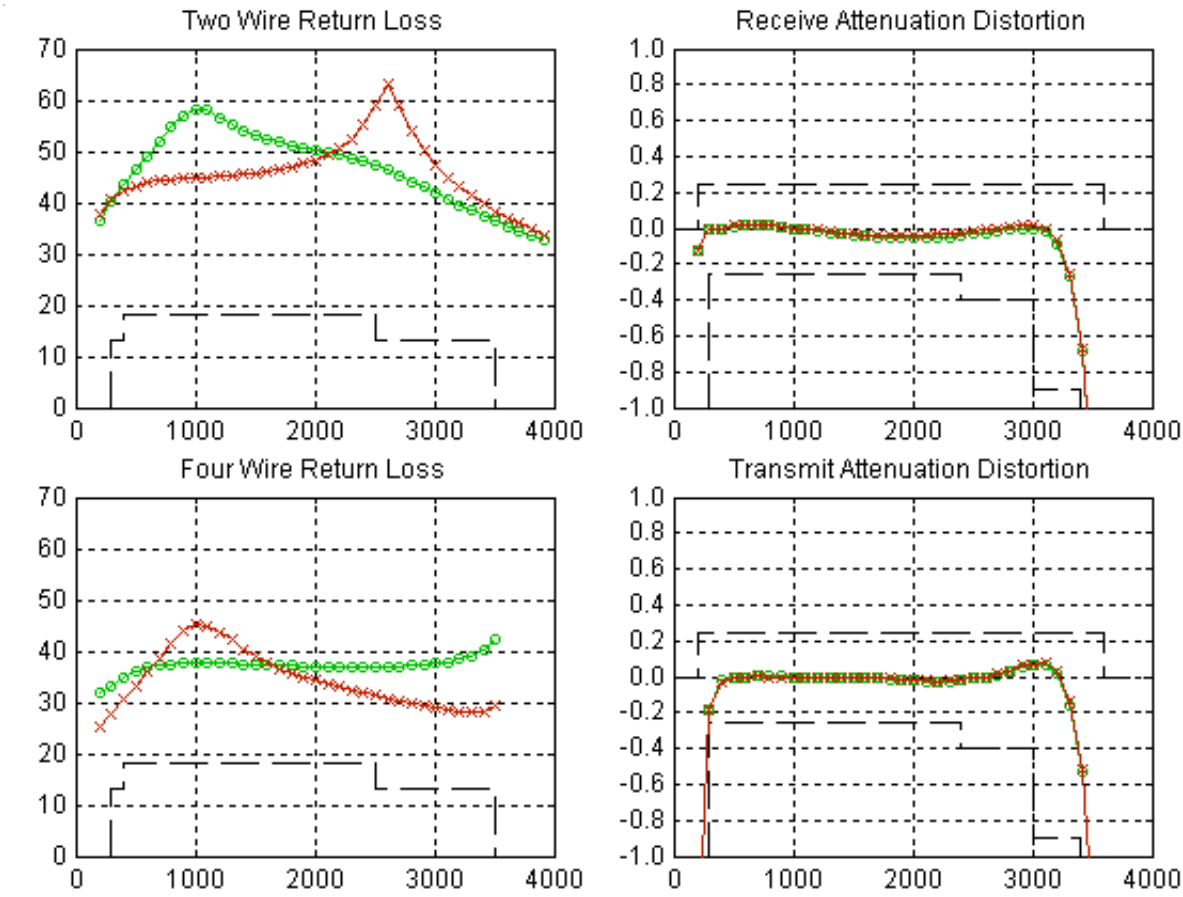


Figure 7. Gain Tracking with Am7920 SLIC Device

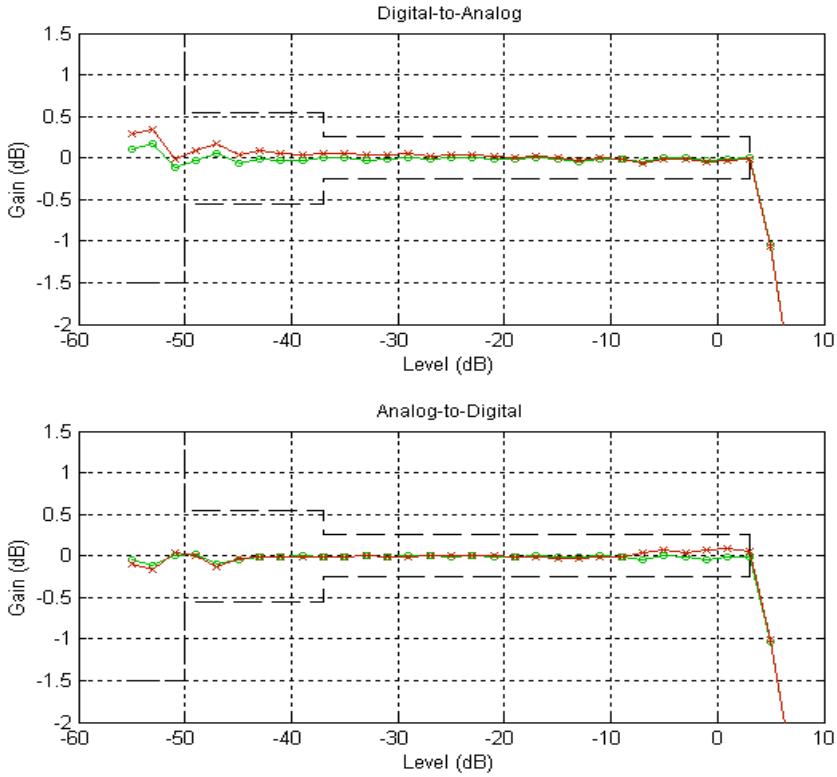


Figure 8. Signal-to-Distortion with Am7920 SLIC Device

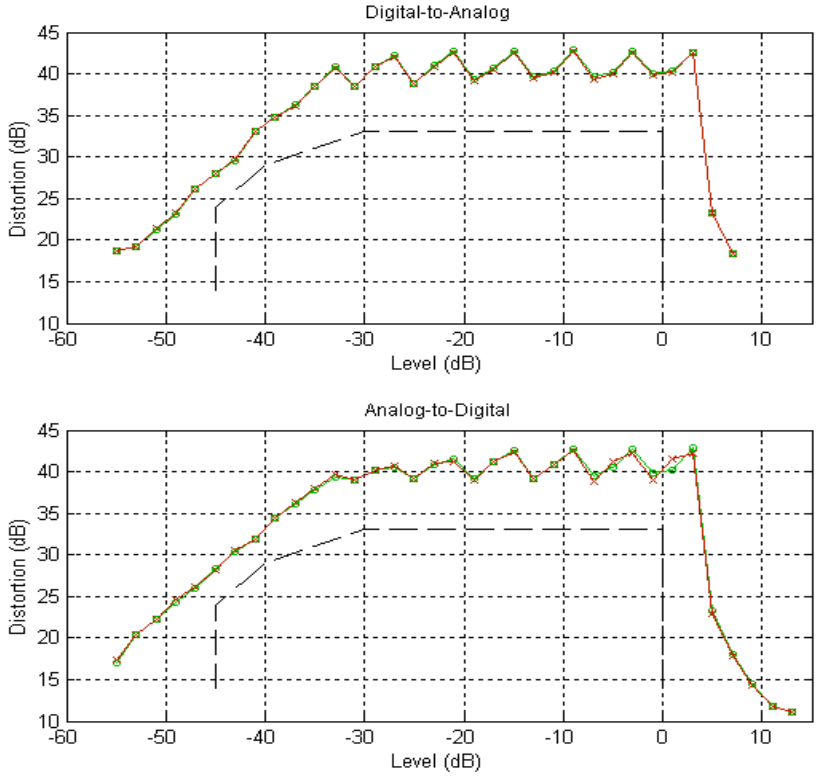


Figure 9 contains transmission plot comparisons for the QSLAC/QLSLAC device designs with an Am79R79 SLIC device, while Figure 10 and Figure 11 compare gain tracking and signal to distortion measurements for an Am79R79 system respectively.

From the plots, it is clear that all the system level transmission measurements meet the template requirements. There are some differences in the two-wire and four wire return losses, however such difference are within the normally expected variances of the device. For the most part, the two-wire return loss achieves similar levels for both the QSLAC and QLSLAC designs. The four-wire return loss performance suffers from receive gain errors introduced by selection of standard resistor components for R_{RX}; however the performance is still greater than 25dB for QLSLAC designs without recomputing filter coefficients. In addition, gain tracking and signal-to-distortion measurements appear to be almost identical for systems using the QSLAC device and QLSLAC device.

Figure 9. Transmission Performance with Am79R79 SLIC Device

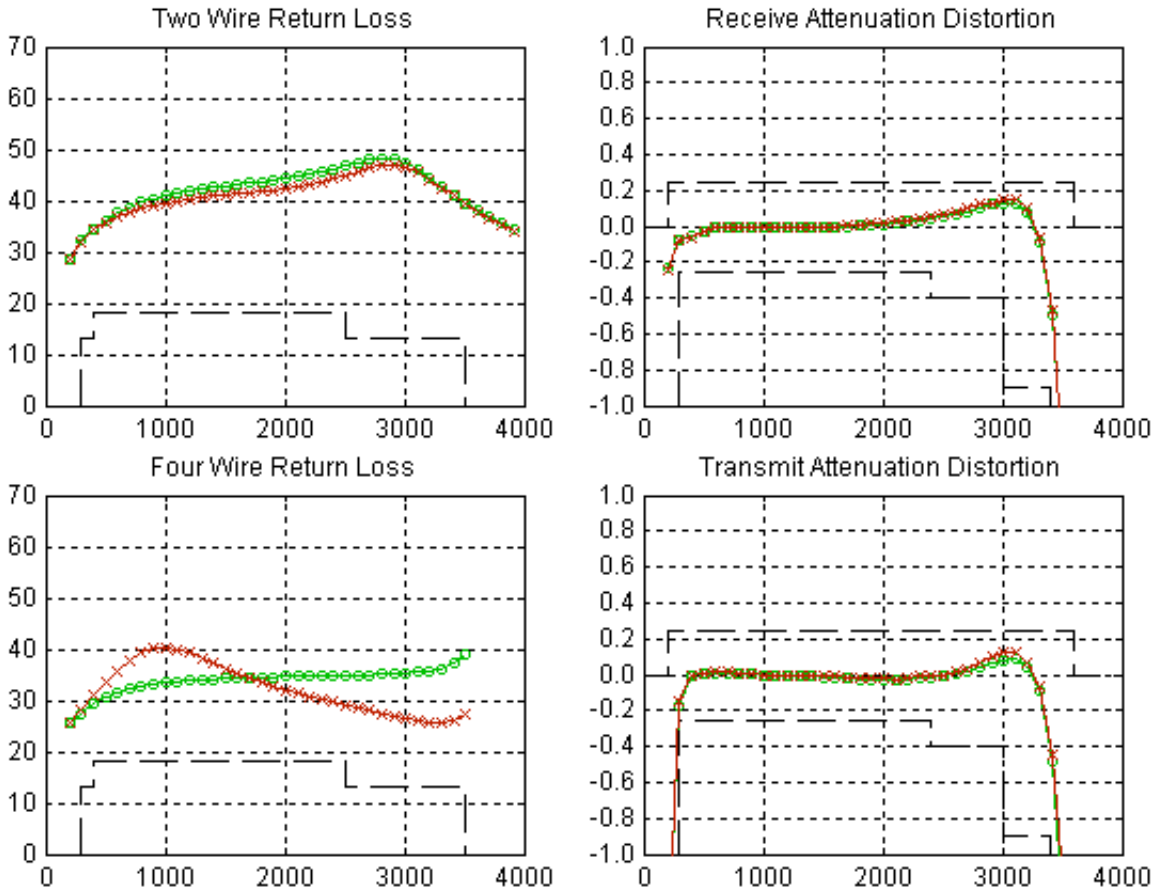


Figure 10. Gain Tracking with Am79R79 SLIC Device

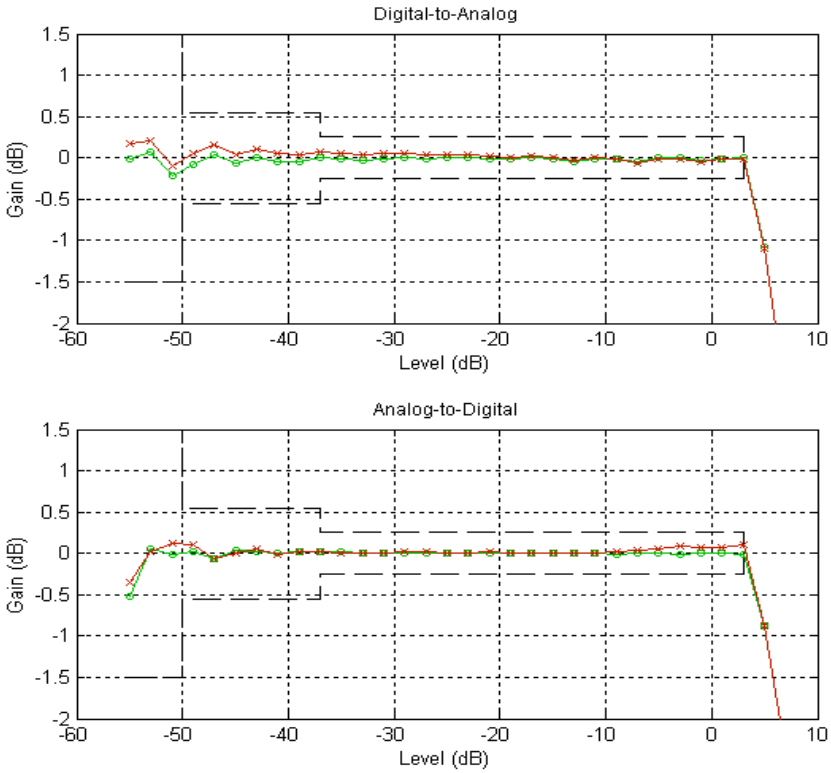
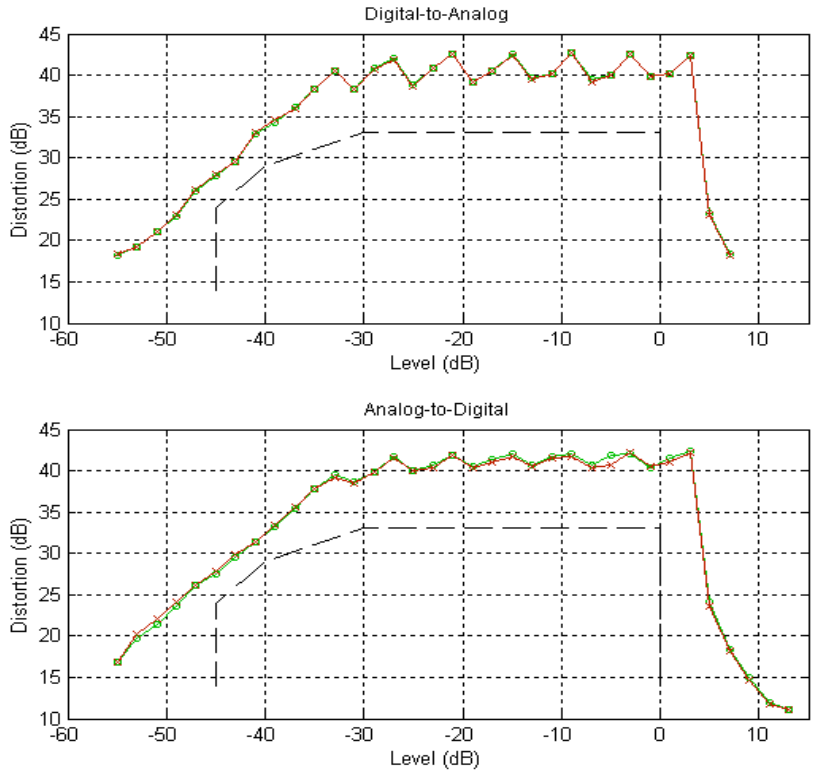


Figure 11. Signal-to-Distortion with Am79R79 SLIC Device



6.0 CONCLUSION

The QLSLAC device performance is equivalent to the QSLAC device with the added benefit of lower power dissipation. This lower voltage device requires only modest layout and component changes for conversion from a QSLAC design. Such changes are straightforward, cost competitive, and allow new QLSLAC device designs to realize complete software compatibility with existing QSLAC designs.

ADDITIONAL REFERENCES

1. *Le58QL02/021/031 QLSLAC™ Data Sheet, Revision A2*, PID# 080753, January, 2002, http://www.zarlink.com.
2. *Le58QL061/063 QLSLAC™ Data Sheet, Revision B1*, PID# 080754, January, 2002, http://www.zarlink.com.
3. *Am79Q02/021/031 QSLAC™ Data Sheet*, PID# 080147, December 2001, http://www.zarlink.com.
4. *Am79Q061/063 QSLAC™ Data Sheet*, PID# 080193, December, 2001, http://www.zarlink.com.
5. *WinSLAC Software User's Guide*, PID# 080628, June, 1999, http://www.zarlink.com.
6. *Transformer SLIC Device Interface Requirements for Zarlink SLAC™ Coded/Filter Devices Application Note*, PID# 080332, October, 2001, http://www.zarlink.com.
7. *Guide to WinSLAC Software Simulations, Comparing Transmission Performance of Designs Using QLSLAC Devices vs. QSLAC Devices Applications Note*, PID# 080722, January, 2002, http://www.zarlink.com.

REVISION HISTORY

Revision A1 to B1

- Added system performance comparisons for the QSLAC and QLSLAC design examples

Revision B1 to C1

- Added information regarding internal attenuator and removed references to external attenuator
- Added information about SLIC control/data pins when pulling up to 5 volts
- Edited "Conclusion" section
- Updated "Additional References" section

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