19-5144; Rev 0; 2/10

可提供评估板

1.0625Gbps至11.3Gbps、SFP+双通道限幅放大器

MAX3945

概述

MAX3945多速率、低功耗限幅放大器采用+3.3V电源供电，优化用于光纤通道以及以太网发送系统，数据速率高达11.3Gbps。高灵敏度限幅放大器对互阻放大器产生的信号进行限幅，产生CML电平差分输出信号。所有差分输入和输出(I/O)都优化于50Ω背向端接PCB传输线。MAX3945双通道限幅放大器带有可编程滤波器，能够针对不同数据速率下的敏感度进行优化，抑制光学系统可能产生的驰豫振荡。MAX3945集成了两路信号丢失(LOS)检测电路和一个可编程时间屏蔽的LOS输出。

3线数字接口减少了引脚数，无需外部器件即可实现LOS门限、LOS极性、LOS模式、CML输出电平、输入失调修正、接收(Rx)极性、Rx输入滤波器以及Rx去加重的控制。

MAX3945采用3mm x 3mm、16引脚TQFN封装。

应用

1x/2x/4x/8x SFF/SFP/SFP+ MSA光纤通道光收发器

10GBASE-SR/LR SFP+光收发器

10G PON ONU

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX3945ETE+	-40°C to +85°C	16 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。

**EP = 裸焊盘。*

典型应用电路在数据资料的最后给出。

特性

- 130mW功耗支持低于1W的SFP+模块设计
- 单模块设计兼容于1000BASE-SX/LX和10GBASE-SR/LR标准
- 采用10.32Gbps ROSA，在1.25Gbps下光信号检测灵敏度为-25.3dBm
- RATE_SEL = 0时，可选择1GHz/2.1GHz/2.5GHz/3GHz输入滤波器
- 支持SFF-8431 SFP+ MSA和SFF-8472数字诊断
- 3.3V供电并提供基于RSSI监测的LOS功能时，总功耗为130mW
- 3.3V供电并提供基于Rx输入的LOS功能时，总功耗为154mW
- 11.3Gbps速率下具有4mV$_{P-P}$输入灵敏度
- RATE_SEL = 1、11.3Gbps速率下具有4ps$_{P-P}$ DJ
- RATE_SEL = 1、8.5Gbps速率下具有4ps$_{P-P}$ DJ
- RATE_SEL = 0、BW1 = 1、BW0 = 1、4.25Gbps速率下具有5ps$_{P-P}$ DJ
- RATE_SEL = 0、BW1 = 0、BW0 = 0、1.25Gbps速率下具有9.0ps$_{P-P}$ DJ
- RATE_SEL = 1时，具有26ps上升和下降时间
- RATE_SEL = 0时，具有52ps上升和下降时间
- CML输出具有电平调节和禁止模式
- 可编程CML输出去加重
- CML输出极性选择
- LOS极性选择
- LOS输出带有可编程屏蔽时间
- 可调节LOS触发/清除电平
- 可选择基于Rx输入的LOS或基于RSSI监测的LOS
- 3线数字接口与Maxim SFP+系列产品兼容

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +4.0V
Voltage Range at SDA, SCL, CSEL, LOS, CAZ, RPMIN ..... -0.3V to (V_{CC} + 0.3V)
Voltage Range at ROUT+, ROUT- ..... (V_{CC} - 2V) to (V_{CC} + 0.3V)
Voltage Range at RIN+, RIN- ..... (V_{CC} - 1.7V) to (V_{CC} + 0.3V)
Current Range Into LOS ..... -1mA to +5mA
Current Range Into SDA ..... -1mA to +1mA
Current Out of ROUT+, ROUT- 40mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 14.7mW/°C above +70°C) 1.176W
Operating Junction Temperature Range ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Current	I_{CC}	Includes the CML output current, V_{DIFF_ROUT} = 400mV_{P-P}, RXDE_EN = 0, LOS1_EN = 1, LOS2_EN = 0		46.6	62	mA
		Includes the CML output current, V_{DIFF_ROUT} = 400mV_{P-P}, RXDE_EN = 0, LOS1_EN = 0, LOS2_EN = 1		39.4	52.5	
Power-Supply Voltage	V_{CC}		2.85		3.63	V
Power-Supply Noise		f < 10MHz			100	mV_{P-P}
		10MHz < f < 20MHz			10	
GENERAL						
Input Data Rate			1.06	10.32	11.3	Gbps
Input/Output SNR			14.1			
BER					10E-12	
POWER-ON RESET (POR)						
POR Deassert Threshold				2.55	2.75	V
POR Assert Threshold			2.3	2.45		V
INPUT SPECIFICATIONS						
Differential Input Resistance RIN+/RIN-	R_{IN_DIFF}		75	100	125	Ω
Input Sensitivity (Note 1)	V_{INMIN}	RATE_SEL = 1, input transition time 25ps, 10.32Gbps, PRBS23-1 pattern		4	8	mV_{P-P}
		RATE_SEL = 0, input transition time 260ps, 1.25Gbps, K28.5 pattern		1	2	
Input Overload	V_{INMAX}		1.2			V_{P-P}
Input Return Loss	SDD11	DUT is powered on, f ≤ 5GHz		10		dB
		DUT is powered on, f ≤ 16GHz		7		
	SCC11	DUT is powered on, 1GHz < f ≤ 5GHz		13		dB
		DUT is powered on, 1GHz < f ≤ 16GHz		5		
RPMIN Input-Current High	I_{IH}	LOS1_EN = 0 and LOS2_EN = 1, V_{RPMIN} = 2V		50		nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External RPMIN Filter Capacitor			100			pF
OUTPUT SPECIFICATIONS						
Differential Output Resistance ROUT+/ROUT-	$R_{OUTDIFF}$		75	100	125	Ω
Output Return Loss	SDD22	DUT is powered on, f ≤ 5GHz		13		dB
		DUT is powered on, f ≤ 16GHz		7		
	SCC22	DUT is powered on, 1GHz < f ≤ 5GHz		10		
		DUT is powered on, 1GHz < f ≤ 16GHz		6		
Differential Output-Voltage High		$5mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, RATE_SEL = 0, SET_CML[7:0] = 169d (decimal)	595	800	1005	mV_{P-P}
		$10mV_{P-P} \le V_{IN} \le 1200mV$, RATE_SEL = 1, SET_CML[7:0] = 181d	595	800	1005	
Differential Output-Voltage Medium		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$, RATE_SEL = 1, SET_CML[7:0] = 91d	300	400	515	mV_{P-P}
SET_CML DAC Range			60		255	Decimal
Differential Output Signal When Squelched (Note 1)		Outputs AC-coupled, SET_CML[7:0] = 181d, at 8.5Gbps, SQ_EN = 1		6	15	mV_{P-P}
Data Output Transition Time (20% to 80%) (Note 1)	t_R/t_F	$60mV_{P-P} \le V_{IN} \le 400mV_{P-P}$ at 10.32Gbps, RATE_SEL = 1, $V_{DIFF\_ROUT} = 400mV_{P-P}$, RXDE_EN = 0, input transition time 25ps, pattern 11110000		26	35	ps
		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 1.25Gbps, RATE_SEL = 0, $V_{DIFF\_ROUT} = 800mV_{P-P}$, input transition time 260ps, pattern 11110000		52	90	
TRANSFER CHARACTERISTICS						
Deterministic Jitter (Notes 1, 2)	DJ	$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 8.5Gbps, RATE_SEL = 1, $V_{DIFF\_ROUT} = 400mV_{P-P}$, RXDE_EN = 0, input transition time 28ps		4	8	ps_{P-P}
		$60mV_{P-P} \le V_{IN} \le 400mV_{P-P}$ at 10.32Gbps, RATE_SEL = 1, $V_{DIFF\_ROUT} = 400mV_{P-P}$, RXDE_EN = 0, input transition time 28ps		4	9	
		$60mV_{P-P} \le V_{IN} \le 400mV_{P-P}$ at 11.3Gbps, RATE_SEL = 1, $V_{DIFF\_ROUT} = 400mV_{P-P}$, RXDE_EN = 0, input transition time 28ps		4	9	
		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 1.25Gbps, RATE_SEL = 0, BW1 = 0, BW0 = 0, $V_{DIFF\_ROUT} = 800mV_{P-P}$, input transition time 260ps		9	30	
		$10mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$ at 4.25Gbps, RATE_SEL = 0, BW1 = 1, BW0 = 1, $V_{DIFF\_ROUT} = 800mV_{P-P}$, input transition time 28ps		5	10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Random Jitter (Note 1)	RJ	Input = 60mV$_{P-P}$ at 10.32Gbps, RATE_SEL = 1, RXDE_EN = 0, input transition time 28ps, pattern 11110000, V_{DIFF_ROUT} = 800mV$_{P-P}$		0.28	0.51	ps$_{RMS}$
Low-Frequency Cutoff (Simulated Value)		RATE_SEL = 0, C_{CAZ} = 0.1µF		2		kHz
		RATE_SEL = 1, C_{CAZ} = 0.1µF		0.7		
Small-Signal Bandwidth (Simulated Value)	f_{3dB}	RATE_SEL = 0, BW1 = 0, BW0 = 0		1.0		GHz
		RATE_SEL = 0, BW1 = 0, BW0 = 1		2.1		
		RATE_SEL = 0, BW1 = 1, BW0 = 0		2.5		
		RATE_SEL = 0, BW1 = 1, BW0 = 1		3.0		
		RATE_SEL = 1		9		
Rx INPUT-BASED LOS SPECIFICATIONS (LOS1_EN = 1 and LOS2_EN = 0) (Note 1)						
LOS Assert Sensitivity Range		(Note 3)	14		77	mV$_{P-P}$
SET_LOS DAC Range			7		63	Decimal
LOS Hysteresis		10log($V_{DEASSERT}$/V_{ASSERT})	1.25	2.1		dB
LOS Assert/Deassert Time		(Note 4)	2.3	20	80	µs
Low Assert Level		SET_LOS[5:0] = 7d (Note 3)	8	11	14	mV$_{P-P}$
Low Deassert Level			14	18	22	
Medium Assert Level		SET_LOS[5:0] = 32d (Note 3)	39	49	58	mV$_{P-P}$
Medium Deassert Level			65	82	95	
High Assert Level		SET_LOS[5:0] = 63d (Note 3)	77	96	112	mV$_{P-P}$
High Deassert Level			127	158	182	
LOS Output Masking Time Range		SET_LOSTIMER[6:0] = 0d for minimum and SET_LOSTIMER[6:0] = 127d for maximum	0		2920	µs
LOS Output Masking DAC Resolution		SET_LOSTIMER[6:0] = 1d to 127d	23	35	50	µs
RSSI MONITOR-BASED LOS SPECIFICATIONS (LOS1_EN = 0 and LOS2_EN = 1) (Note 1)						
LOS Assert Sensitivity Range		(Note 5)	8.3		90	mV
SET_LOS DAC Range			4		63	Decimal
LOS Hysteresis		10log($V_{DEASSERT}$/V_{ASSERT})	1.25	2.1		dB
LOS Assert/Deassert Time		(Note 4)	2.3	20	80	µs
Low Assert Level		SET_LOS[5:0] = 4d (Note 5)	5.1	6.7	8.3	mV
Low Deassert Level			9.0	10.8	12.7	
Medium Assert Level		SET_LOS[5:0] = 32d (Note 5)	45	50	55	mV
Medium Deassert Level			77	85	92	
High Assert Level		SET_LOS[5:0] = 63d (Note 5)	90	98	106	mV
High Deassert Level			153	167	180	
LOS Output Masking Time Range		SET_LOSTIMER[6:0] = 0d for minimum and SET_LOSTIMER[6:0] = 127d for maximum	0		2920	µs
LOS Output Masking DAC Resolution		SET_LOSTIMER[6:0] = 1d to 127d	23	35	50	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT LEVEL VOLTAGE DAC (SET_CML)						
Full-Scale Voltage	V_{FS}	100Ω differential resistive load, RXDE_EN = 0		1192		mV_{P-P}
		100Ω differential resistive load, RATE_SEL = 1, RXDE_EN = 1, RXDE1 = 1, RXDE0 = 1 (maximum deemphasis)		828		
Resolution		100Ω differential resistive load, RXDE_EN = 0		4.5		mV_{P-P}
		100Ω differential resistive load, RATE_SEL = 1, RXDE_EN = 1, RXDE1 = 1, RXDE0 = 1 (maximum deemphasis)		3.3		
Integral Nonlinearity	INL	SET_CML[7:0] > 60d		±0.9		LSB
LOS THRESHOLD VOLTAGE DAC (SET_LOS)						
Full-Scale Voltage	V_{FS}	LOS1_EN = 1, LOS2_EN = 0		96		mV_{P-P}
		LOS1_EN = 0, LOS2_EN = 1		98		mV
Resolution		LOS1_EN = 1, LOS2_EN = 0		1.52		mV_{P-P}
		LOS1_EN = 0, LOS2_EN = 1		1.56		mV
Integral Nonlinearity	INL	SET_LOS[5:0] > 3d		±0.7		LSB
CONTROL I/O SPECIFICATIONS						
LOS Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ to 10kΩ to V_{CC}	V_{CC} - 0.5		V_{CC}	V
LOS Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ to 10kΩ to V_{CC}	0		0.4	V
3-WIRE DIGITAL I/O SPECIFICATIONS (SDA, CSEL, SCL)						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}			0.082		V
Input Leakage Current	$I_{IL,IH}$	V_{IN} = 0V or V_{CC}, internal pullup or pulldown (75kΩ typ)			85	µA
Output High Voltage	V_{OH}	External pullup of 4.7kΩ to V_{CC}	V_{CC} - 0.5		V_{CC}	V
Output Low Voltage	V_{OL}	External pullup of 4.7kΩ to V_{CC}	0		0.4	V
3-WIRE DIGITAL INTERFACE TIMING CHARACTERISTICS (see Figure 5)						
SCL Clock Frequency	f_{SCL}		0	400	1000	kHz
SCL Pulse-Width High	t_{CH}		500			ns
SCL Pulse-Width Low	t_{CL}		500			ns
SDA Setup Time	t_{DS}			100		ns
SDA Hold Time	t_{DH}			100		ns
SCL Rise to SDA Propagation Time	t_D			5		ns
CSEL Pulse-Width Low	t_{CSW}		500			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.85V to 3.63V, CML receiver output is AC-coupled to differential 100Ω load, C_{CAZ} = 0.1µF, T_A = -40°C to +85°C. Registers are set to default values, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSEL Leading Time Before the First SCL Edge	t_L			500		ns
CSEL Trailing Time After the Last SCL Edge	t_T			500		ns
SDA, SCL External Load	C_B	Total bus capacitance on one line with 4.7kΩ to V_{CC}			20	pF

Note 1: Guaranteed by design and characterization, T_A = -40°C to +95°C.

Note 2: Deterministic jitter is measured with a repeating K28.5 pattern [00111110101100000101] for 1.25Gbps to 8.5Gbps data. At 10.32Gbps and 11.3Gbps, a repeating K28.5 plus 59 0s and K28.5 plus 59 1s pattern is used. Deterministic jitter is defined as the arithmetic sum of pulse-width distortion (PWD) and pattern-dependent jitter (PDJ).

Note 3: LOS1_EN = 1, data rates of 1.25Gbps to 8.5Gbps with K28.5 pattern, and 6.4GHz input filter. For data rates of 10.32Gbps to 11.3Gbps, the input filter is 12.5GHz and the pattern is PRBS23-1.

Note 4: Measurement includes an input AC-coupling capacitor of 100nF and C_{CAZ} of 100nF. The signal at the RIN or RPMIN input is switched between two amplitudes: Signal_ON and Signal_OFF.

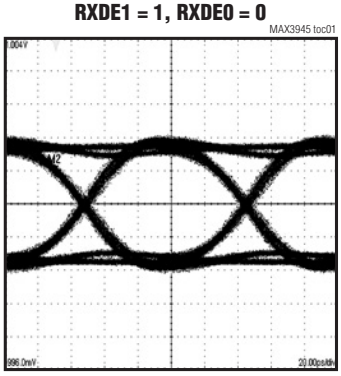
1) Receiver operates at sensitivity level plus 1dB power penalty
   a) Signal_OFF = 0
      Signal_ON = (+8dB) + 10log(min_assert_level)
   b) Signal_ON = (+1dB) + 10log(max_deassert_level)
      Signal_OFF = 0
2) Receiver operates at overload
   Signal_OFF = 0
   Signal_ON = $1.2V_{P-P}$
   max_deassert_level and min_assert_level are measured for one SET_LOS setting

Note 5: LOS1_EN = 0, LOS2_EN = 1, DC voltage applied to the RPMIN input.

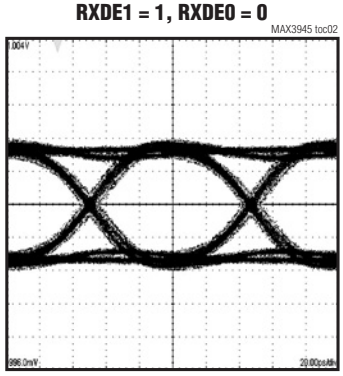
典型工作特性

(VCC = 3.3V, TA = +25°C, unless otherwise noted. Registers are set to default values, unless otherwise noted, and the 3-wire interface is static during measurements.)

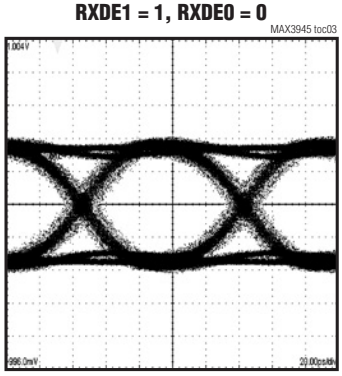
RECEIVE OUTPUT FROM OPTICAL SYSTEM, 10.32Gbps, OPTICAL INPUT -10dBm, RXDE1 = 1, RXDE0 = 0



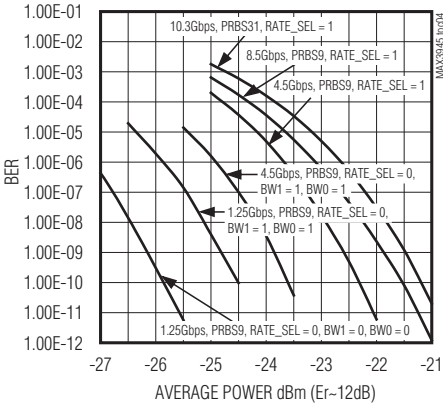
RECEIVE OUTPUT FROM OPTICAL SYSTEM, 10.32Gbps, OPTICAL INPUT -15dBm, RXDE1 = 1, RXDE0 = 0



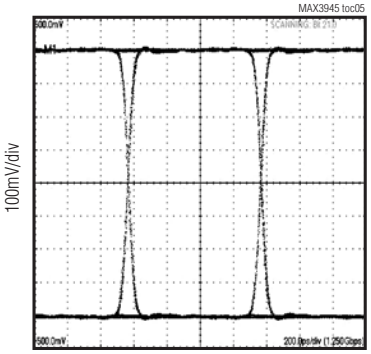
RECEIVE OUTPUT FROM OPTICAL SYSTEM, 10.32Gbps, OPTICAL INPUT -20dBm, RXDE1 = 1, RXDE0 = 0



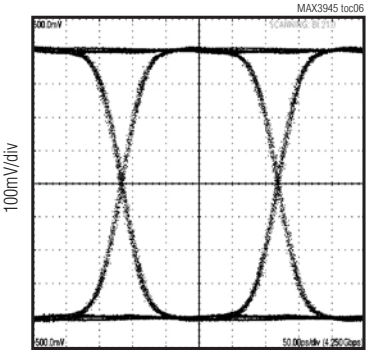
OPTICAL BER CURVES (NEC NR3312)



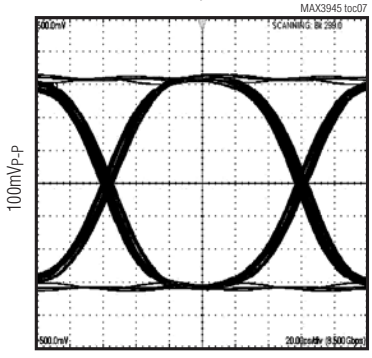
K28.5 PATTERN AT 1.25Gbps, SET_CML[7:0] = 169d, RATE_SEL = 0, BW0 = 0, BW1 = 0



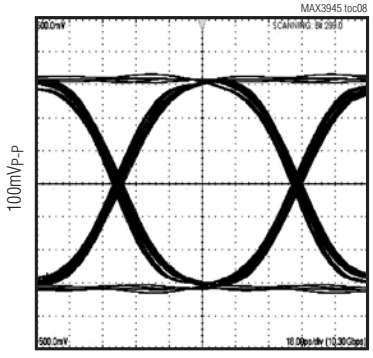
K28.5 PATTERN AT 4.25Gbps, SET_CML[7:0] = 169d, RATE_SEL = 0, BW0 = 1, BW1 = 1



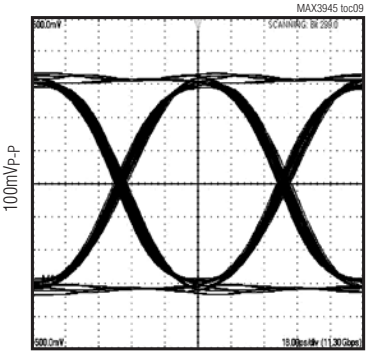
K28.5 PATTERN AT 8.5Gbps, SET_CML[7:0] = 148d, RATE_SEL = 1, RXDE_EN = 0



K28.5 PATTERN AT 10.3Gbps, SET_CML[7:0] = 148d, RATE_SEL = 1, RXDE_EN = 0



K28.5 PATTERN AT 11.3Gbps, SET_CML[7:0] = 148d, RATE_SEL = 1, RXDE_EN = 0

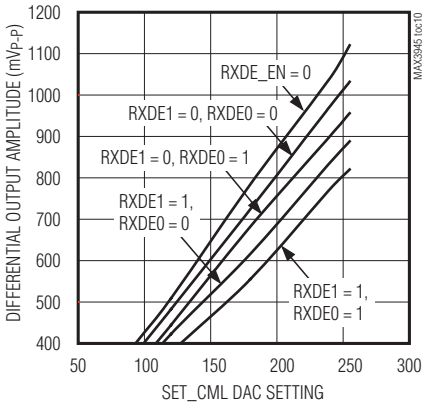


1.0625Gbps至11.3Gbps、SFP+双通道限幅放大器

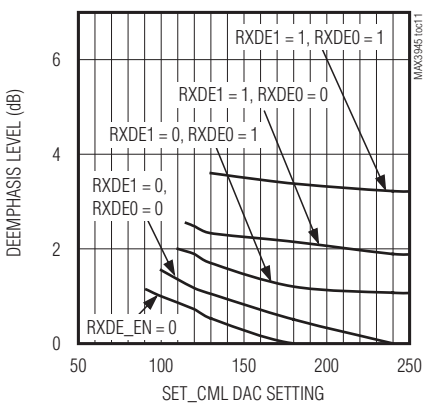
典型工作特性(续)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted. Registers are set to default values, unless otherwise noted, and the 3-wire interface is static during measurements.)

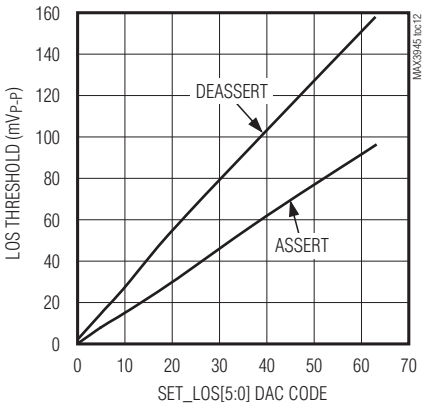
DIFFERENTIAL OUTPUT SIGNAL LEVEL vs. SET_CML DAC SETTING



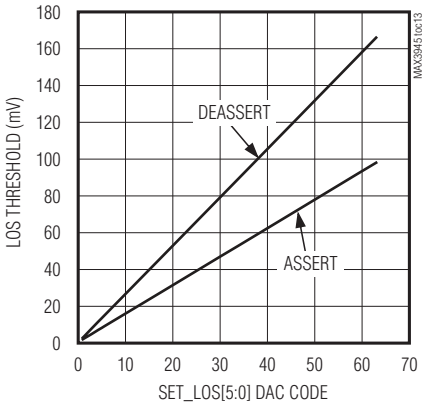
DEEMPHASIS VALUE vs. SET_CML DAC SETTING (RATE_SEL = 1)



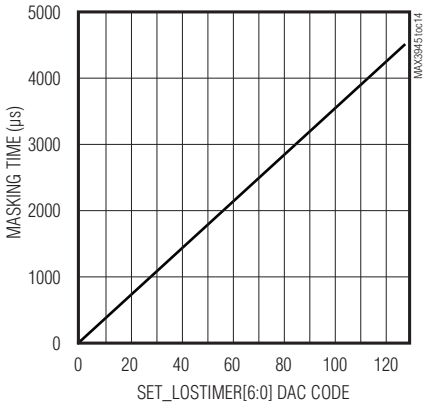
Rx INPUT-BASED LOS THRESHOLD vs. DAC CODE (LOS1_EN = 1 AND LOS2_EN = 0)



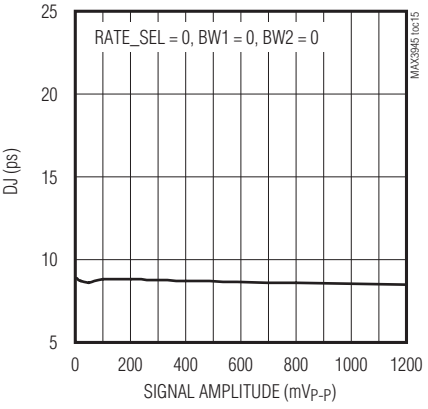
RSSI MONITOR-BASED LOS THRESHOLDS (LOS1_EN = 0 AND LOS2_EN = 1)



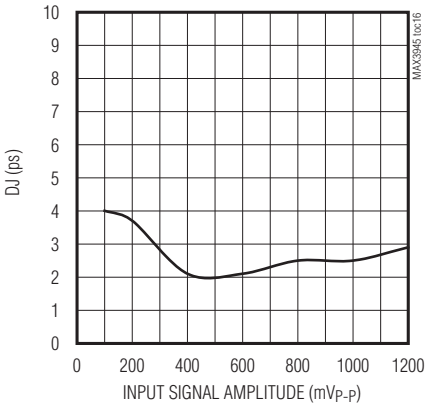
LOS MASKING TIME vs. DAC SETTING



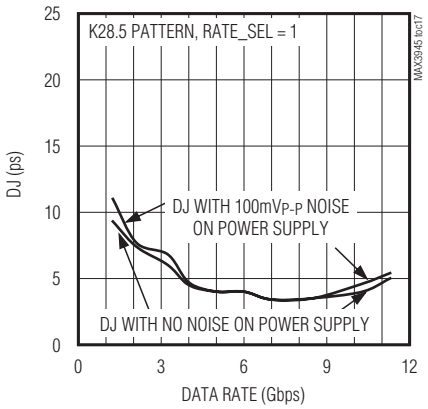
DETERMINISTIC JITTER vs. INPUT AMPLITUDE AT 1.25Gbps (K28.5 PATTERN, 933MHz INPUT FILTER)



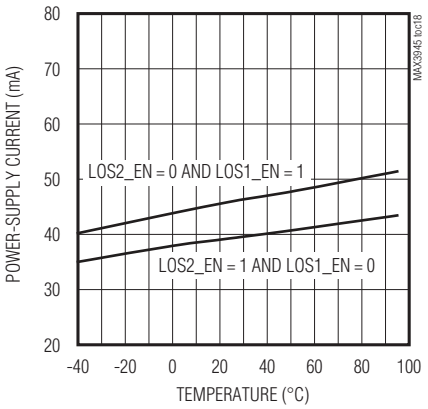
DETERMINISTIC JITTER AT 10.32Gbps (PRBS7 PATTERN WITH 100 CIDs, RATE_SEL = 1)



DETERMINISTIC JITTER vs. DATA RATE (INPUT = 100mVP-P)



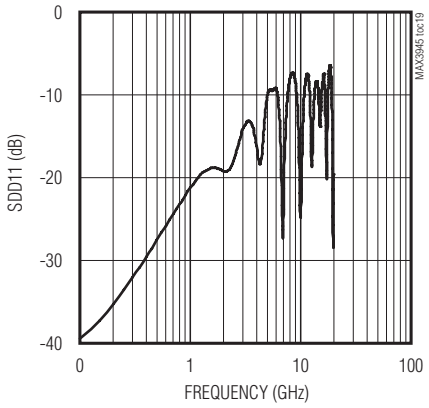
POWER-SUPPLY CURRENT vs. TEMPERATURE (SET_CML[7:0] = 91d)



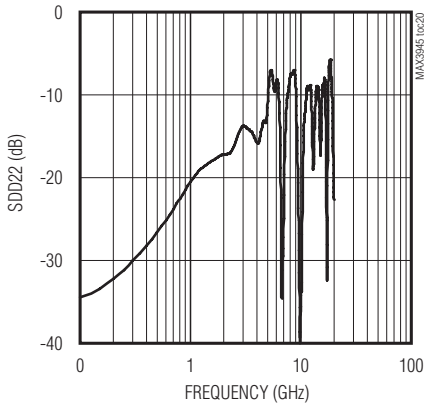
典型工作特性(续)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted. Registers are set to default values, unless otherwise noted, and the 3-wire interface is static during measurements.)

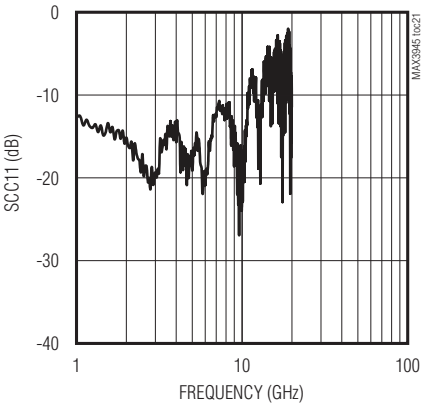
**INPUT RETURN GAIN (SDD11)
(INPUT POWER OF 0dBm, ENABLED)**



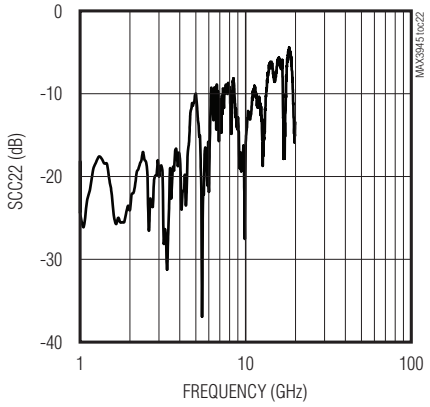
**OUTPUT RETURN GAIN (SDD22)
(INPUT POWER OF 0dBm, ENABLED)**



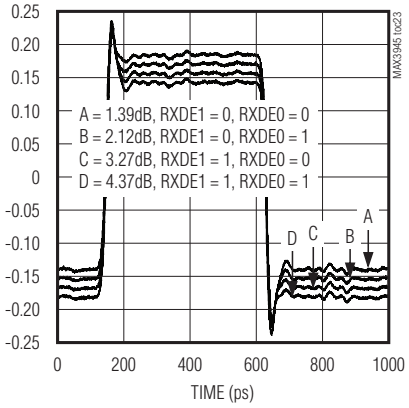
**INPUT COMMON-MODE RETURN GAIN (SCC11)
(INPUT POWER OF 0dBm, ENABLED)**



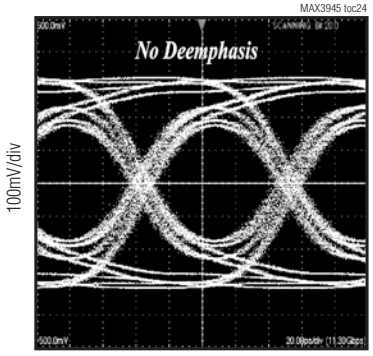
**OUTPUT COMMON-MODE RETURN GAIN (SCC22)
(INPUT POWER OF 0dBm, ENABLED)**



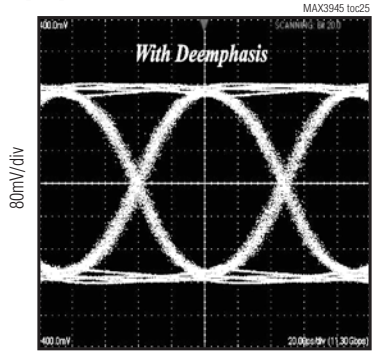
**TRANSIENT RESPONSE (10.3Gbps,
10 ONES 10 ZEROS PATTERN, SET_CML[7:0] = 92d)**



**ELECTRICAL EYE DIAGRAM AFTER 6in OF FR4
AND 72in OF CABLE WITH NO DEEMPHASIS (11.3Gbps K28.5,
RATE_SEL = 1, SET_CML[7:0] = 160d, RXDE_EN = 0)**

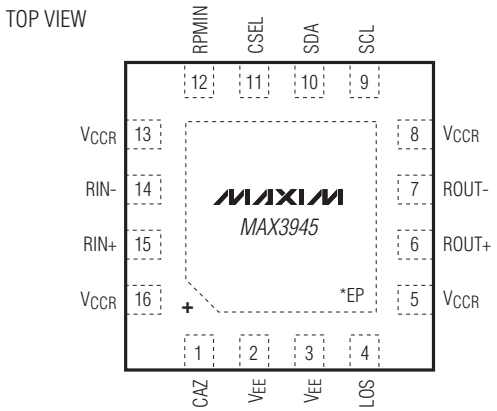


**ELECTRICAL EYE DIAGRAM AFTER 6in OF FR4
AND 72in OF CABLE WITH DEEMPHASIS (11.3Gbps K28.5, RATE_SEL = 1,
SET_CML[7:0] = 160d, RXDE_EN = 1, RXDE0 = 1, RXDE1 = 1)**



1.0625Gbps至11.3Gbps、SFP+双通道限幅放大器

引脚配置



THIN QFN
(3mm × 3mm)

*THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

引脚说明

引脚	名称	功能
1	CAZ	失调修正环路电容。连接在该引脚和相邻V_{EE}引脚之间的电容设置失调修正环路的时间常数。通过数字接口设置AZ_EN = 0，并将该引脚连接至地，即可禁用失调修正。
2, 3	V_{EE}	限幅放大器接地端。
4	LOS	信号丢失检测输出，该输出为漏极开路输出。当输入信号电平下降到SET_LOS[5:0]设置的门限以下时，触发LOS报警输出；当信号电平高于门限时，解除LOS报警状态。设置LOS_POL = 0可以使LOS输出极性反转。通过设置LOS1_EN = 0和LOS2_EN = 0，即可禁用LOS电路，参见表8。
5, 8, 13, 16	V_{CCR}	电源，为限幅放大器提供供电电压。所有的引脚必须连接至供电电源。
6	ROUT+	同相输出，CML。50Ω负载背向端接。
7	ROUT-	反相输出，CML。50Ω负载背向端接。
9	SCL	串行时钟输入，TTL/CMOS。该引脚具有75kΩ内部下拉电阻。
10	SDA	串行数据双向I/O，TTL/CMOS输入和漏极开路输出。该引脚具有75kΩ内部上拉电阻，但需要一个4.7kΩ外部上拉电阻，以满足3线数字时序的要求(提供数据线冲突保护)。
11	CSEL	片选输入，TTL/CMOS。在内部由75kΩ电阻下拉。CSEL = 1启动一个SPI工作周期；CSEL = 0时，终止SPI工作过程，并复位控制状态机。
12	RPMIN	高阻接收器功率监测输入。不使用时连接到地。
14	RIN-	反相数据输入，CML，50Ω端接。
15	RIN+	同相数据输入，CML，50Ω端接。
—	EP	裸焊盘，必须焊接到电路地。

详细说明

MAX3945的设计工作速率为1.0625Gbps至11.3Gbps。器件包括一个双通道限幅器、失调修正电路、CML输出级和LOS电路。MAX3945的特性可通过片上3线接口控制。控制器件功能的寄存器包括：RXCTRL1、RXCTRL2、RXSTAT、SET_CML、SET_LOS、MODECTRL和SET_LOSTIMER。MAX3945提供集成DAC，允许配合低成本控制器IC使用，图1所示为输入和输出结构的简化框图。

双通道限幅器

限幅放大器包含一路低数据速率通道(1.0625Gbps至4.25Gbps)和一路高数据速率通道(高达11.3Gbps)，能够对整体系统性能进行优化处理，图2所示为功能框图。数据通路选择由RATE_SEL位控制。低数据速率通道还带有一个可编程滤波器，在1.0625Gbps、1.25Gbps、2.125Gbps和4.25Gbps速率下优化工作性能。调整第一级带宽得到特定数据率下的最佳接收灵敏度并降低最大接收带宽。表1汇总了RATE_SEL、BW1和BW0控制位的功能，工作速率高达11.3Gbps时，建议采用高数据速率模式(RATE_SEL = 1)。

通过RX_POL位设置ROUT+/ROUT-相对于RIN+/RIN-的极性，如表2所示。

失调修正电路

失调修正电路用于消除差分放大器固有的失调电压所产生的PWD。连接在CAZ引脚和地之间的0.1µF外部电容将失调修正环路的截止频率设置在大约2kHz (RATE_SEL = 0)或0.7kHz (RATE_SEL = 1)。利用AZ_EN位可禁用失调修正环路，如表3所示。

CML输出级

CML输出使能和禁止

CML输出级优化于差分100Ω负载。输出级由RX_EN和SQ_EN位及内部LOS状态组合控制，请参考表4。

表1. 数据速率选择和带宽控制

RXCTRL1[3:1]			OPERATION MODE DESCRIPTION		
BW1	BW0	RATE_SEL	DATA RATE (Gbps)	FILTER BANDWIDTH (MHz)	RISE/FALL TIME (ps)
0	0	0	1.0625 to 1.25	1000	52
0	1	0	2.125	2100	52
1	0	0	2.125	2500	52
1	1	0	4.25	3000	52
X	X	1	11.3	9000	26

表2. 信号极性控制

RX_POL	OPERATION MODE DESCRIPTION
0	Inversed polarity of the differential signal path
1	Normal polarity of the differential signal path

表3. 失调修正使能/禁止控制

AZ_EN	OPERATION MODE DESCRIPTION
0	Autozero loop is disabled
1	Autozero loop is enabled

表4. CML输出级工作模式

RX_EN	SQ_EN	LOS STATUS	OPERATION MODE DESCRIPTION
0	X	X	CML output disabled
1	0	X	CML output enabled
1	1	0	CML output enabled
1	1	1	CML output disabled

1.0625Gbps至11.3Gbps、SFP+双通道限幅放大器

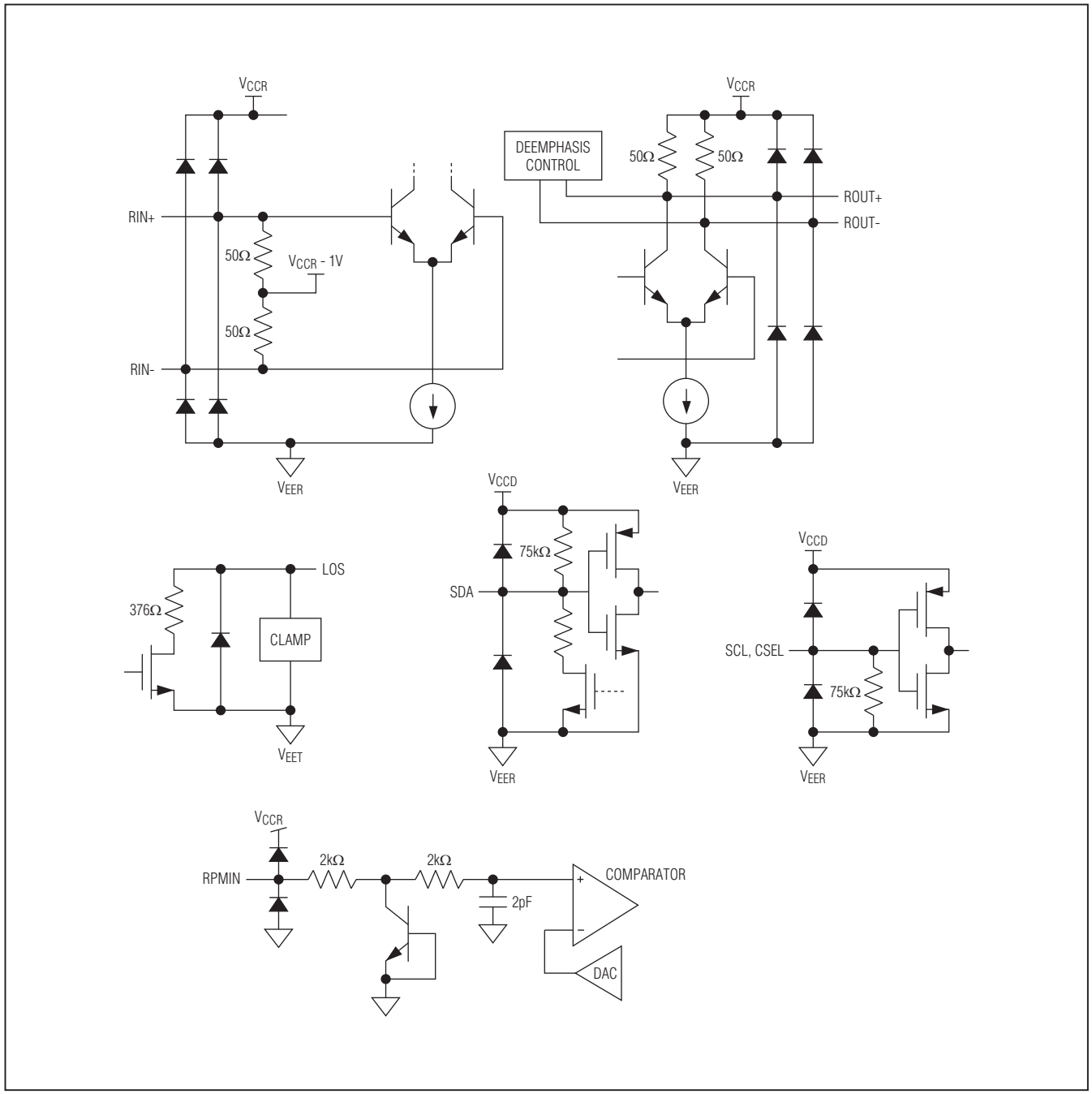


图1. 输入/输出结构简化框图

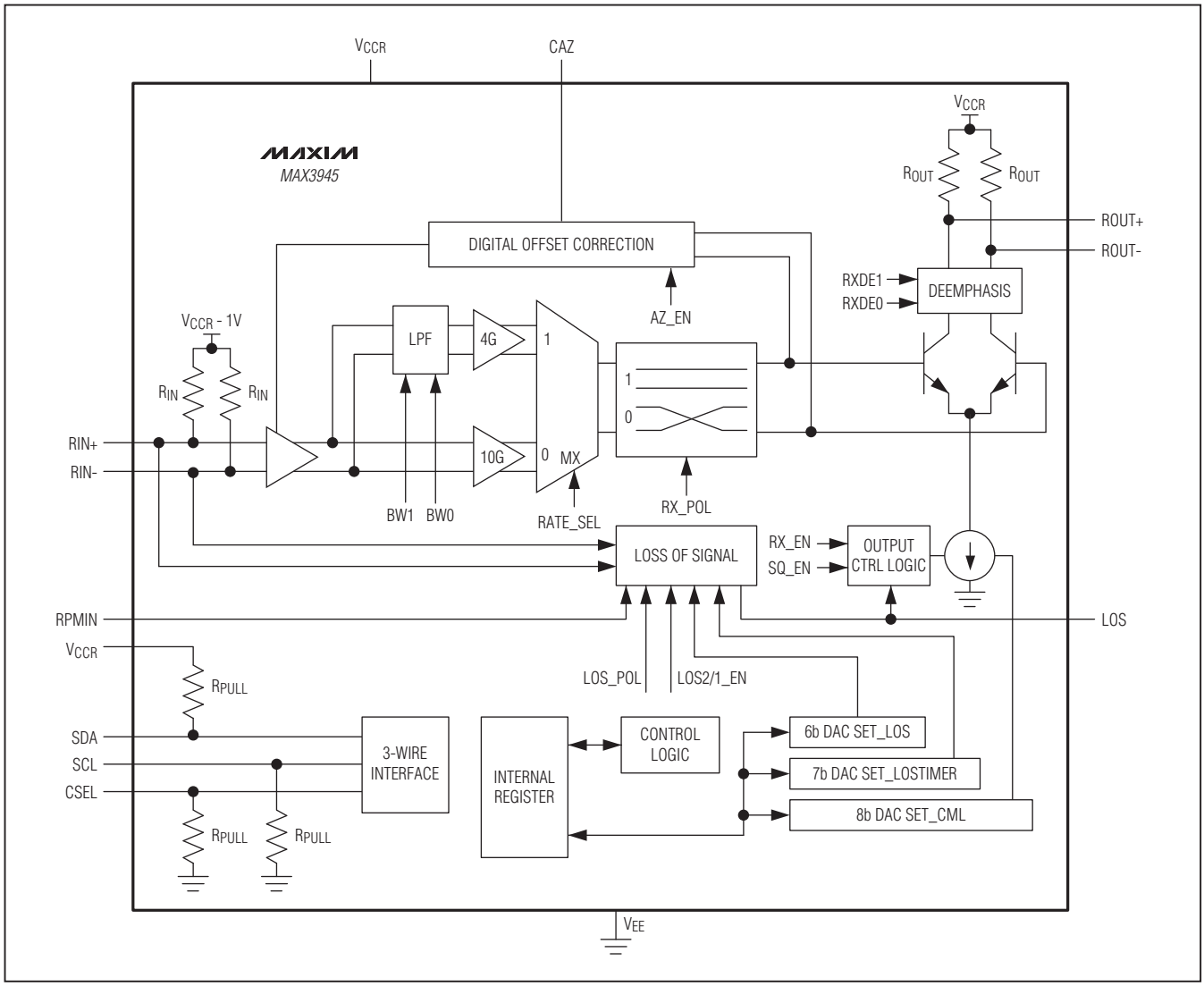


图2. 功能框图

CML输出去加重

CML输出级针对标准FR4电路板的100Ω差分传输线进行优化。RXDE1和RXDE0位增加了可编程模拟输出去加重，以补偿FR4电路板损耗和SFP连接器损耗，表5给出了去加重控制设置。

设置CML输出幅度

8位SET_CML寄存器控制CML输出幅度，最大可编程输出电平取决于MAX3945的工作模式。表6列出了这些输出电平(假设采用理想的100Ω差分负载)及其相应的控制位，表7所示为相应的输出DAC分辨率。

表5. 输出信号去加重控制

RXCTRL2[1]	RXCTRL1[7:6]		OPERATION MODE DESCRIPTION	
RXDE_EN	RXDE1	RXDE0	MODE	DEEMPHASIS (dB)
0	X	X	Deemphasis block is disabled	0
1	0	0	Deemphasis block is enabled Level 1	0.3
1	0	1	Deemphasis block is enabled Level 2	1.1
1	1	0	Deemphasis block is enabled Level 3	2.1
1	1	1	Deemphasis block is enabled Level 4	4.3

表6. CML输出幅度范围(典型值)

RXCTRL1[1]	RXCTRL2[1]	RXCTRL1[7:6]		MODE	OUTPUT AMPLITUDE (mV_{P-P})
RATE_SEL	RXDE_EN	RXDE1	RXDE0		
0	X	X	X	Low data-rate path	400 to 1192
1	0	X	X	High data-rate path	400 to 1147
1	1	0	0	High data-rate path with deemphasis	400 to 1041
1	1	0	1	High data-rate path with deemphasis	400 to 987
1	1	1	0	High data-rate path with deemphasis	400 to 908
1	1	1	1	High data-rate path with deemphasis	400 to 828

表7. CML输出DAC分辨率(典型值)

RXCTRL1[1]	RXCTRL2[1]	RXCTRL1[7:6]		MODE	RESOLUTION (mV_{P-P})
RATE_SEL	RXDE_EN	RXDE1	RXDE0		
0	X	X	X	Low data-rate path	4.5
1	0	X	X	High data-rate path	4.5
1	1	0	0	High data-rate path with deemphasis	4.1
1	1	0	1	High data-rate path with deemphasis	3.9
1	1	1	0	High data-rate path with deemphasis	3.6
1	1	1	1	High data-rate path with deemphasis	3.3

表8. LOS控制

LOS2_EN	LOS1_EN	OPERATION MODE DESCRIPTION
0	0	LOS circuitry is disabled and powered down
X	1	LOS circuitry is enabled and Rx input amplitude is detected
1	0	LOS circuitry is enabled and RPMIN input amplitude is detected

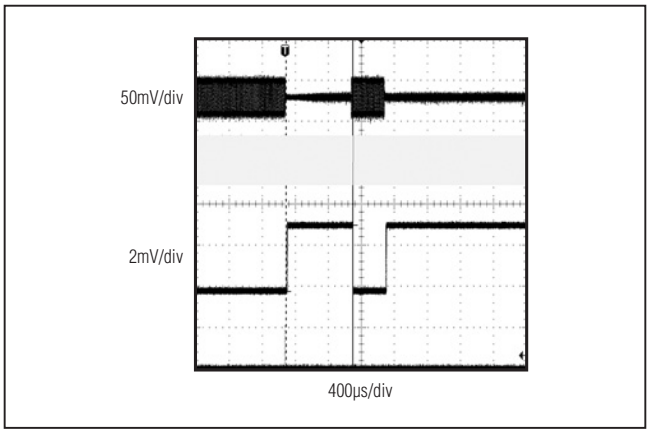


图3. 对短突发脉冲输入信号的LOS响应

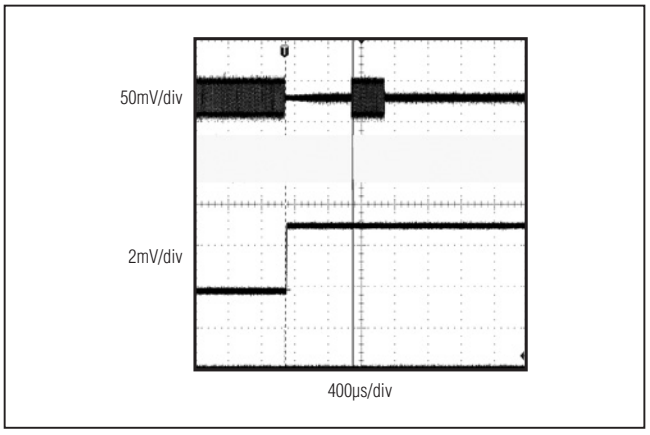


图4. 对短突发脉冲输入信号的LOS响应(在LOS屏蔽周期结束之前屏蔽LOS的任何变化)

LOS电路

LOS电路有两种工作模式，由LOS1_EN和LOS2_EN位控制(参见表8)。第一种模式下，LOS电路检测输入信号的差分幅度，并将其与SET_LOS寄存器的6个控制位预设的门限进行比较；第二种模式下，LOS电路将RPMIN引脚电压与SET_LOS寄存器的6个控制位预设的门限进行比较。第二种模式根据平均光电二极管电流使能低功耗LOS检测。

触发LOS报警输出的门限大约为1.5mV$_{P-P}$ x SET_LOS[5:0]；解除LOS报警状态的门限大约为触发门限的1.6倍，避免LOS稠楸。LOS极性、禁止控制以及LOS屏蔽时间不受LOS1_EN或LOS2_EN选择的影响。

可编程LOS输出屏蔽时间

这一功能能够在光纤链路发生光信号丢失事件后屏蔽故障输入信号。这些故障输入信号由互阻放大器的工作所导致，可能扰乱LOS输出并导致系统级链路的诊断错误。

LOS输出屏蔽时间可利用7位SET_LOSTIMER[6:0]寄存器设置在0至4500µs范围，步长为35µs。LOS信号的第1次跳变初始化输出屏蔽定时器，并在可编程LOS屏蔽周期结束之前避免对LOS输出信号的任何改变。应该仔细选择LOS输出屏蔽时间，使其大于任何预计的输入干扰的持续时间。图3中未使用LOS输出屏蔽时间功能，当输入信号变化大约800µs后，LOS信号发生变化。图4采用了LOS输出屏蔽时间功能，当输入信号发生变化时，LOS信号被屏蔽。

表9. 数字通信字结构

BIT															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Address							RWN	Data that is written or read.							

表10. 寄存器说明和地址

ADDRESS	NAME	FUNCTION
H0x00	RXCTRL1	Receiver Control Register 1
H0x01	RXCTRL2	Receiver Control Register 2
H0x02	RXSTAT	Receiver Status Register
H0x03	SET_CML	CML Output Level Setting Register
H0x04	SET_LOS	LOS Threshold Assert Level Setting Register
H0x0E	MODECTRL	General Control Register
H0x12	SET_LOSTIMER	LOS Timer Setting Register

3线数字通信

概述

MAX3945采用专有的3线数字接口，由外部控制器产生时钟。3线接口由SDA双向数据线、SCL时钟信号输入和CSEL片选输入(高电平有效)组成。外部主控制器通过使能CSEL引脚启动一次数据传输。主控制器在CSEL引脚置1后开始产生时钟信号，所有的数据传输均为最高有效位(MSB)在前。

协议

每次操作包括16位传输(15位地址/数据、1位RWN)。总线主控制器向SCL发出16个时钟周期，所有操作向MAX3945传输8位数据。RWN位确定周期为读操作还是写操作，请参考表9。

寄存器地址

MAX3945有7个可编程寄存器，表10列出了寄存器及其地址。

写模式(RWN = 0)

主控制器在SCL产生16个时钟周期。主控制器在时钟下降沿向SDA输出数据，共计16位数据(MSB在前)。主控制器通过将CSEL置0终止传输。图5所示为接口时序，表11定义了不同的时序参数。

读模式(RWN = 1)

主控制器在SCL产生16个时钟周期。主控制器在时钟下降沿向SDA输出数据，共计8位数据(MSB在前)。发送RWN位之后释放SDA，从器件在时钟的上升沿输出8位数据(MSB在前)。主控制器通过将CSEL置0终止传输，图5所示为接口时序。

模式控制

常规模式下允许对MODECTRL以外的所有寄存器执行只读命令，默认模式为常规模式。

设置模式下允许主控制器对RXSTAT以外的所有寄存器进行写操作，写入数据不受限制。为了进入设置模式，MODECTRL寄存器(地址 = H0x0E)必须置为H0x12。MODECTRL寄存器置为H0x12后，随后操作不再受限。在下一步操作完成之后，自动退出设置模式状态。如果需要进行多次不受限的设置，必须重复这一过程。

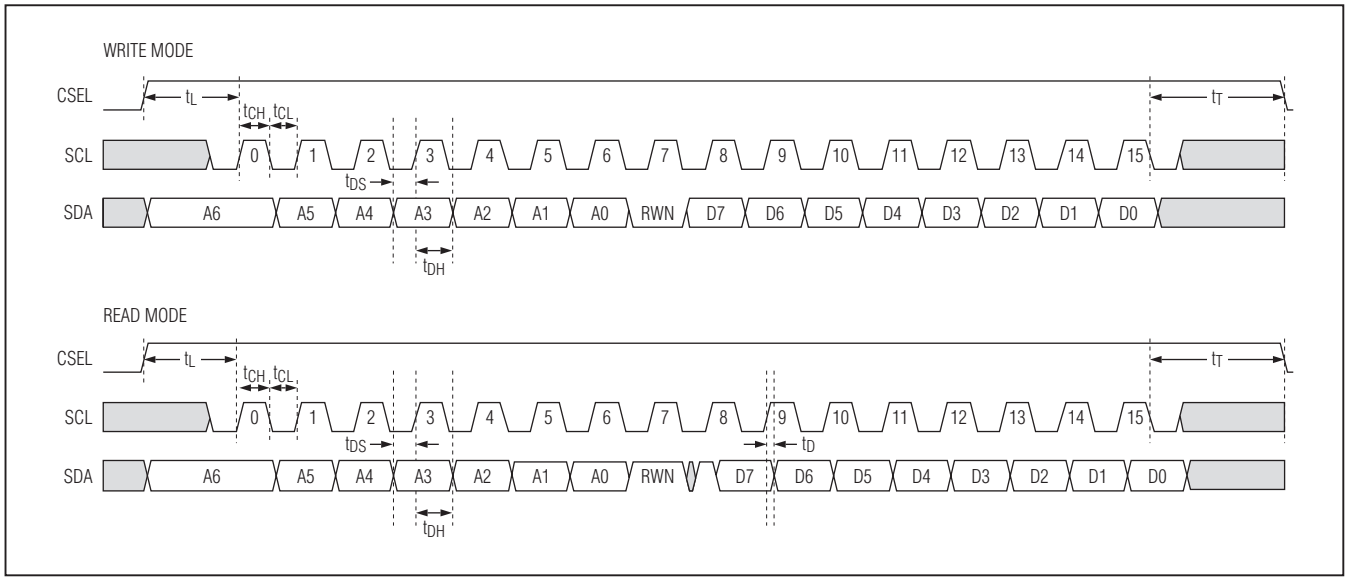


图5. 3线数字接口时序

表11. 接口时序参数

SYMBOL	DEFINITION
t_L	CSEL leading time before the first SCL edge
t_{CH}	SCL pulse-width high
t_{CL}	SCL pulse-width low
t_D	SCL rise to SDA propagation time
t_{DS}	SDA setup time
t_{DH}	SDA hold time
t_T	CSEL trailing time after last SCL edge

寄存器说明

接收器控制寄存器1 (RXCTRL1)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	RXDE1	RXDE0	X*	SOFTRES	BW1	BW0	RATE_SEL	X*	H0x00
Default Value	0	0	1	0	1	1	1	1	

**请勿修改默认设置。*

第7位和第6位：RXDE[1:0]。这2位用于控制输出波形去加重，关于控制位设置及相应的去加重电平，请参考表5。

第4位：SOFTRES。在3线接口写操作期间，若将该位置1，一旦CSEL变为低电平，所有寄存器将置为默认状态。

第3位和第2位：BW[1:0]。RATE_SEL = 0时，这2位控制限幅放大器带宽，相关设置及滤波器选择请参考表1。

第1位：RATE_SEL。RATE_SEL选择窄带数据通路(1.0625Gbps至4.25Gbps)和宽带数据通路(4.25Gbps至11.3Gbps)。RATE_SEL置1时，选择宽带通路；RATE_SEL置0时，选择窄带通路。

接收器控制寄存器2 (RXCTRL2)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	LOS2_EN	LOS1_EN	LOS_POL	RX_POL	SQ_EN	RX_EN	RXDE_EN	AZ_EN	H0x01
Default Value	0	1	1	1	0	1	0	1	

第7位：LOS2_EN。使能或禁用基于RSSI监测器的LOS电路，与LOS1_EN位组合控制。下表列出了什么情况下禁用或使能基于RSSI监测器的LOS。

LOS2_EN	LOS1_EN	RX_EN	Rx INPUT-BASED LOS	RSSI MONITOR-BASED LOS
0	0	X	Disabled and powered down	Disabled and powered down
0	1	1	Enabled	Disabled and powered down
X	1	0	Disabled and powered down	Disabled and powered down
1	1	1	Enabled	Disabled and powered down
1	0	0	Disabled and powered down	Enabled
1	0	1	Disabled and powered down	Enabled

第6位：LOS1_EN。控制基于Rx输入的LOS电路，RX_EN置0时也禁止LOS检测电路。

0 = 禁止

1 = 使能

第5位：LOS_POL。控制LOS引脚极性。

0 = 反相

1 = 标称极性

第4位：RX_POL。控制CML输出极性。

0 = 反相

1 = 标称极性

第3位：SQ_EN。SQ_EN = 1时，CML输出在触发LOS报警时被禁止。

0 = 禁止

1 = 使能

第2位：RX_EN。使能或禁用接收电路。

0 = 禁止

1 = 使能

第1位：RXDE_EN。使能或禁用CML输出去加重。

0 = 禁止

1 = 使能

第0位：AZ_EN。使能或禁用自动调零电路。

0 = 禁止

1 = 使能

接收器状态寄存器(RXSTAT)

Bit #	7	6	5	4	3	2	1 (STICKY)	0 (STICKY)	ADDRESS
Name	X	X	X	X	X	X	POR_2d	LOS_2d	H0x02
Default Value	X	X	X	X	X	X	X	X	

第1位：POR_2d。当V_{CC}供电电压低于2.3V时，POR电路将POR_2d置为高电平；当供电电压高于2.75V时，将解除POR电路的报警状态，但POR_2d位仍将保持高电平，直到读取该位。

第0位：LOS_2d。LOS状态的拷贝。这是一个关联位，读操作后清除。锁存第一次逻辑0至逻辑1的变化，直到主控制器读取该位或发生POR。

CML输出电平设置寄存器(SET_CML)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	SET_CML[7] (MSB)	SET_CML[6]	SET_CML[5]	SET_CML[4]	SET_CML[3]	SET_CML[2]	SET_CML[1]	SET_CML[0] (LSB)	H0x03
Default Value	0	1	0	1	1	1	0	0	

第7位至第0位：SET_CML[7:0]。SET_CML寄存器为8位寄存器，最大可置为255，对应于最大CML输出幅度。关于确定CML输出电平和SET_CML之间关系的公式请参考表13。

LOS门限触发电平设置寄存器(SET_LOS)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	X	SET_LOS[5] (MSB)	SET_LOS[4]	SET_LOS[3]	SET_LOS[2]	SET_LOS[1]	SET_LOS[0] (LSB)	H0x04
Default Value	X	X	0	0	1	1	0	0	

第5位至第0位：SET_LOS[5:0]。SET_LOS寄存器为6位寄存器，用于设置LOS门限。关于基于Rx输入的LOS和基于RSSI监测器的LOS的典型LOS门限电压与DAC码之间的关系，请参考*典型工作特性*部分。

通用控制寄存器(MODECTRL)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	MODECTRL[7] (MSB)	MODECTRL[6]	MODECTRL[5]	MODECTRL[4]	MODECTRL[3]	MODECTRL[2]	MODECTRL[1]	MODECTRL[0] (LSB)	H0x0E
Default Value	0	0	0	0	0	0	0	0	

第7位至第0位：MODECTRL[7:0]。MODECTRL寄存器使能常规模式和设置模式之间的转换。将该寄存器置为H0x12时，选择设置模式状态。MODECTRL必须在每次写操作之前更新。

LOS定时器设置寄存器(SET_LOSTIMER)

Bit #	7	6	5	4	3	2	1	0	ADDRESS
Name	X	SET_ LOSTIMER[6] (MSB)	SET_ LOSTIMER[5]	SET_ LOSTIMER[4]	SET_ LOSTIMER[3]	SET_ LOSTIMER[2]	SET_ LOSTIMER[1]	SET_ LOSTIMER[0] (LSB)	H0x12
Default Value	X	0	0	0	0	0	0	0	

第6位至第0位：SET_LOSTIMER[6:0]。SET_LOSTIMER寄存器为7位寄存器，数值范围从0至127。 关于定时器周期与DAC码之间的关系，请参考*典型工作特性*部分。

表12. 寄存器

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Receiver Control Register 1 Address = H0x00	RXCTRL1	R	RW	7	RXDE1	0	Rx deemphasis MSB control with RXDE_EN = 1
		R	RW	6	RXDE0	0	Rx deemphasis LSB control with RXDE_EN = 1
		R	RW	5	X	1	Must be set to 1
		R	RW	4	SOFTRES	0	Soft reset control bit
		R	RW	3	BW1	1	Input bandwidth control with RATE_SEL = 0: 00: 1GHz 01: 2.1GHz 10: 2.5GHz 11: 3GHz
		R	RW	2	BW0	1	
		R	RW	1	RATE_SEL	1	Rate-select control 0: 1G/4G mode 1: fast mode
		R	RW	0	X	1	Must be set to 1

表12. 寄存器(续)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Receiver Control Register 2 Address = H0x01	RXCTRL2	R	RW	7	LOS2_EN	0	RSSI monitor-based LOS 0: disabled 1: enabled when LOS1_EN = 0
		R	RW	6	LOS1_EN	1	Rx input-based LOS 0: disabled 1: enabled
		R	RW	5	LOS_POL	1	LOS polarity 0: inverse 1: normal
		R	RW	4	RX_POL	1	Rx polarity 0: inverse 1: normal
		R	RW	3	SQ_EN	0	Squelch 0: disabled 1: enabled
		R	RW	2	RX_EN	1	Rx control 0: disabled 1: enabled
		R	RW	1	RXDE_EN	0	Rx deemphasis 0: disabled 1: enabled
		R	RW	0	AZ_EN	1	Rx autozero control 0: disabled 1: enabled
Receiver Status Register Address = H0x02	RXSTAT	R	R	1 (sticky)	POR_2d	X	POR -> V_{CC} low limit violation
		R	R	0 (sticky)	LOS_2d	X	Copy of LOS status

表12. 寄存器(续)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
CML Output Level Setting Register Address = H0x03	SET_CML	R	RW	7	SET_CML[7]	0	MSB output level DAC
		R	RW	6	SET_CML[6]	1	
		R	RW	5	SET_CML[5]	0	
		R	RW	4	SET_CML[4]	1	
		R	RW	3	SET_CML[3]	1	
		R	RW	2	SET_CML[2]	1	
		R	RW	1	SET_CML[1]	0	
		R	RW	0	SET_CML[0]	0	LSB output level DAC
LOS Threshold Assert Level Setting Register Address = H0x04	SET_LOS	R	RW	5	SET_LOS[5]	0	MSB LOS threshold DAC
		R	RW	4	SET_LOS[4]	0	
		R	RW	3	SET_LOS[3]	1	
		R	RW	2	SET_LOS[2]	1	
		R	RW	1	SET_LOS[1]	0	
		R	RW	0	SET_LOS[0]	0	LSB LOS threshold DAC
General Control Register Address = H0x0E	MODECTRL	RW	RW	7	MODECTRL[7]	0	MSB mode control
		RW	RW	6	MODECTRL[6]	0	
		RW	RW	5	MODECTRL[5]	0	
		RW	RW	4	MODECTRL[4]	0	
		RW	RW	3	MODECTRL[3]	0	
		RW	RW	2	MODECTRL[2]	0	
		RW	RW	1	MODECTRL[1]	0	
		RW	RW	0	MODECTRL[0]	0	LSB mode control
LOS Timer Setting Register Address = H0x12	SET_LOSTIMER	R	RW	6	SET_LOSTIMER[6]	0	MSB LOS timer
		R	RW	5	SET_LOSTIMER[5]	0	
		R	RW	4	SET_LOSTIMER[4]	0	
		R	RW	3	SET_LOSTIMER[3]	0	
		R	RW	2	SET_LOSTIMER[2]	0	
		R	RW	1	SET_LOSTIMER[1]	0	
		R	RW	0	SET_LOSTIMER[0]	0	LSB LOS timer

设计步骤

设置CML输出电平

请参考表13和表14，对于表13中RXDE1和RXDE0位的每个值，去加重值随着SET_CML[7:0]的设置而变化。表13给出了SET_CML[7:0] = 120d情况下的去加重值，其它SET_CML[7:0]设置情况下的去加重值，请参考*典型工作特性*(请参考Deemphasis Value vs. SET_CML DAC Setting (RATE_SEL = 1)曲线图)。注意，即使RXDE_EN = 0，当幅值控制低于SET_CML[7:0] = 170d且RATE_SEL = 1时，仍然会存在一定程度的去加重。

选择耦合电容

对于交流耦合，耦合电容C_{IN}和C_{OUT}的选择应使接收器的确定性抖动降至最小。当输入低频截点(f_{IN})降低时，抖动会减小：$f_{IN} = 1/[2\pi(50)(C_{IN})]$。建议在MAX3945应用中采用0.1µF的$C_{IN}$和$C_{OUT}$。

选择失调修正电容

CAZ和地之间的电容决定了信号通路直流失调抑制环路的时间常数，建议在MAX3945的CAZ和地之间采用0.1µF电容。

应用信息

布局考虑

采用良好的高频布线技术以及不间断地平面的多层电路板，将EMI和串扰降至最小。

裸焊盘封装

16引脚TQFN封装的裸焊盘为IC提供了一条低热阻散热通道。该焊盘也是MAX3945的电气地，必须焊接到电路板的地，以保证适当的散热和电气性能。详细信息请参考应用笔记862：*HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*。

表13. CML输出幅度公式(典型值)

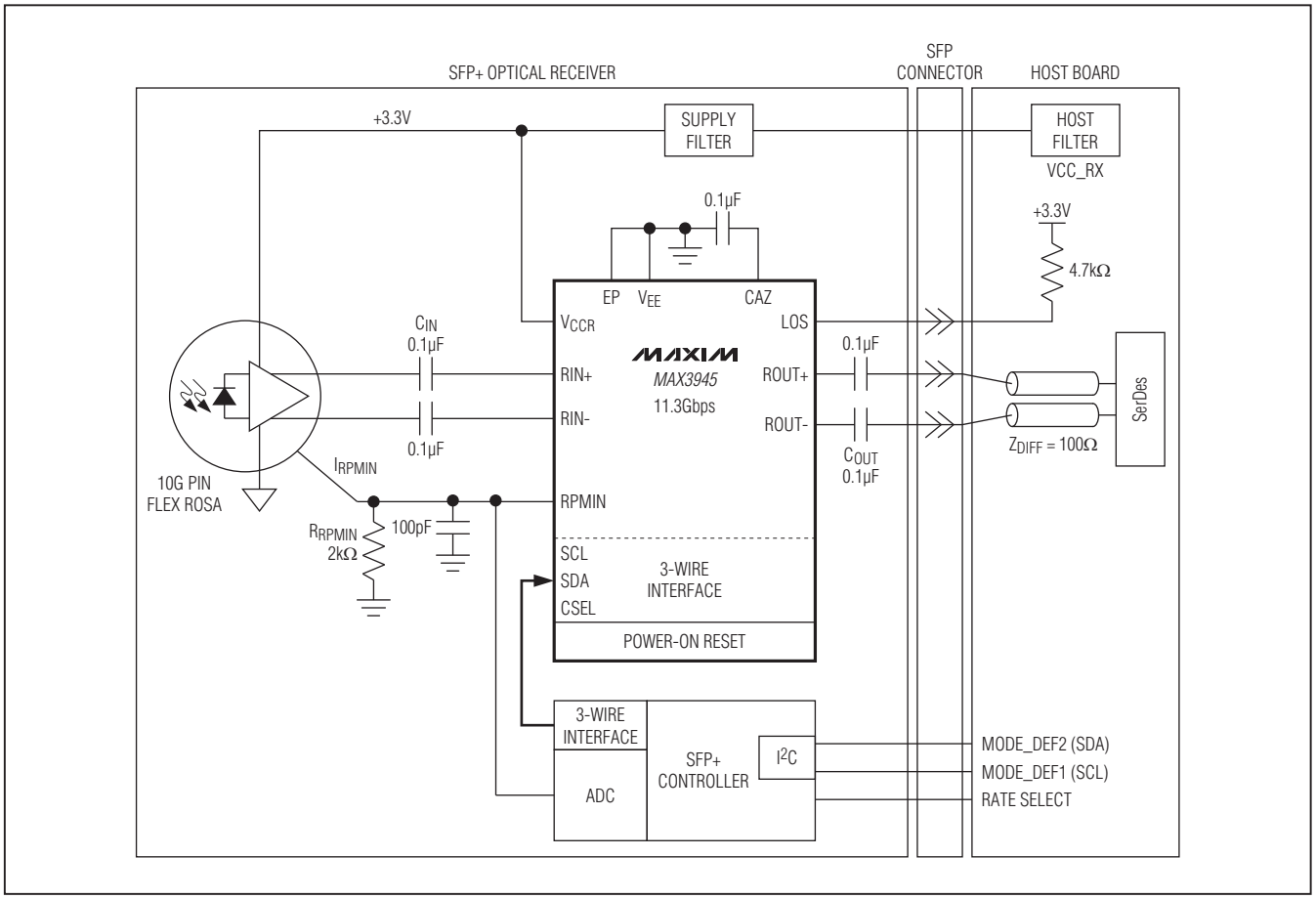
RXCTRL1[1]	RXCTRL2[1]	RXCTRL1[7:6]		DEEMPHASIS (dB) (SET_CML[7:0] = 120d)	EQUATION FOR (V_{ROUT+} - V_{ROUT-})
RATE_SEL	RXDE_EN	RXDE1	RXDE0		
0	X	X	X	0	45mV_{P-P} + 4.5mV_{P-P} x SET_CML
1	0	X	X	0.72	4.5mV_{P-P} x SET_CML
1	1	0	0	1.17	-4mV_{P-P} + 4.1mV_{P-P} x SET_CML
1	1	0	1	1.89	-7mV_{P-P} + 3.9mV_{P-P} x SET_CML
1	1	1	0	2.48	-10mV_{P-P} + 3.6mV_{P-P} x SET_CML
1	1	1	1	3.86	-13mV_{P-P} + 3.3mV_{P-P} x SET_CML

表14. 400mV_{P-P}和800mV_{P-P}输出电平的SET_CML DAC编码

RXCTRL1[1]	RXCTRL2[1]	RXCTRL1[7:6]		SET_CML DAC CODE	
RATE_SEL	RXDE_EN	RXDE1	RXDE0	400mV_{P-P}	800mV_{P-P}
0	X	X	X	80	169
1	0	X	X	91	181
1	1	0	0	98	194
1	1	0	1	106	208
1	1	1	0	115	225
1	1	1	1	126	245

1.0625Gbps至11.3Gbps、SFP+双通道限幅放大器

典型应用电路



封装信息

如需最近的封装外形信息和焊盘布局，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	文档编号
16 TQFN-EP	T1633+5	**21-0136**

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