LTC3542

500mA, 2.25MHz Synchronous Step-Down DC/DC Converter

FEATURES

- **High Efficiency: Up to 96%**
- **High Peak Switch Current: 1000mA**
- **Low Output Ripple (<20mV$_{P-P}$ Typical) Burst Mode Operation: Only 26µA**
- **Very Low Quiescent Current: Only 26µA**
- **2.5V to 5.5V Input Voltage Range**
- **2.25MHz Constant Frequency Operation**
- **1MHz to 3MHz External Frequency Synchronization**
- **Low Dropout Operation: 100% Duty Cycle**
- **No Schottky Diode Required**
- Internal Soft-Start Limits Inrush Current
- 0.6V Reference Allows Low Output Voltages
- Shutdown Mode Draws <1µA Supply Current
- ±2% Output Voltage Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Overtemperature Protected
- Available in 6-Lead 2mm × 2mm DFN and Small TSOT

APPLICATIONS

- Cellular Telephones
- Wireless and DSL Modems
- Digital Cameras
- MP3 Players
- PDAs and Other Handheld Devices

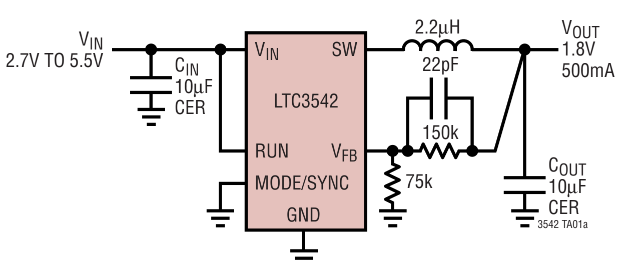
DESCRIPTION

The LTC®3542 is a high efficiency monolithic synchronous buck converter using a constant frequency, current mode architecture. Supply current during operation is only 26µA, dropping to <1µA in shutdown. The 2.5V to 5.5V input voltage range makes the LTC3542 ideally suited for single Li-Ion battery-powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems. The output voltage is adjustable from 0.6V to V_{IN}. Internal power switches are optimized to provide high efficiency and eliminate the need for an external Schottky diode.

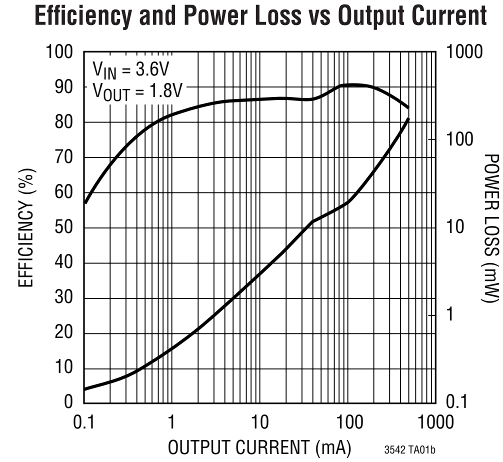
Switching frequency is internally set at 2.25MHz, allowing the use of small surface mount inductors and capacitors, and it can synchronize to an external clock signal with a frequency range of 1MHz to 3MHz through the MODE/SYNC pin. The LTC3542 is specifically designed to work well with ceramic output capacitors, achieving very low output voltage ripple and a small PCB footprint.

The LTC3542 can be configured for the power saving Burst Mode® Operation. For reduced noise and RF interference, the MODE/SYNC pin can be configured for pulse skipping operation.

TYPICAL APPLICATION



Efficiency and Power Loss vs Output Current

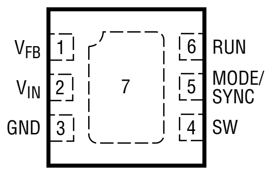


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) .... –0.3V to 6V
V_{FB}, RUN Voltages ....–0.3V to V_{IN}
MODE Voltage................................–0.3V to (V_{IN} + 0.3V)
SW Voltage ....–0.3V to (V_{IN} + 0.3V)
Operating Ambient Temperature Range
(Note 2)... –40°C to 85°C
Junction Temperature (Note 7) .... 125°C
Storage Temperature Range................... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
TSOT-23.. 300°C
Reflow Peak Body Temperature (DFN) .... 260°C

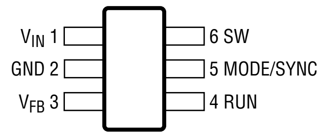
PACKAGE/ORDER INFORMATION

TOP VIEW



DC PACKAGE
6-LEAD (2mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 3°C/W (SOLDERED TO A 4-LAYER BOARD, NOTE 3)
EXPOSED PAD (PIN 7) IS PGND, MUST BE SOLDERED TO PCB

TOP VIEW



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER	DC PART MARKING	ORDER PART NUMBER	S6 PART MARKING
LTC3542EDC	LCFR	LTC3542ES6	LCFS

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.5		5.5	V
I_{FB}	Feedback Input Current					±30	nA
V_{FB}	Feedback Voltage (Note 4)		●	0.588	0.6	0.612	V
ΔV_{LINE_REG}	Reference Voltage Line Regulation (Note 4)	V_{IN} = 2.5V to 5.5V			0.04	0.2	%/V
ΔV_{LOAD_REG}	Output Voltage Load Regulation (Note 4)	I_{LOAD} = 100mA to 500mA			0.02	0.2	%
I_S	Input DC Supply Current (Note 5) Active Mode Sleep Mode Shutdown	 V_{FB} = 0.5V V_{FB} = 0.7V, MODE = 0V RUN = 0V			 26 0.1	 500 35 1	 µA µA µA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronous Frequency	V_{FB} = 0.6V		1		3	MHz
I_{LIM}	Peak Switch Current	V_{IN} = 3V, V_{FB} = 0.5V, Duty Cycle < 35%		650	1000		mA
$R_{DS(ON)}$	P-Channel On Resistance (Note 6) N-Channel On Resistance (Note 6)	I_{SW} = 100mA I_{SW} = –100mA			0.5 0.35	0.65 0.55	Ω Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{SW(LKG)}$	Switch Leakage Current	V_{IN} = 5V, V_{RUN} = 0V, V_{SW} = 0V or 5V			±0.01	±1	µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		 1.8	2.0 1.9	2.3	V V
V_{RUN}	RUN Threshold		●	0.3		1.5	V
I_{RUN}	RUN Leakage Current		●		±0.01	±1	µA
$V_{MODE/SYNC}$	MODE/SYNC Threshold		●	0.3		1.2	V
$I_{MODE/SYNC}$	MODE/SYNC Leakage Current		●		±0.01	±1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. No pin should exceed 6V.

Note 2: The LTC3542 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Failure to solder the Exposed Pad of the package to the PC board will result in a thermal resistance much higher than 40°C/W.

Note 4: The converter is tested in a proprietary test mode that connects the output of the error amplifier to the SW pin, which is connected to an external servo loop.

Note 5: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 6: The DFN switch on resistance is guaranteed by correlation to wafer level measurements.

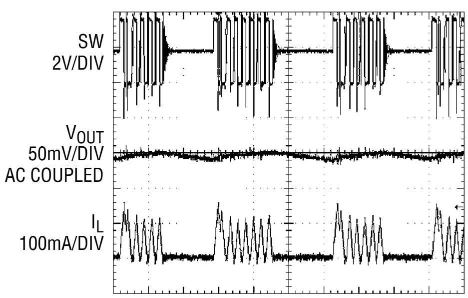
Note 7: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D) \bullet (\theta_{JA}).$$

TYPICAL PERFORMANCE CHARACTERISTICS

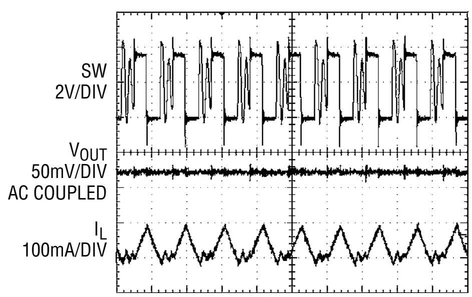
T_A = 25°C unless otherwise specified.

Burst Mode Operation



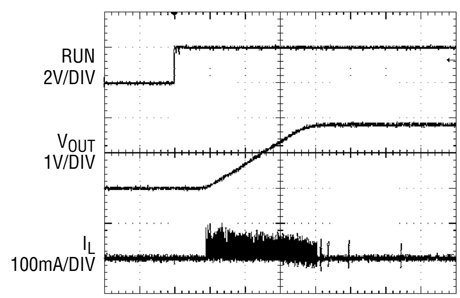
V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 25mA
FIGURE 3a CIRCUIT

Pulse Skip Mode Operation



V_{IN} = 3.6V 400ns/DIV
V_{OUT} = 1.8V
I_{LOAD} = 25mA
FIGURE 3a CIRCUIT

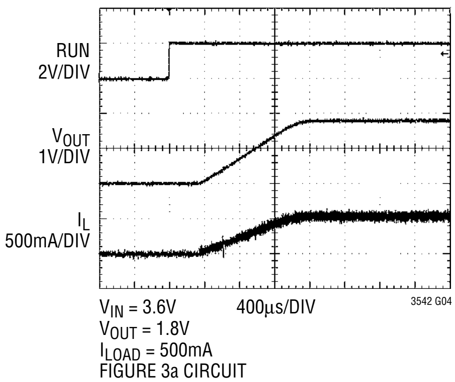
Start-Up from Shutdown



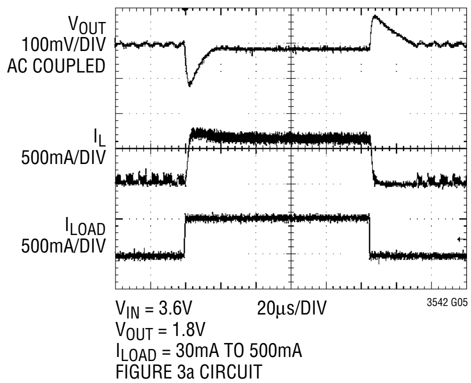
V_{IN} = 3.6V 400µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 0A
FIGURE 3a CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

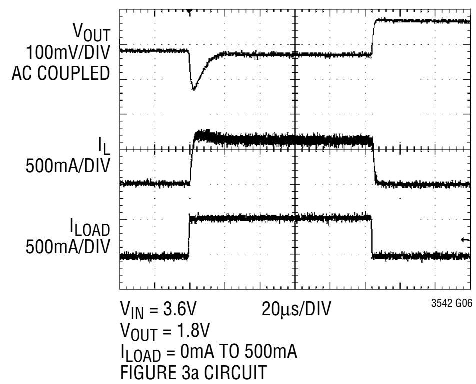
Start-Up from Shutdown



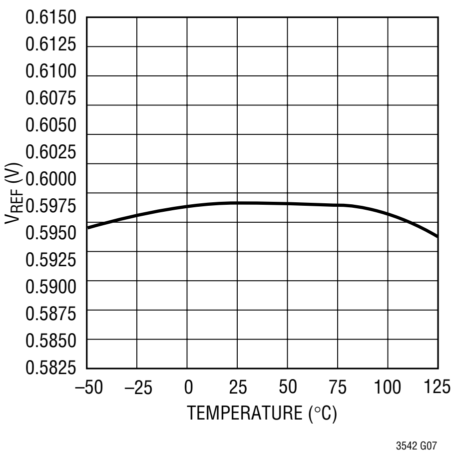
Load Step



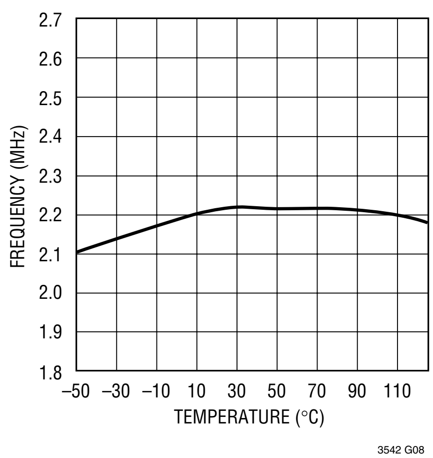
Load Step



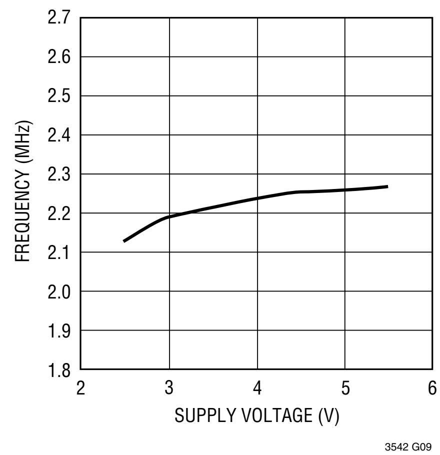
Reference Voltage vs Temperature



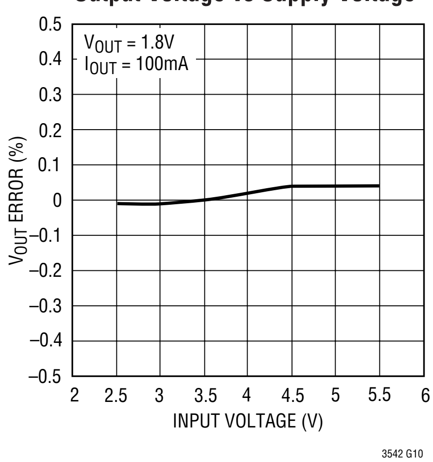
Oscillator Frequency vs Temperature



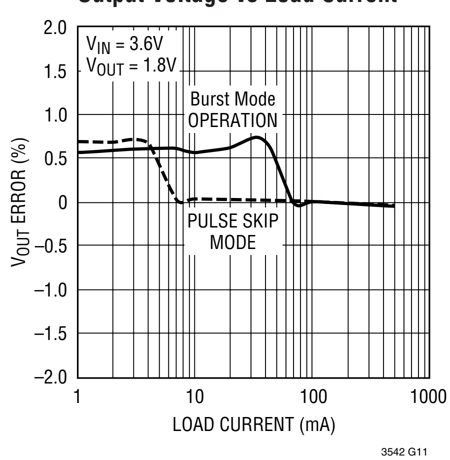
Oscillator Frequency vs Supply Voltage



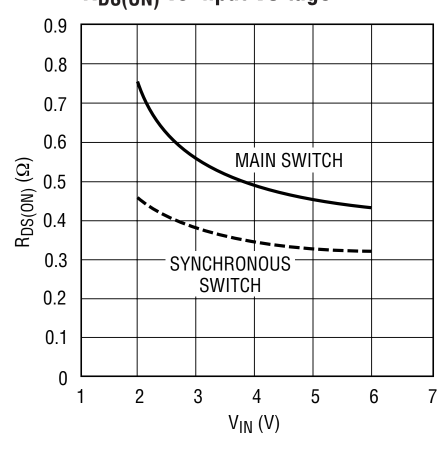
Output Voltage vs Supply Voltage



Output Voltage vs Load Current

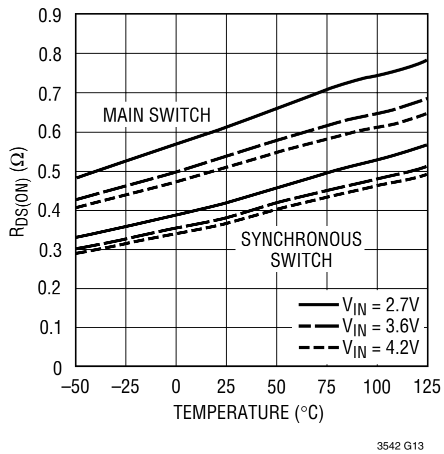


$R_{DS(ON)}$ vs Input Voltage

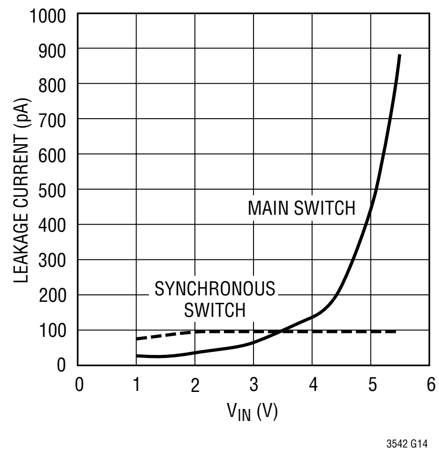


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

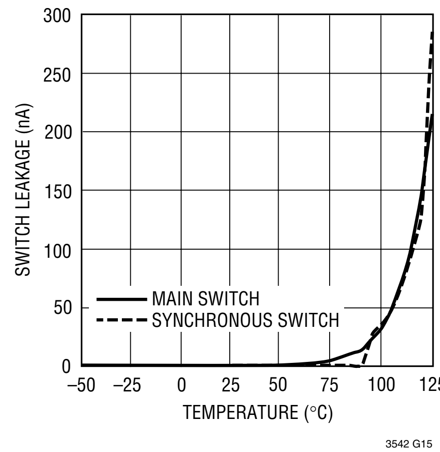
$R_{DS(ON)}$ vs Temperature



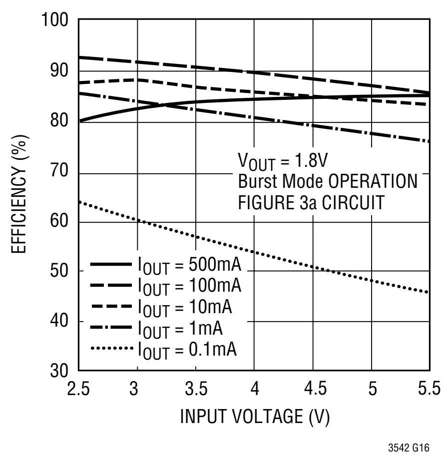
Switch Leakage vs Input Voltage



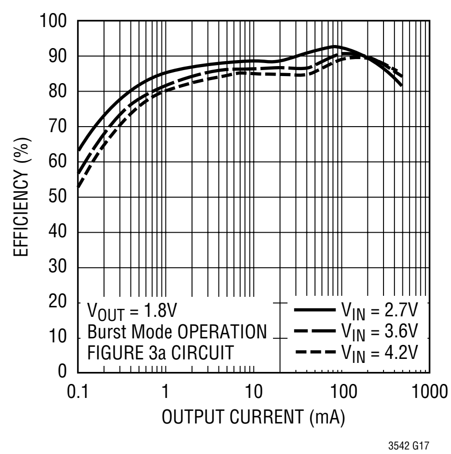
Switch Leakage vs Temperature



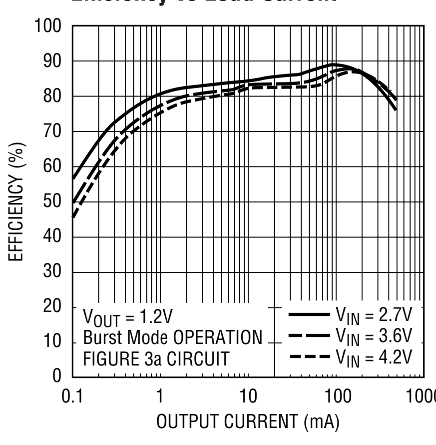
Efficiency vs Input Voltage



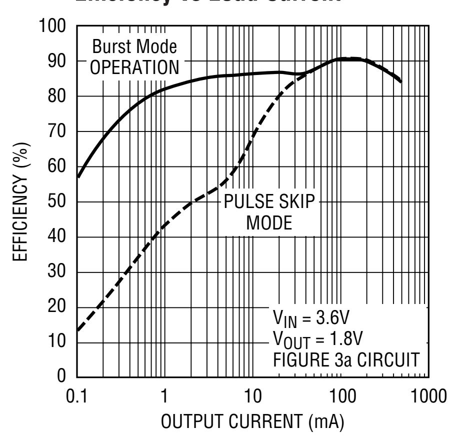
Efficiency vs Load Current



Efficiency vs Load Current



Efficiency vs Load Current



PIN FUNCTIONS (DFN/TSOT-23)

V_{FB} (Pin 1/Pin 3): Output Feedback Pin. Receives the feedback voltage from an external resistive divider across the output. Nominal voltage for this pin is 0.6V.

V_{IN} (Pin 2/Pin 1): Power Supply Pin. Must be closely decoupled to GND.

GND (Pin 3/Pin 2): Ground Pin.

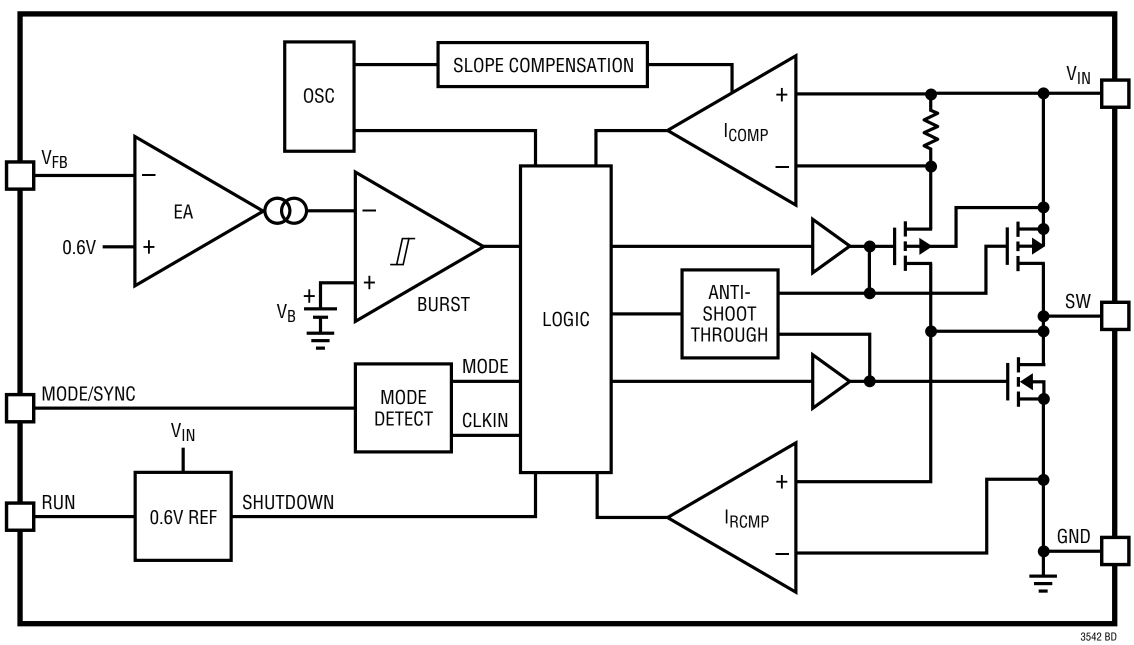
SW (Pin 4/Pin 6): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

MODE/SYNC (Pin 5/Pin 5): Mode Selection and Oscillator Synchronization Pin. This pin controls the operation of the device. When tied to GND or V_{IN}, Burst Mode operation or pulse skipping mode is selected, respectively. Do not float this pin. The oscillation frequency can be synchronized to an external oscillator applied to this pin and pulse skipping mode is automatically selected.

RUN (Pin 6/Pin 4): Converter Enable Pin. Forcing this pin above 1.5V enables this part, while forcing it below 0.3V causes the device to shut down. In shutdown, all functions are disabled drawing <1µA supply current. This pin must be driven; do not float.

GND (Pin 7, DFN Package Only): Exposed Pad. The Exposed Pad is ground. It must be soldered to PCB ground to provide both electrical contact and optimum thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3542 uses a constant frequency, current mode, step-down architecture. The operating frequency is set at 2.25MHz and can be synchronized to an external oscillator. To suit a variety of applications, the selectable MODE/SYNC pin allows the user to trade-off noise for efficiency.

The output voltage is set by an external divider returned to the V_{FB} pin. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the reference voltage. The current flows into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom switch (N-channel MOSFET) into the load until the next clock cycle. The peak inductor current is controlled by the internally compensated output of the error amplifier. When the load current increases, the V_{FB} voltage decreases slightly below the reference. This decrease causes the error amplifier to increase its output voltage until the average inductor current matches the new load current. The main control loop is shut down by pulling the RUN pin to ground.

Low Load Current Operation

By selecting MODE/SYNC pin, two modes are available to control the operation of the LTC3542 at low load currents. Both modes automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, the Burst Mode operation can be selected. When the converter is in Burst Mode operation, the peak current of the inductor is set to approximately 60mA regardless of the output load. Each burst event can last from a few cycles at light loads to almost continuously cycling with short sleep intervals at moderate loads. In between these burst events, the power MOSFETs and any unneeded circuitry are turned off, reducing the quiescent current to 26µA. In this sleep state, the load current is being supplied solely from the output capacitor. As the output voltage drops, the EA amplifier's output rises above the sleep threshold and turns the top MOSFET on. This process repeats at a rate that is dependent on the load demand. By running cycles periodically, the switching losses which are dominated by the gate charge losses of the power MOSFETs are minimized.

For lower ripple noise at low load currents, the pulse skip mode can be used. In this mode, the regulator continues to switch at a constant frequency down to very low load currents, where it will begin skipping pulses.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100%, which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor. An important design consideration is that the $R_{DS(ON)}$ of the P-channel switch increases with decreasing input supply voltage (See Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC3542 is used at 100% duty cycle with low input voltage (See Thermal Considerations in the Applications Information Section).

Low Supply Operation

To prevent unstable operation, the LTC3542 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below about 2V.

Internal Soft-Start

At start-up when the RUN pin is brought high, the internal reference is linearly ramped from 0V to 0.6V in about 1ms. The regulated feedback voltage follows this ramp resulting in the output voltage ramping from 0% to 100% in 1ms. The current in the inductor during soft-start is defined by the combination of the current needed to charge the output capacitance and the current provided to the load as the output voltage ramps up. The start-up waveform, shown in the Typical Performance Characteristics, shows the output voltage start-up from 0V to 1.8V with a 500mA load and V_{IN} = 3.6V (refer to Figure 3a).

APPLICATIONS INFORMATION

A general LTC3542 application circuit is shown in Figure1. External component selection is driven by the load requirement and begins with the selection of the inductor L. Once the inductor is chosen, C_{IN} and C_{OUT} can be selected.

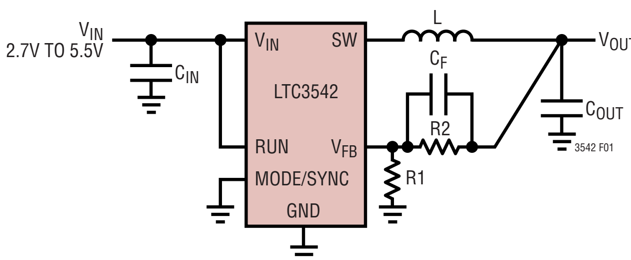


Figure 1. LTC3542 General Schematic

Inductor Selection

The inductor value has a direct effect on ripple current ΔI_L, which decreases with higher inductance and increases with higher V_{IN} or V_{OUT}, as shown in following equation:

$$\Delta I_L = \frac{V_{OUT}}{f_O \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where f_O is the switching frequency. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4 \bullet I_{OUT(MAX)}$, where $I_{OUT(MAX)}$ is 500mA. The largest ripple current ΔI_L occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT}}{f_O \bullet \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 600mA rated inductor should be enough for most applications (500mA + 100mA). For better efficiency, chose a low DC-resistance inductor.

The inductor value will also have an effect on Burst Mode operation. The transition to low current operation begins when the inductor's peak current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes the transition to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes change the size/current and price/current relationships of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3542 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3542 applications.

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where the maximum average output current I_{MAX} equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{LIM} - \Delta I_L/2$. This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours life time. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the

APPLICATIONS INFORMATION

Table 1. Representative Surface Mount Inductors

MANUFACTURER	PART NUMBER	VALUE (µH)	MAX DC CURRENT (A)	DCR (Ω)	SIZE (mm³)
Sumida	CDRH2D11-2RM	2.2	0.780	0.098	3.2 × 3.2 × 1.2
	CDRH3D16	2.2	1.2	0.075	3.8 × 3.8 × 1.8
	CMD4D11	2.2	0.95	0.116	4.4 × 5.8 × 1.2
	CDH2D09B	3.3	0.85	0.15	2.8 × 3 × 1
	CLS4D09	4.7	0.75	0.15	4.9 × 4.9 × 1
Murata	LQH32CN	2.2	0.79	0.097	2.5 × 3.2 × 1.55
	LQH43CN	4.7	0.75	0.15	4.5 × 3.2 × 2.6
TDK	IVLC453232	2.2	0.85	0.18	4.8 × 3.4 × 3.4
	VLF3010AT-2R2M1R0	2.2	1.0	0.12	2.8 × 2.6 × 1

design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling, when not using an all ceramic capacitor solution.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \bullet f_O \bullet C_{OUT}} \right)$$

where f_O is the switching frequency, C_{OUT} is the output capacitance and ΔI_L is the inductor ripple current. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

If tantalum capacitors are used, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current rating, high voltage rating and low ESR are tempting for switching regulator use. However, the ESR is so low that it can cause loop stability problems. Since the LTC3542's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used to achieve very low output ripple and small circuit size. X5R or X7R ceramic capacitors are recommended because these dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part. For more information, see Application Note 88. The recommended capacitance value to use is 10µF for both input and output capacitors.

APPLICATIONS INFORMATION

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1 + \frac{R2}{R1}\right)$$

To improve the frequency response, a feed-forward capacitor, C_F, may also be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Mode Selection and Frequency Synchronization

The MODE/SYNC pin is a multipurpose pin that provides mode selection and frequency synchronization. Connecting this pin to GND enables Burst Mode operation, which provides the best low current efficiency at the cost of a higher output voltage ripple. Connecting this pin to V_{IN} selects pulse skip mode operation, which provides the lowest output ripple at the cost of low current efficiency. The LTC3542 can also be synchronized to an external clock signal with range from 1MHz to 3MHz by the MODE/SYNC pin. During synchronization, the mode is set to pulse skip and the top switch turn-on is synchronized to the falling edge of the external clock.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3542 circuits: 1) V_{IN} quiescent current, 2) I^2R loss and 3) switching loss. V_{IN} quiescent current loss dominates the power loss at very low load currents, whereas the other two dominate at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power loss is of no consequence as illustrated in Figure 2.

1) The V_{IN} quiescent current is the DC supply current given in the Electrical Characteristics which excludes MOSFET charging current. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load.

2) I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L, but is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(D) + (R_{DS(ON)BOT})(1 – D)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

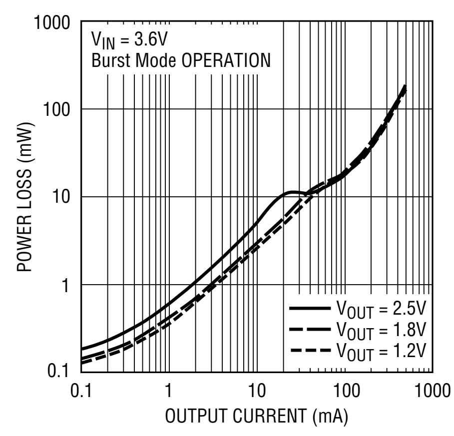


Figure 2. Power Loss vs Load Current

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3) The switching current is MOSFET gate charging current, that results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

Other "hidden" losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses include diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In most applications the LTC3542 does not dissipate much heat due to its high efficiency. But in applications where the LTC3542 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3542 from exceeding the maximum junction temperature, the user need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3542 in dropout at an input voltage of 2.7V, a load current of 500mA and an ambient temperature of 70°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is approximately 0.7Ω. Therefore, power dissipated by the part is:

$$P_D = I_{LOAD}^2 \bullet R_{DS(ON)} = 175\text{mW}$$

For the DFN package, the θ_{JA} is 40°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 70°C + 0.175 \bullet 40 = 77°C$$

which is below the maximum junction temperature of 125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching loads with large (>1µF) bypass capacitors. The discharged bypass capacitors are effectively put in

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parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limit, short circuit protection and soft-start.

Design Example

As a design example, assume the LTC3542 is used in a single lithium-ion battery-powered cellular phone application. The V_{IN} will be operating from a maximum of 4.2V down to about 2.7V. The load current requirement is a maximum of 0.5A, but most of the time it will be in standby mode, requiring only 2mA. Efficiency at both low and high load currents is important. Output voltage is 1.8V.

With this information we can calculate L using:

$$L = \frac{1}{f \bullet \Delta I_L} \bullet V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Substituting V_{OUT} = 1.8V, V_{IN} = 4.2V, ΔI_L = 200mA and f = 2.25MHz gives:

$$L = \frac{1.8V}{2.25MHz \bullet 200mA} \bullet \left(1 - \frac{1.8V}{4.2V}\right) = 2.28\mu H$$

Choosing a vendor's closest inductor value of 2.2µH results in a maximum ripple current of:

$$\Delta I_L = \frac{1.8V}{2.25MHz \bullet 2.2\mu H} \bullet \left(1 - \frac{1.8V}{4.2V}\right) = 207.8mA$$

C_{IN} will require an RMS current rating of at least 0.25A ≅ $I_{LOAD(MAX)}/2$ at temperature and C_{OUT} will require ESR of less than 0.2Ω. In most cases, ceramic capacitors will satisfy these requirements. Select C_{OUT} = 10µF and C_{IN} = 10µF.

For the feedback resistors, choose R1 = 75k, R2 can be calculated from:

$$R2 = \left(\frac{V_{OUT}}{0.6V} - 1\right) \bullet R1 = \left(\frac{1.8V}{0.6V} - 1\right) \bullet 75k = 150k$$

Figure 3 shows the complete circuit along with its efficiency curve, load step response and recommended layout

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3542. These items are also illustrated graphically in Figure 3b. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.

2. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and ground.

3. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.

4. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

5. Keep the switching node, SW, away from the sensitive V_{FB} node.

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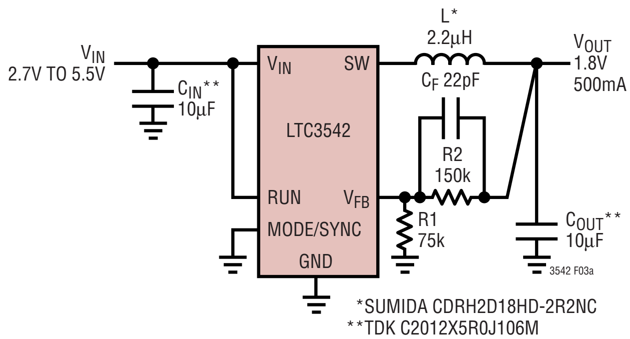


Figure 3a. Typical Application

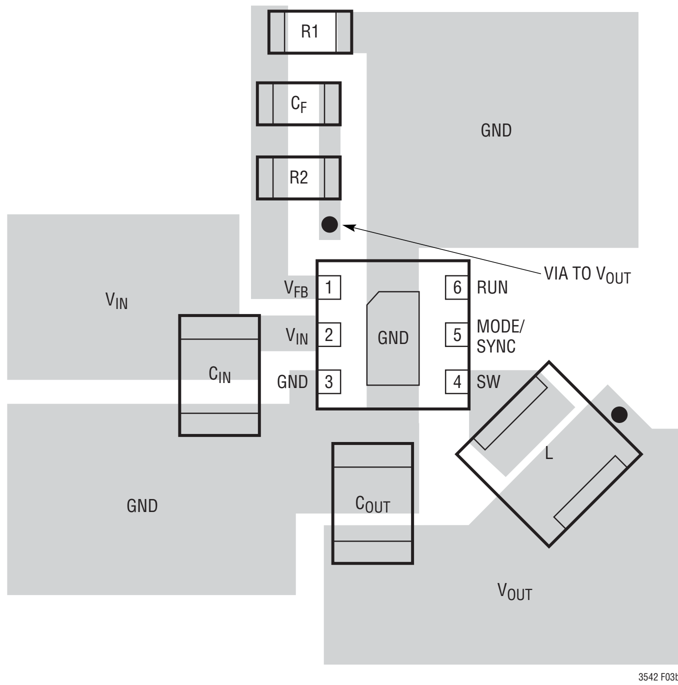


Figure 3b. Layout Diagram

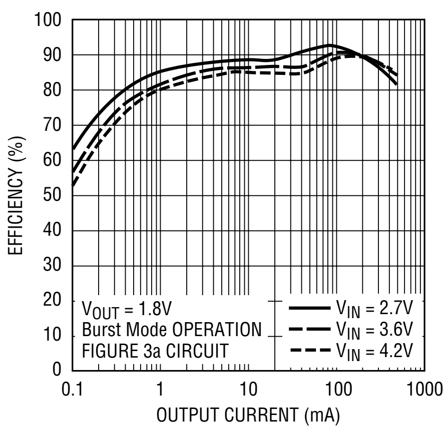


Figure 3c. Efficiency Curve

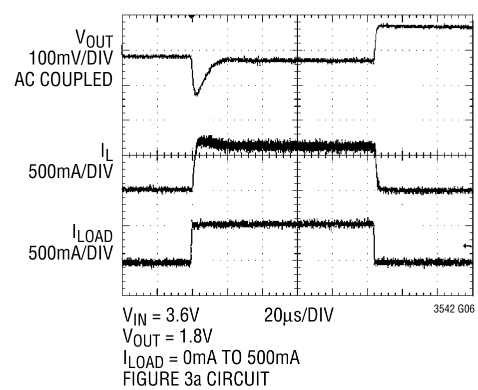
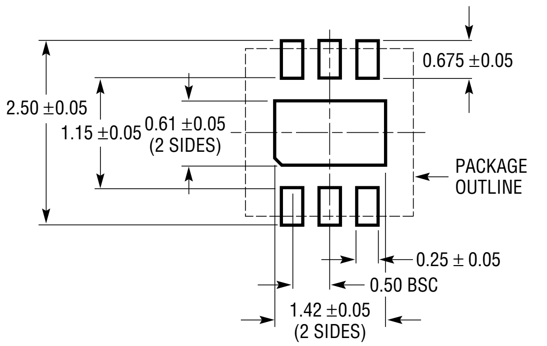


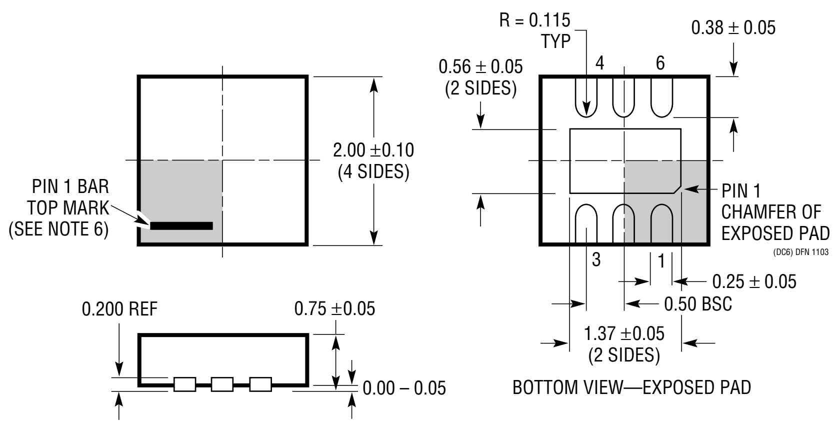
Figure 3d. Load Step

PACKAGE DESCRIPTION

DC Package
6-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1703)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

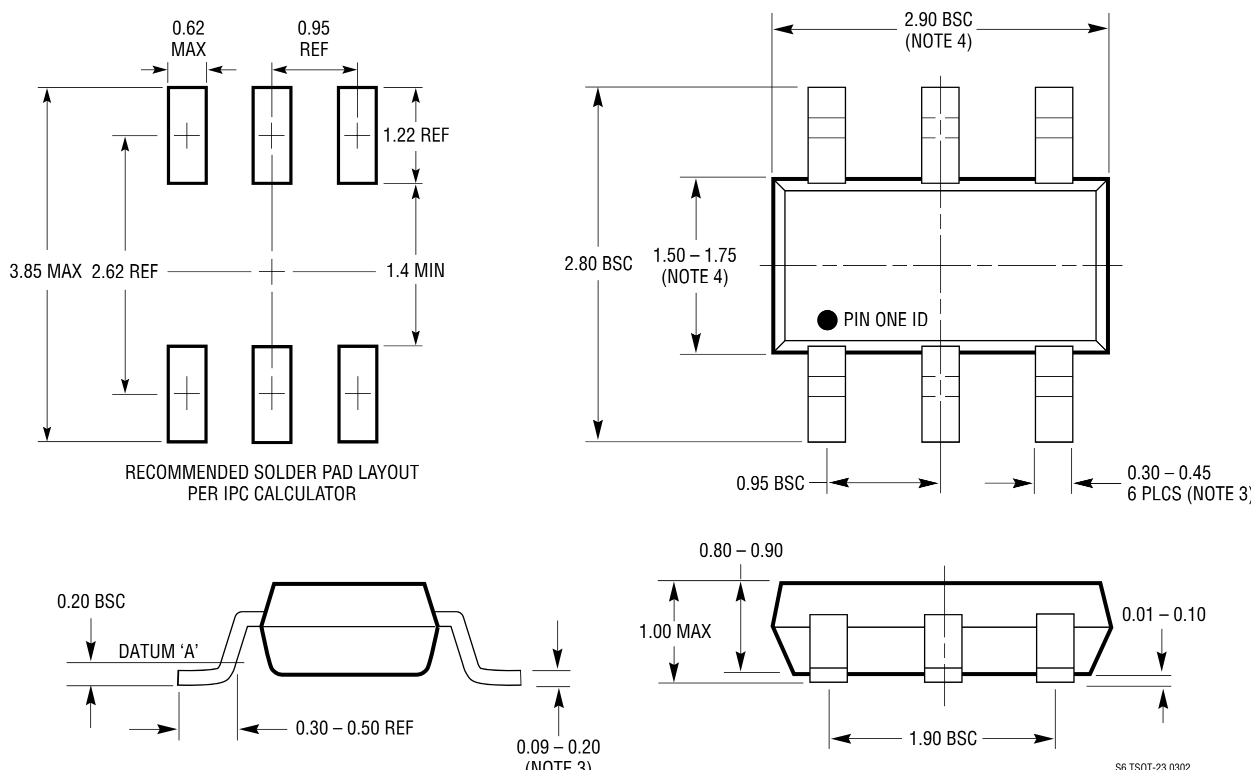


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

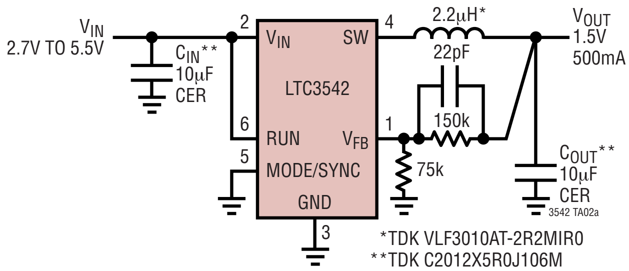
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

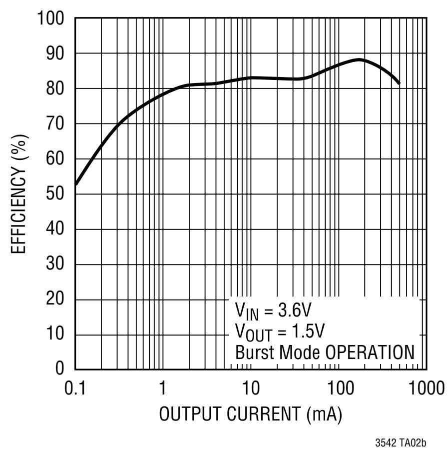
TYPICAL APPLICATION

Using Low Profile Components, <1mm Height



*TDK VLF3010AT-2R2MIR0
**TDK C2012X5R0J106M

Efficiency vs Output Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3405/LTC3405B	300mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20μA, I_{SD} < 1μA, ThinSOT Package
LTC3406/LTC3406B	600mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20μA, I_{SD} < 1μA, ThinSOT Package
LTC3407/LTC3407-2	Dual 600mA/800mA I_{OUT}, 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40μA, I_{SD} < 1μA, MS10E, DFN Packages
LTC3409	600mA I_{OUT}, 1.7MHz/2.6MHZ, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65μA, I_{SD} < 1μA, DFN Package
LTC3410/LTC3410B	300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26μA, I_{SD} < 1μA, SC70 Package
LTC3411	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60μA, I_{SD} < 1μA, MS10, DFN Packages
LTC3548	Dual 400mA/800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40μA, I_{SD} < 1μA, MS10, DFN Packages
LTC3561	1A I_{OUT}, 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.6V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 240μA, I_{SD} < 1μA, 3mm × 3mm DFN Package

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