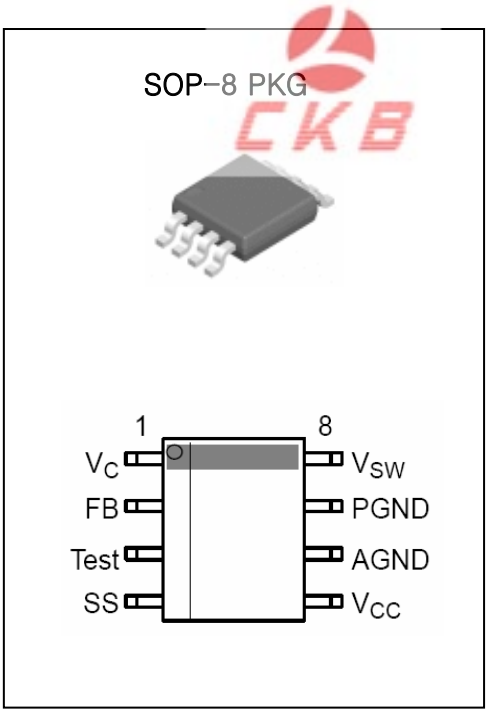
## FEATURES

- Intergrated Power Switch 1.5A Guaranteed
- Wide Input Voltage Range 2.7V to 30V
- High Frequency Allows for Small Components
- Minimum External Components
- Easy External Synchronization
- Frequency Foldback Reduces Component Stress During an Overcurrent Condition
- Thermal Shutdown with Hysteresis
- Shut Down Current is 50 uA Maximum
- Wide Ambient Temperature Range Commercial Grade : 0℃ to 70℃
- Moisture Sensitivity Level 3




ORDERING INFORMATION

| Device | Marking | Package |
|---|---|---|
| LM5171D | LM5171 | SOP-8 |

## DESCRIPTION

The LM5171 product is 280 kHz switching regulator with a high efficiency, 1.5A intergrated switch. This part operate over a wide input voltage range, from 2.7V to 30V. The flexibility of the design allows the chip to operate in most power supply configurations, including boost, flyback, forward, invering, and SEPIC.

This Ics utilize current mode architecture, which allows excellent load and line regulatuon, as well as a practical means for limiting current. Combining high frequency operation with a highly integrated regulator circuit results in an extremely compact power supply solution. The circuit design include provisions for features such as frequency synchronization, shutdown, and feedback control.

Figure 1. Application Circuit

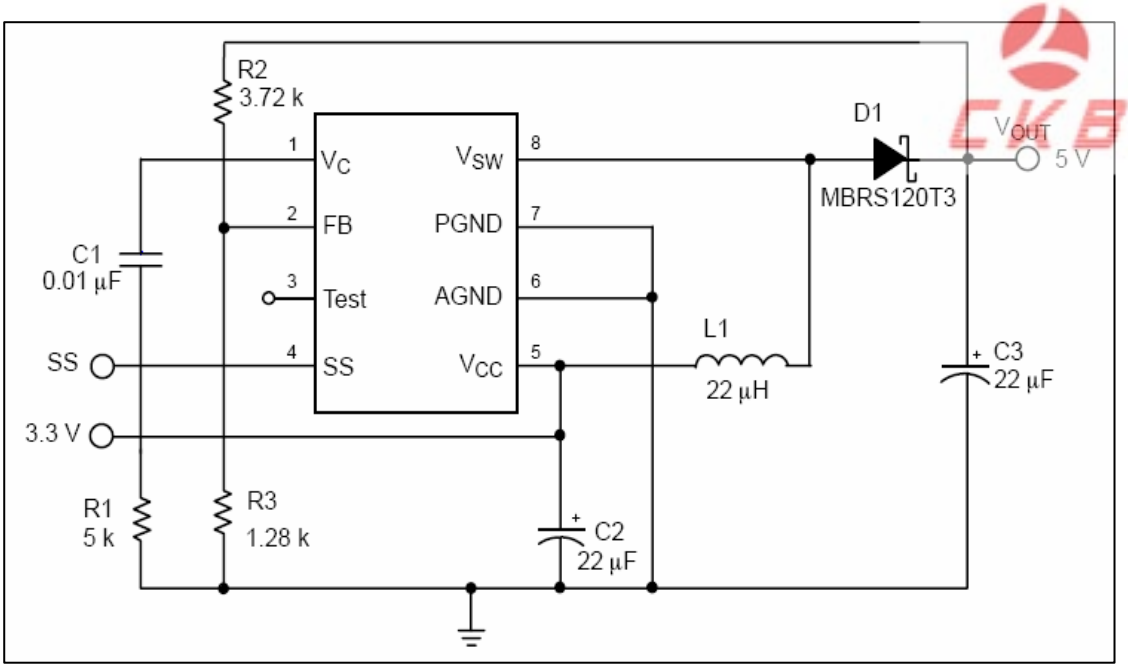
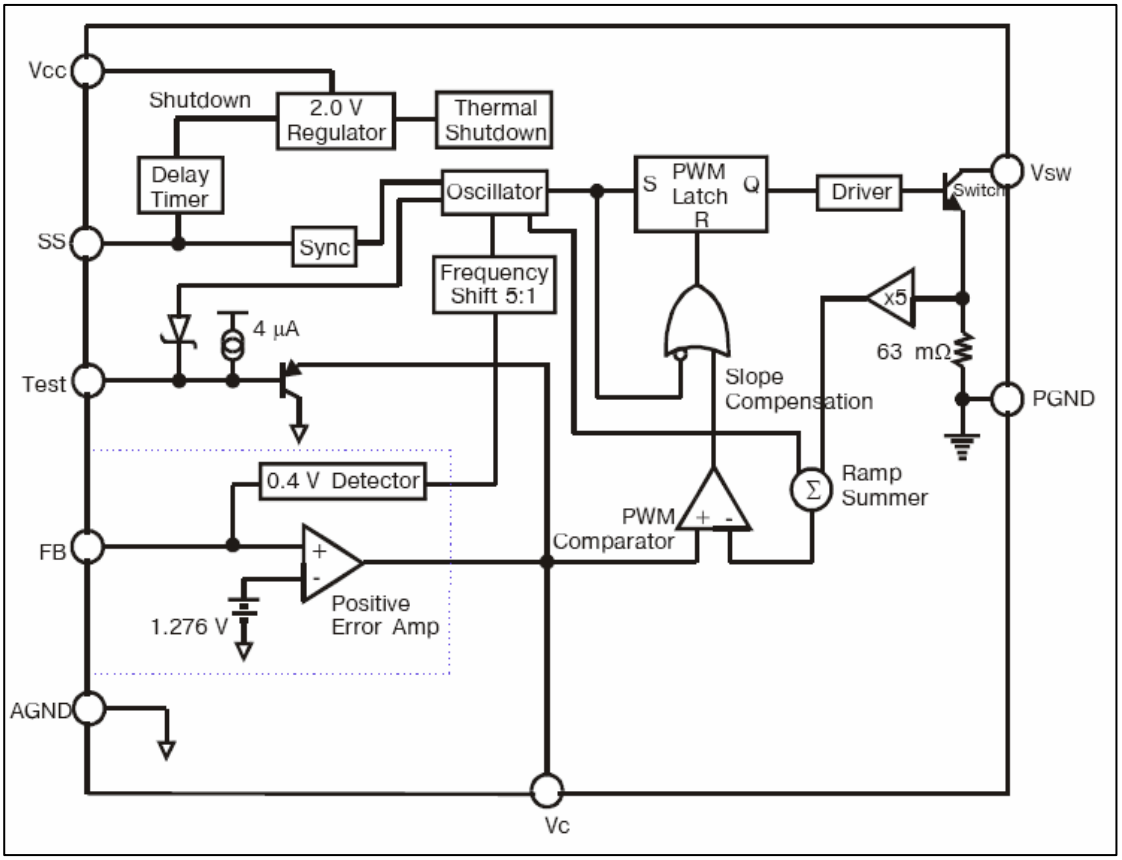



Figure 2. Block Diagram



## ABSOLUTE MAXIMUM RATINGS

(Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Maximum ratings applied to the device are individule stress limit value and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, dama may occur and reliability may be affected.

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Junction Temperature Range | $T_J$ | 0 to125 | ℃ |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | ℃ |
| Thermal Resistance, Juntion to Ambient | $R_{\theta JA}$ | 165 | ℃/W |
| Thermal Resistance, Juntion to Case | $R_{\theta JC}$ | 45 | ℃/W |
| Minimum ESD Rating (Human Body Model :C=100 pF, R=1.5kΩ) | – | 1.2 | kV |
| Lead Temperature Soldering : Reflow (Note 1) | – | 230 | ℃ |

Note 1. 60 second maximum above 183℃

## ABSOLUTE MAXIMUM RATINGS

(Operating Ratings indicate conditions for which the device is intended to be but do not guarantee specific performance limits. For guaranteed specifications, see the Electrical Characteristics.)

| Pin Name | Pin Symbol | $V_{MAX}$ | $V_{MIN}$ | $I_{SOURCE}$ | $I_{SINK}$ |
|---|---|---|---|---|---|
| IC Power Input | Vcc | 30 V | − 0.3 V | N / A | 200 mA |
| Shutdown / Sync | SS | 30 V | − 0.3 V | 1.0 mA | 1.0 mA |
| Loop Compensation | Vc | 6.0 V | − 0.3 V | 10 mA | 10 mA |
| Voltage Feedback Input | FB | 10 V | − 0.3 V | 1.0 mA | 1.0 mA |
| Test Pin | Test | 6.0 V | − 0.3 V | 1.0 mA | 1.0 mA |
| Power Ground | PGND | 0.3 V | − 0.3 V | 4.0 A | 1.0 mA |
| Analog Ground | AGND | 0 V | 0 V | N / A | 10 mA |
| Switch Input | Vsw | 40 V | − 0.3 V | 10 mA | 3.0 A |

ELECTRICAL CHARACTERISTICS (2.7V < Vcc < 30 V, 0℃ < $T_J$ < 125℃, unless otherwise stated. )

| Characteristics | Test Condition | Min | TYP | Max | Unit |
|---|---|---|---|---|---|
| **Error Amplifier** | | | | | |
| FB Reference Voltage | Vc tied to FB : Measure at FB | 1.246 | 1.276 | 1.300 | V |
| FB Input Voltage | FB = $V_{REF}$ | −1.0 | 0.1 | 1.0 | uA |
| FB Reference Voltage Line Regulati | Vc = FB | – | 0.01 | 0.03 | %/V |
| Error Amp Transconductance | Ivc = ±25 uA | 300 | 550 | 800 | uMho |
| Error Amp Gain | Note 2 | 200 | 500 | – | V/ V |
| Vc Source current | FB = 1.0V, Vc = 1.25V | 25 | 50 | 90 | uA |
| Vc Sink Current | FB = 1.5V, Vc = 1.25V | 200 | 625 | 1500 | uA |
| Vc High Clamp Voltage | FB = 1.0V, Vc sources 25uA | 1.5 | 1.7 | 1.9 | V |
| Vc Low Clamp Voltage | FB = 1.5V, Vc sinks 25uA | 0.25 | 0.50 | 0.65 | V |
| Vc Threshold | Reduce Vc from 1.5V until switching stops | 200 | 625 | 1500 | uA |
| **Oscillator** | | | | | |
| Base Operating Frequency | FB = 1V | 230 | 280 | 310 | kHz |
| Reduced Operating Frequency | FB = 0V | 30 | 52 | 120 | kHz |
| Maximum Duty Cycle | | 90 | 94 | – | % |
| FB Frequency Shift Threshold | Frequency Drops to reduced operating frequency | 0.36 | 0.40 | 0.44 | V |
| **Sync / Shutdown** | | | | | |
| Sync Range | | 320 | – | 500 | kHz |
| Sync Pulse Transition Threshold | Rise Time = 20 ns | 2.5 | – | – | V |
| SS Bias Current | SS = 0V | −15 | −3 | – | uA |
| | SS = 3.0V | – | 3 | 8 | |
| Shutdown Threshold | | 0.50 | 0.85 | 1.20 | V |
| Shutdown Delay | 2.7V ≤ Vcc ≤ 12V | 12 | 80 | 350 | us |
| | 12V ≤ Vcc ≤ 30V | 12 | 36 | 200 | us |
| **Power Switch** | | | | | |
| Switch Saturation Voltage | $I_{SWITCH}$ = 1.5A, Note 2 | – | 0.8 | 1.4 | V |
| | $I_{SWITCH}$ = 1.0A, 0℃≤$T_A$≤70℃ | – | 0.55 | 1.00 | V |
| | $I_{SWITCH}$ = 10mA | – | 0.09 | 0.45 | V |
| Switch Current Limit | 50% duty cycle, Note 2 | 1.6 | 1.9 | 2.4 | A |
| | 80% duty cycle, Note 2 | 1.5 | 1.7 | 2.2 | A |
| Minimum Pulse Width | FB = 0V, Isw=4.0A, Note 2 | 200 | 250 | 300 | ns |
| ΔIcc/ΔIvsw | 2.7V≤Vcc≤12V, 10mA≤Isw≤1.0A | – | 10 | 30 | mA/A |
| | 12V≤Vcc≤30V, 10mA≤Isw≤1.0A | – | – | 100 | mA/A |
| | 2.7V≤Vcc≤12V,10mA≤Isw≤1.5A(note2) | – | 17 | 30 | mA/A |
| | 12V≤Vcc≤30V, 10mA≤Isw≤1.5A(note2) | – | – | 100 | mA/A |
| Switch Leakage | Vsw = 40V, Vcc = 0V | – | 2.0 | 100 | uA |
| **General** | | | | | |
| Operating Current | Isw = 0 | – | 5.5 | 8 | mA |
| Shutdown mode Current | Vc<0.8V, SS=0V, 2.7V≤Vcc≤12V | – | 12 | 60 | uA |
| | Vc<0.8V, SS=0V, 12V≤Vcc≤30V | – | – | 100 | uA |
| Minimum Operating Input Voltage | Vsw Switching, Maximum Isw=10mA | – | 2.45 | 2.70 | V |
| Thermal Shutdown | Note 2 | 150 | 180 | 210 | ℃ |
| Thermal Hysteresis | Note 2 | – | 25 | – | ℃ |

Note 2 : Guaranteed by design, not 100% tested in production.

## TYPICAL PERFORMANCE CHARACTERISTICS

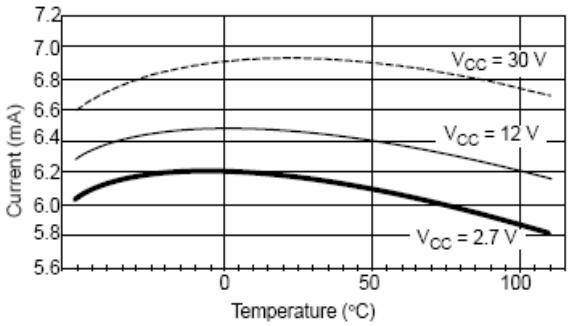



Figure 3. $I_{CC}$ (No Switching) vs. Temperature

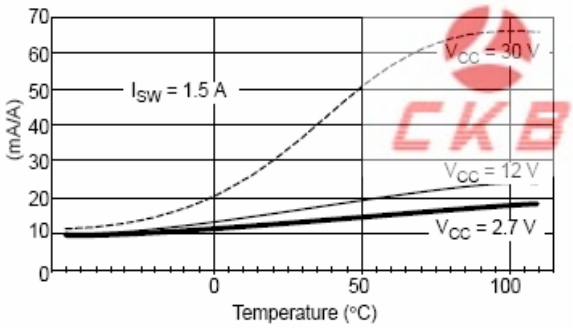



Figure 4. $\Delta I_{CC}/\Delta I V_{SW}$ vs. Temperature

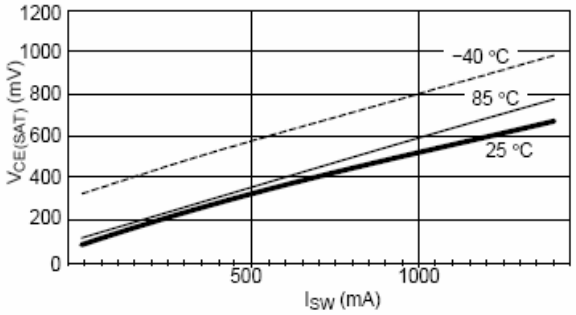



Figure 5. $V_{CE(SAT)}$ vs. $I_{SW}$

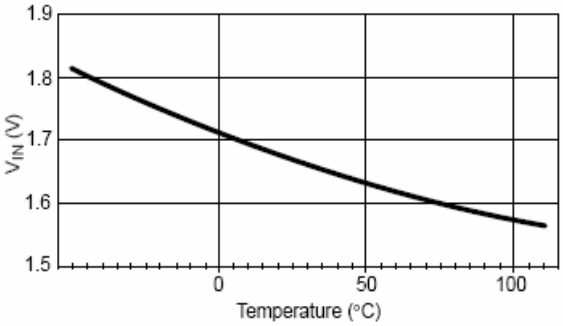



Figure 6. Minimum Input Voltage vs. Temperature

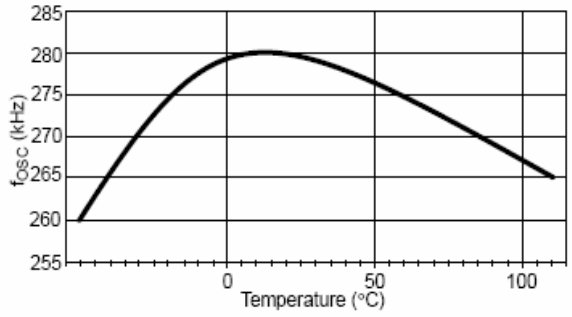



Figure 7. Switching Frequency vs. Temperature

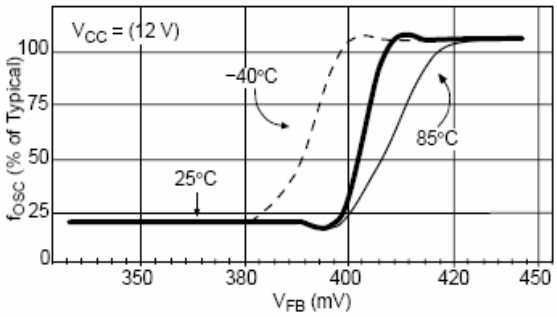



Figure 8. Switching Frequency vs. $V_{FB}$

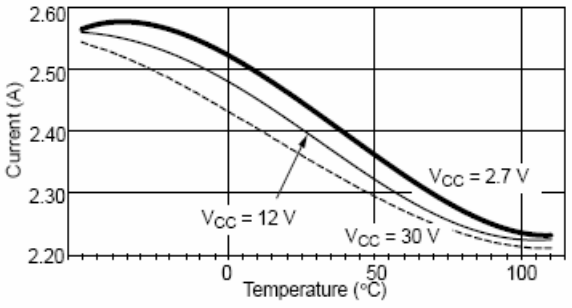



Figure 9. Current Limit vs. Temperature

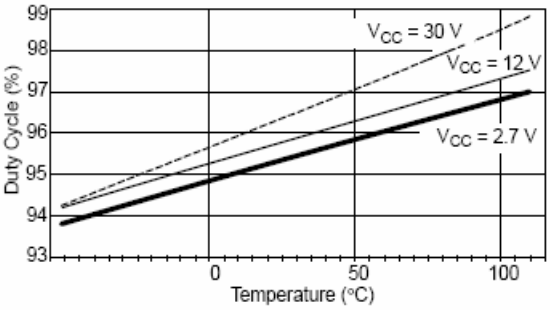



Figure 10. Maximum Duty Cycle vs. Temperature

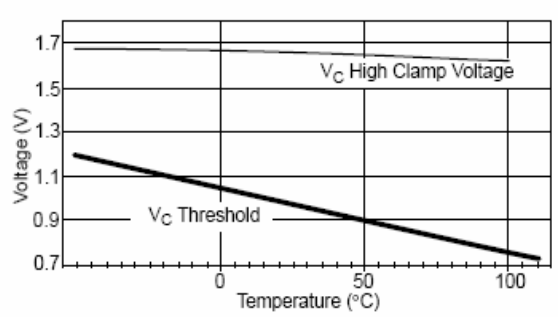



Figure 11. $V_C$ Threshold and High Clamp Voltage vs. Temperature

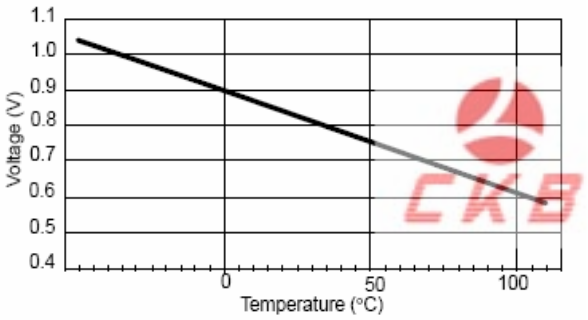



Figure 12. Shutdown Threshold vs. Temperature

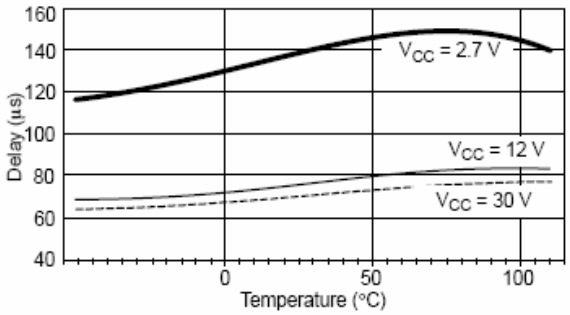



Figure 13. Shutdown Delay vs. Temperature

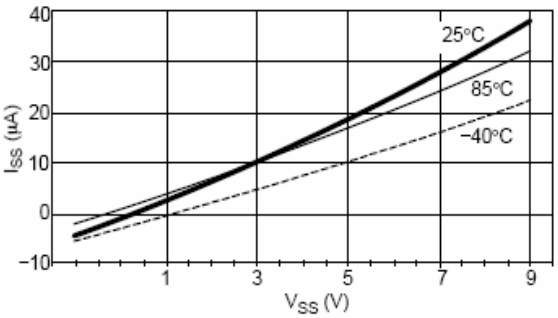



Figure 14. $I_{SS}$ vs. $V_{SS}$

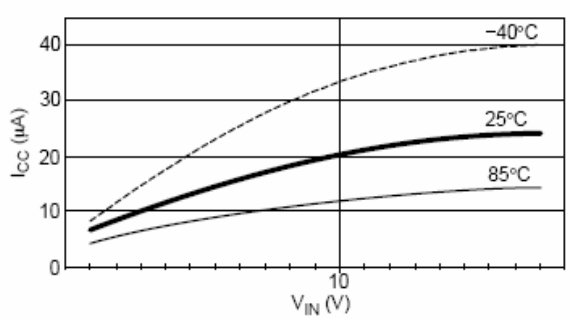



Figure 15. $I_{CC}$ vs. $V_{IN}$ During Shutdown

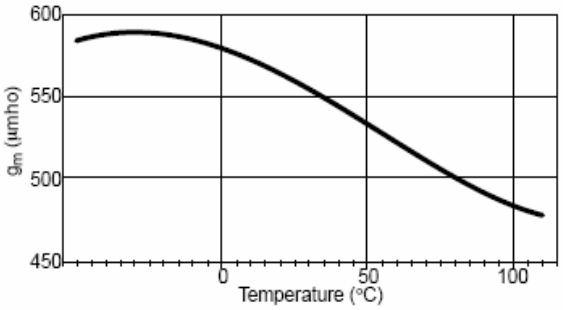



Figure 16. Error Amplifier Transconductance vs. Temperature

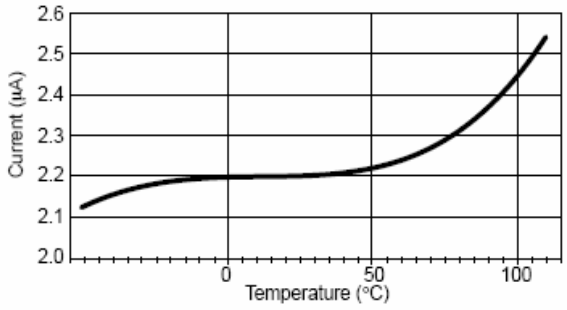



Figure 17. Switch Leakage vs. Temperature

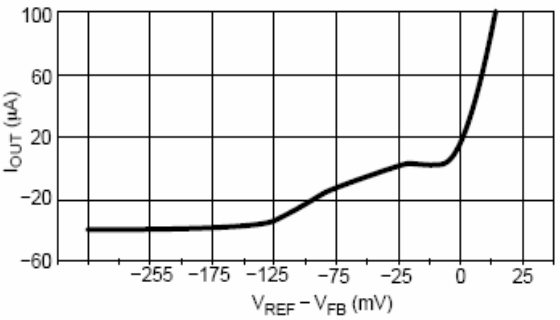



Figure 18. Error Amplifier $I_{OUT}$ vs. $V_{FB}$

## THEORI of OPERATION：Current Mode Control

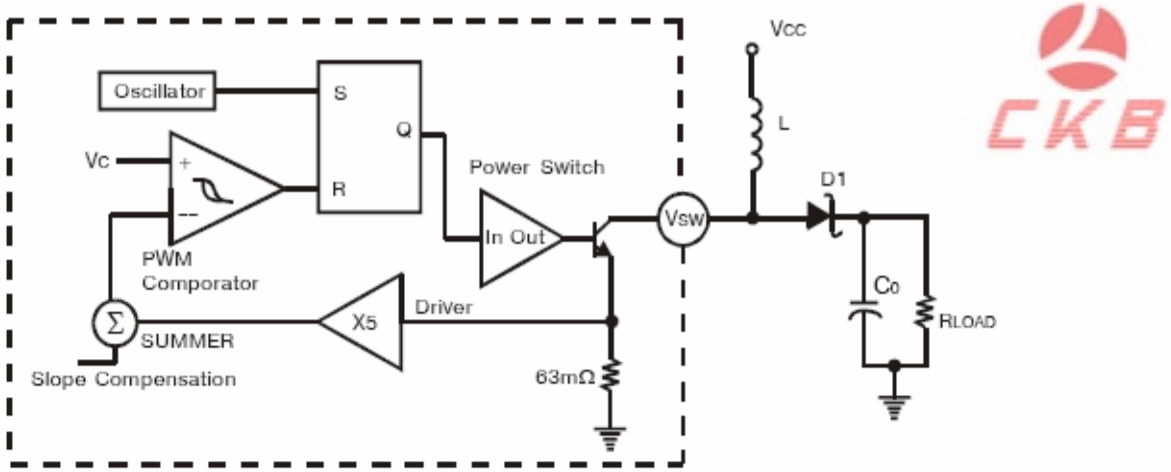



**Figure 19. Current Mode Control Scheme**

The LM5171 is a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on–time of the power switch. The oscillator is used as a fixed–frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse–by–pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both a simpler compensation and a higher gain–bandwidth over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problems, mainly, subharmonic oscillation at duty cycles over 50%. The LM5171 solves this problem by adopting a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

## Oscillator and Shutdown

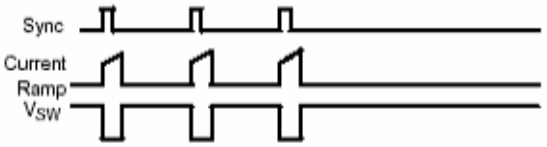



**Figure 20. Timing Diagram of Sync and Shutdown**

The oscillator is trimmed to guarantee an 18% frequency accuracy. The output of the oscillator turns on the power switch at a frequency of 280 kHz, as shown in Figure 1. The power switch is turned off by the output of the PWM Comparator.

A TTL–compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in Figure 2, in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator goes high, thereby resetting the oscillator. The sync operation allows multiple power supplies to operate at the same frequency.

A sustained logic low at the SS pin will shut down the IC and reduce the supply current.

An additional feature includes frequency shift to 20% of the nominal frequency when the FB pin trigger the threshold. During power up, overload, or short circuit conditions, the minimum switch on–time is limited by the PWM comparator minimum pulse width. Extra switch off–time reduces the minimum duty cycle to protect external components and the IC itself.

As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

## Error Amplifier

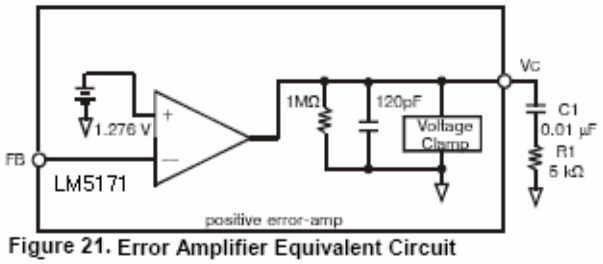



**Figure 21. Error Amplifier Equivalent Circuit**

The FB pin is directly connected to the inverting input of the positive error amplifier, whose non–inverting input is fed by the 1.276 V reference. The amplifier is transconductance amplifier with a high output impedance of approximately 1 MΩ, as shown in Figure 3. The $V_C$ pin is connected to the output of the error amplifiers and is internally clamped between 0.5 V and 1.7 V. A typical connection at the $V_C$ pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.

An external shunt can be connected between the $V_C$ pin and ground to reduce its clamp voltage.

Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

## Switch Driver and Power Switch

The switch driver receives a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors (63 mΩ total) to the PGND pin. PGND is not connected to the IC substrate so that switching noise can be isolated from the analog ground. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 1.5 A and varies with duty cycle due to slope compensation. The power switch can withstand a maximum voltage of 40 V on the collector ($V_{SW}$ pin). The saturation voltage of the switch is typically less than 1 V to minimize power dissipation.

## Short Circuit Condition

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don't have the means to limit load current, an external current limit circuit such as a fuse or relay) has to be implemented to protect the load, power supply and ICs.

In other topologies, the frequency shift built into the IC prevents damage to the chip and external components. This feature reduces the minimum duty cycle and allows the transformer secondary to absorb excess energy before the switch turns back on.

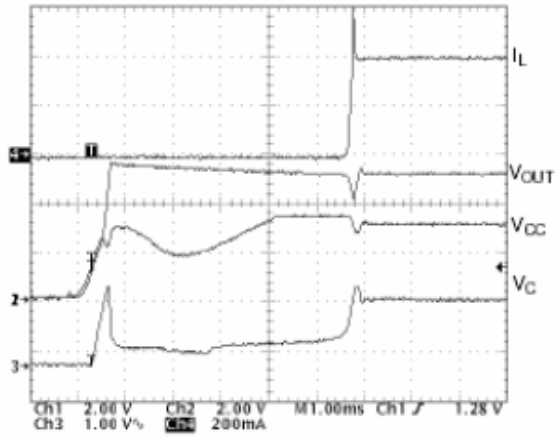



**Figure 22. Startup Waveforms of Circuit Shown in the Application Diagram.**
**Load = 400 mA.**

The LM5171 can be activated by either connecting the $V_{CC}$ pin to a voltage source or by enabling the SS pin. Startup waveforms shown in Figure 4 are measured in the boost converter demonstrated in the Application Diagram on the page 1 of this document. Recorded after the input voltage is turned on, this waveform shows the various phases during the power up transition.

When the $V_{CC}$ voltage is below the minimum supply voltage, the $V_{SW}$ pin is in high impedance. Therefore, current conducts directly from the input power source to the output through the inductor and diode. Once $V_{CC}$ reaches approximately 1.5 V, the internal power switch briefly turns on. This is a part of the LM5171 normal operation. The turn–on of the power switch accounts for the initial current swing.

When the $V_C$ pin voltage rises above the threshold, the internal power switch starts to switch and a voltage pulse can be seen at the $V_{SW}$ pin. Detecting a low output voltage at the FB pin, the built–in frequency shift feature reduces the switching frequency to a fraction of its nominal value, reducing the minimum duty cycle, which is otherwise limited by the minimum on–time of the switch. The peak current during this phase is clamped by the internal current limit.

When the FB pin voltage rises above 0.4 V, the frequency increases to its nominal value, and the peak current begins to decrease as the output approaches the regulation voltage. The overshoot of the output voltage is prevented by the active pull–on, by which the sink current of the error amplifier is increased once an overvoltage condition is detected. The overvoltage condition is defined as when the FB pin voltage is 50 mV greater than the reference voltage.

# COMPONENT SELECTION

## Frequency Compensation

The goal of frequency compensation is to achieve desirable transient response and DC regulation while ensuring the stability of the system. A typical compensation network, as shown in Figure 5, provides a frequency response of two poles and one zero. This frequency response is further illustrated in the Bode plot shown in Figure 6.

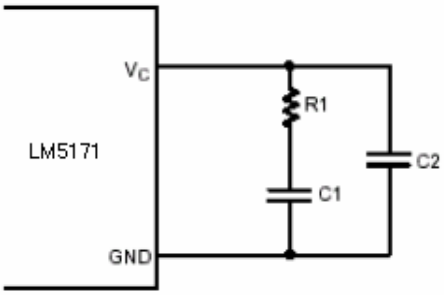



**Figure 23. A Typical Compensation Network**

The high DC gain in Figure 6 is desirable for achieving DC accuracy over line and load variations. The DC gain of a transconductance error amplifier can be calculated as follows:

$$Gain_{DC} = G_M \times R_0$$

where:
$G_M$ = error amplifier transconductance;
$R_0$ =error amplifier output resistance ≈1MΩ.

The low frequency pole, $f_{P1}$, is determined by the error amplifier output resistance and C1 as:

$$f_{P1} = \frac{1}{2\pi C1 R_0}$$

The first zero generated by C1 and R1 is:

$$f_{Z1} = \frac{1}{2\pi C1 R1}$$

The phase lead provided by this zero ensures that the loop has at least a 45° phase margin at the crossover frequency. Therefore, this zero should be placed close to the pole generated in the power stage which can be identified at frequency:

$$f_P = \frac{1}{2\pi C_0 R_{LOAD}}$$

where:
$C_0$ = equivalent output capacitance of the error amplifier ≈120pF;
$R_{LOAD}$= load resistance.

The high frequency pole, $f_{P2}$, can be placed at the output filter's ESR zero or at half the switching

frequency. Placing the pole at this frequency will cut down on switching noise. The frequency of this pole is determined by the value of C2 and R1:

$$f_{P2} = \frac{1}{2\pi C2R1}$$

One simple method to ensure adequate phase margin is to design the frequency response with a –20 dB per decade slope, until unity–gain crossover. The crossover frequency should be selected at the midpoint between $f_{z1}$ and $f_{P2}$ where the phase margin is maximized.

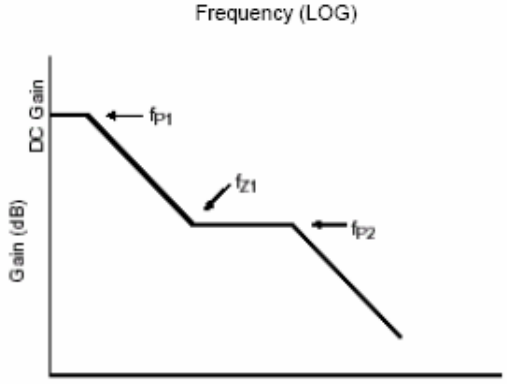



**Figure 24. Bode Plot of the Compensation Network Shown in Figure 23.**

## $V_{SW}$ Voltage Limit

In the boost topology, $V_{SW}$ pin maximum voltage is set by the maximum output voltage plus the output diode forward voltage. The diode forward voltage is typically 0.5V for Schottky diodes and 0.8V for ultrafast recovery diodes

$$V_{SW(MAX)}=V_{OUT(MAX)}+V_F$$

where:

$V_F$ = output diode forward voltage.

In the flyback topology, peak VSW voltage is governed by:

$$V_{SW(MAX)}=V_{CC(MAX)}+(VOUT+V_F)xN$$

where:

N = transformer turns ratio, primary over secondary.

When the power switch turns off, there exists a voltage spike superimposed on top of the steady–state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the $V_{SW}$ and PGND pins. To prevent the voltage at the $V_{SW}$ pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the $V_{SW}$ pin and ground.

## Magnetic Component Selection

When choosing a magnetic component, one must consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is the product of output current and voltage gain ($V_{OUT}/V_{CC}$), assuming 100% energy transfer efficiency. In continuous conduction mode, inductor ripple current is

$$I_{RIPPLE} = \frac{V_{CC}(V_{OUT}-V_{CC})}{(f)(L)(V_{OUT})}$$

where:

f=280 kHz.

The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced when selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. A core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometries, such as toroids, provide a closed magnetic loop to prevent EMI.

## Input Capacitor Selection

In boost circuits, the inductor becomes part of the input filter, as shown in **Figure 26**. In continuous mode, the input current waveform is triangular and does not contain a large pulsed current, as shown in **Figure 25**. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. As we can see from **Figure 25** the product of the inductor current ripple and the input capacitor's effective series resistance (ESR) determine the $V_{CC}$ ripple. In most applications, input capacitors in the range of 10 µF to 100 µF with an ESR less than 0.3 Ω work well up to a full 1.5 A switch current.


**Figure 25. Boost Input Voltage and Current Ripple Waveforms**

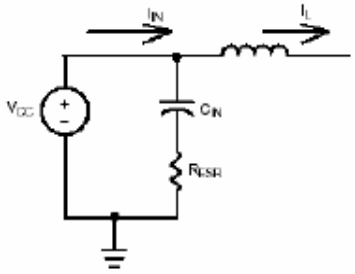



**Figure 26. Boost Circuit Effective Input Filter**

The situation is different in a flyback circuit. The input current is discontinuous and a significant pulsed current is seen by the input capacitors. Therefore, there are two requirements for capacitors in a flyback regulator: energy storage and filtering. To maintain a stable voltage supply to the chip, a storage capacitor larger than 20 µF with low ESR is required. To reduce the noise generated by the inductor, insert a 1.0 µF ceramic capacitor between $V_{CC}$ and ground as close as possible to the chip.

By examining the waveforms shown in Figure 9, we can see that the output voltage ripple comes from two major sources, namely capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off, $I_L$ flows into the output capacitor causing an instant $\Delta V = I_{IN} \times ESR$. At the same time, current $I_L - I_{OUT}$ charges the capacitor and increases the output voltage gradually.

## Output Capacitor Selection


Figure 27. Typical Output Voltage Ripple

$$V_{OUT(RIPPLE)} = \frac{(I_{IN} - I_{OUT})(1-D)}{(C_{OUT})(f)} + \frac{I_{OUT}D}{(C_{OUT})(f)} + I_{IN} \times ESR$$

The equation can be expressed more conveniently in terms of $V_{CC}$, $V_{OUT}$ and $I_{OUT}$ for design purposes as follows:

$$V_{OUT(RIPPLE)} = \frac{I_{OUT}(V_{OUT} - V_{CC})}{(C_{OUT})(f)} \times \frac{1}{(C_{OUT})(f)} + \frac{(I_{OUT})(V_{OUT})(ESR)}{V_{CC}}$$

The capacitor RMS ripple current is:

$$I_{RIPPLE} = \sqrt{(I_{IN} - I_{OUT})^2(1-D) + (I_{OUT})^2(D)} = I_{OUT}\sqrt{\frac{V_{OUT} - V_{CC}}{V_{CC}}}$$

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

## Reducing the Current Limit

In some applications, the designer may prefer a lower limit on the switch current than 1.5 A. An external shunt can be connected between the $V_C$ pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

The voltage on the $V_C$ pin can be evaluated with the equation

$$V_C = I_{SW} R_E A_V$$

where:

$R_E$= 0.063Ω, the value of the internal emitter resistor;

$A_V$=5 V/V, the gain of the current sense amplifier.

Since $R_E$ and $A_V$ cannot be changed by the end user, the only available method for limiting switch current below 1.5 A is to clamp the $V_C$ pin at a lower voltage. If the maximum switch or inductor current is substituted into the equation above, the desired clamp voltage will result.

A simple diode clamp, as shown in **Figure 28.** clamps the $V_C$ voltage to a diode drop above the voltage on resistor R3. Unfortunately, such a simple circuit is not generally acceptable if $V_{IN}$ is loosely regulated.

Another solution to the current limiting problem is to externally measure the current through the switch using a sense resistor. Such a circuit is illustrated in **Figure 29.**

The switch current is limited to

$$I_{SWITCH(PEAK)} = \frac{V_{BE(Q1)}}{R_{SENSE}}$$

where:

$V_{BE(Q1)}$=the base–emitter voltage drop of Q1, typically 0.65V.

When the power switch is turned on, $I_L$ is shunted to ground and $I_{OUT}$ discharges the output capacitor. When the $I_L$ ripple is small enough, $I_L$ can be treated as a constant and is equal to input current $I_{IN}$. Summing up, the output voltage peak–peak ripple can be calculated by:

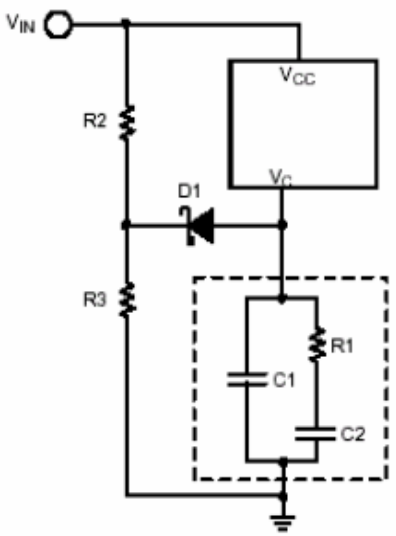



Figure 28. Current Limiting using a Diode Clamp

The improved circuit does not require a regulated voltage to operate properly. Unfortunately, a price must be paid for this convenience in the overall efficiency of the circuit. The designer should note that the input and output grounds are no longer common. Also, the addition of the current sense resistor, $R_{SENSE}$, results in a considerable power loss which increases with the duty cycle. Resistor R2 and capacitor C3 form a low–pass filter to remove noise.

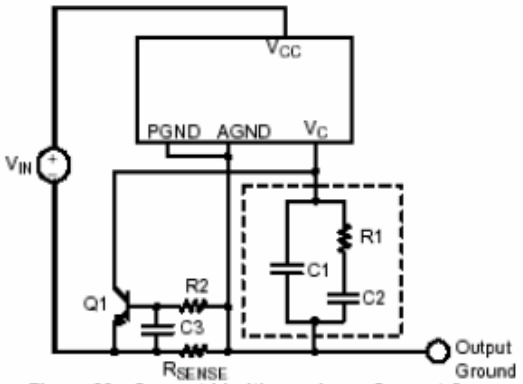



Figure 29. Current Limiting using a Current Sense Resistor

## Subharmonic Oscillation

Subharmonic oscillation (SHM) is a problem found in current–mode control systems, where instability results when duty cycle exceeds 50%. SHM only occurs in switching regulators with a continuous inductor current. This instability is not harmful to the converter and usually does not affect the output voltage regulation. SHM will increase the radiated EM noise from the converter and can cause, under certain circumstances, the inductor to emit high–frequency audible noise.

SHM is an easily remedied problem. The rising slope of the inductor current is supplemented with internal "slope compensation" to prevent any duty cycle instability from carrying through to the next switching cycle. In the LM5171, slope compensation is added during the entire switch on–time, typically in the amount of 180 mA/µs.

In some cases, SHM can rear its ugly head despite the presence of the onboard slope compensation. The simple cure to this problem is more slope compensation to avoid the unwanted oscillation. In that case, an external circuit, shown in Figure 40, can be added to increase the amount of slope compensation used. This circuit requires only a few components and is "tacked on" to the compensation network.

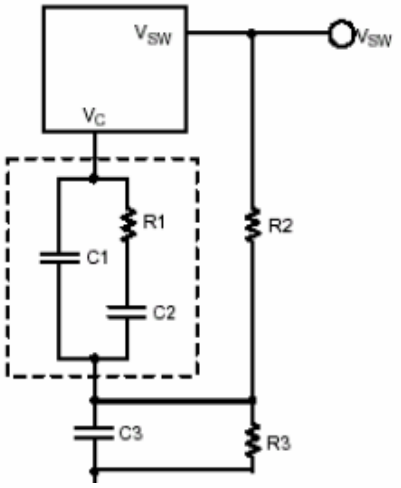



Figure 30. Technique for Increasing Slope Compensation

The dashed box contains the normal compensation circuitry to limit the bandwidth of the error amplifier. Resistors R2 and R3 form a voltage divider off of the $V_{SW}$ pin. In normal operation, $V_{SW}$ looks similar to a square wave, and is dependent on the converter topology. Formulas for calculating $V_{SW}$ in the boost and flyback topologies are given in the section "$V_{SW}$ Voltage Limit." The voltage on $V_{SW}$ charges capacitor C3 when the switch is off, causing the voltage at the $V_C$ pin to shift upwards. When the switch turns on, C3 discharges through R3, producing a negative slope at the $V_C$ pin. This negative slope provides the slope compensation.

The amount of slope compensation added by this circuit is

$$\frac{\Delta I}{\Delta T} = V_{SW}\left(\frac{R_3}{R_2+R_3}\right)\left(1-e^{\frac{-(1-D)}{R_3C_3f_{SW}}}\right)\left(\frac{f_{SW}}{(1-D)R_E A_V}\right)$$

where:

$\Delta I/\Delta T$ = the amount of slope compensation added (A/s);
$V_{SW}$ = the voltage at the switch node when the transistor is turned off (V);
$f_{SW}$ = the switching frequency, typically 280 kHz;
D = the duty cycle;
$R_E$ = 0.063 Ω, the value of the internal emitter resistor;
$A_V$ = 5 V/V, the gain of the current sense amplifier.

In selecting appropriate values for the slope compensation network, the designer is advised to choose a convenient capacitor, then select values for R2 and R3 such that the amount of slope compensation added is 100 mA/µs. Then R2 may be increased or decreased as necessary. Of course, the series combination of R2 and R3 should be large enough to avoid drawing excessive current from $V_{SW}$. Additionally, to ensure that the control loop stability is *improved*, the time constant formed by the additional components should be chosen such that

$$R_3C_3 \langle \frac{1-D}{f_{SW}}$$

Finally, it is worth mentioning that the added slope compensation is a trade–off between duty cycle stability and transient response. The more slope compensation a designer adds, the slower the transient response will be, due to the external circuitry interfering with the proper operation of the error amplifier.

## Soft Start

Through the addition of an external circuit, a soft–start function can be added to the CS5171. Soft–start circuitry prevents the $V_C$ pin from slamming high during startup, thereby inhibiting the inductor current from rising at a high slope.

This circuit, shown in Figure 13, requires a minimum number of components and allows the soft–start circuitry to activate any time the SS pin is used to restart the converter.

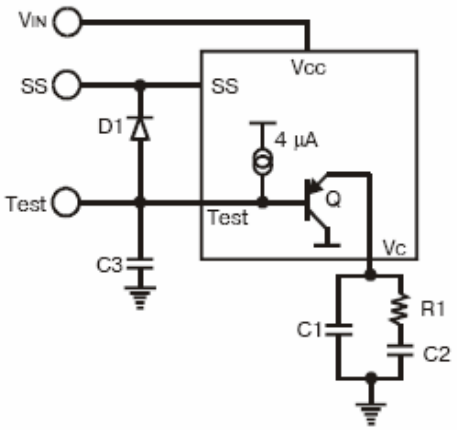



Figure 31. Soft Start

Resistor R1 and capacitors C1 and C2 form the compensation network. At turn on, the voltage at the $V_C$ pin starts to come up, charging capacitor C3 through transistor Q, clamping the voltage at the $V_C$ pin such that switching begins when $V_C$ reaches the VC threshold, typically 1.05 V.

Therefore, C3 slows the startup of the circuit by limiting the voltage on the $V_C$ pin. The soft–start time increases with the size of C3.

Diode D1 discharges C3 when SS is low. If the shutdown function is not used with this part, the cathode of D1 should be connected to $V_{IN}$.

## Calculating Junction Temperature

To ensure safe operation of the LM5171, the designer must calculate the on–chip power dissipation and determine its expected junction temperature. Internal thermal protection circuitry will turn the part off once the junction temperature exceeds 180°C±30°. However, repeated operation at such high temperatures will ensure a reduced operating life.

Calculation of the junction temperature is an imprecise but simple task. First, the power losses must be quantified. There are three major sources of power loss on the LM5171:

- biasing of internal control circuitry, $P_{BIAS}$
- switch driver, $P_{DRIVER}$
- switch saturation, $P_{SAT}$

The internal control circuitry, including the oscillator and linear regulator, requires a small amount of power even when the switch is turned off. The specifications section of this datasheet reveals that the typical operating current, $I_Q$, due to this circuitry is 5.5mA. Additional guidance can be found in the graph of operating current vs. temperature. This graph shows that $I_Q$ is strongly dependent on input voltage, $V_{IN}$, and the ambient temperature, $T_A$. Then

$$P_{BIAS}=V_{IN}I_Q$$

Since the onboard switch is an NPN transistor, the base drive current must be factored in as well. This current is drawn from the $V_{IN}$ pin, in addition to the control circuitry current. The base drive current is listed in the specifications as $\Delta I_{CC}/\Delta I_{SW}$, or switch transconductance. As before, the designer will find additional guidance in the graphs. With that information, the designer can calculate

$$P_{DRIVER} = V_{IN} I_{SW} \times \frac{I_{CC}}{\Delta I_{SW}} \times D$$

where:
$I_{SW}$=the current through the switch;
D=the duty cycle or percentage of switch on–time.

$I_{SW}$ and D are dependent on the type of converter. In a boost converter,

$$I_{SW(AVG)} \cong I_{LOAD} \times D \times \frac{1}{Efficiency}$$

$$D \cong \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

In a flyback converter,

$$I_{SW(AVG)} \cong \frac{V_{OUT} I_{LOAD}}{V_{IN}} \times \frac{1}{Efficiency}$$

$$D \cong \frac{V_{OUT}}{V_{OUT} + \frac{N_S}{N_P} V_{IN}}$$

The switch saturation voltage, $V_{(CE)SAT}$, is the last major source of on–chip power loss. $V_{(CE)SAT}$ is the collector–emitter voltage of the internal NPN transistor when it is driven into saturation by its base drive current. The value for $V_{(CE)SAT}$ can be obtained from the specifications or from the graphs, as "Switch Saturation Voltage." Thus,

$$P_{SAT} \cong V_{(CE)SAT} I_{SW} \times D$$

Finally, the total on–chip power losses are

$$P_D = P_{BIAS} + P_{DRIVER} + P_{SAT}$$

Power dissipation in a semiconductor device results in the generation of heat in the junctions at the surface of the chip. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the resistive properties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturers' data sheets as $\Theta_{JA}$, or junction–to–ambient thermal resistance. The on–chip junction temperature can be calculated if $\Theta_{JA}$, the air temperature near the surface of the IC, and the on–chip power dissipation are known.

$$T_J = T_A + (P_D \Theta_{JA})$$

where:
$T_J$ = IC or FET junction temperature (°C);
$T_A$ = ambient temperature (°C);
$P_D$ = power dissipated by part in question (W);
$\Theta_{JA}$ = junction–to–ambient thermal resistance (°C/W). For the LM5171 $\Theta_{JA}$=165°C/W.

Once the designer has calculated $T_J$, the question whether the LM5171 can be used in an application is settled. If $T_J$ exceeds 150°C, the absolute maximum allowable junction temperature, the LM5171 is not suitable for that application.

If $T_J$ approaches 150°C, the designer should consider possible means of reducing the junction temperature. Perhaps another converter topology could be selected reduce the switch current. Increasing the airflow across the surface of the chip might be considered to reduce $T_A$.

## Circuit Layout Guidelines

In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents combined with trace inductance generates voltage transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on–chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on–chip power transistor, while the transformer, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.
2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best results.
3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.