Quartus II 用户指南











- 多种设计输入方法
 - Quartus II
 - 原理图式图形设计输入
 - 文本编辑
 - AHDL, VHDL, Verilog
 - 内存编辑
 - Hex, Mif
 - 第三方工具
 - EDIF
 - HDL
 - VQM
 - 或采用一些别的方法去优化和提高输入的灵活性:
 - 混合设计格式
 - •利用LPM和宏功能模块来加速设计输入



设计输入文件



该编辑器既可以编辑图表模块,又可以编辑原理图

- ■图表模块编辑是主要的顶层设计的主要方法
- 原理图编辑是传统的设计输入方法
- 用户可以利用加入Quartus II 提供的LPMs, 宏功能等涵数 以及用户自己的库涵数来设计
- 提供"智能"的模块链接和映射



图表模块 - 设计流程

- 产生一个新的模块设计文件
 - 画出图表模块或输入设计单元符号
 - 输入接口和参数信息
 - 连接各个设计单元(利用单连线,总线等)
- 保存设计
 - 文件的后缀名为 .bdf
- 顶层模块可以是用户产生的HDL文件或图形编辑文件
- 人顶层设计可以产生设计单元,头文件,或转化成 Verilog/VHDL文件



模块编辑器 – 产生一个新的文件







■ 从工具栏中产生模块和输入端口





模块编辑器-"智能"连接

Quartus II 有 "智能" 模块连接和映射

- 如果连接不同模块时,两边端口的名字相同的话就不用标注出来
- 一个管道可以连接模块之间所有的普通 I/O





模块编辑器-产生设计文件





综合工具

Leonardo Spectrum* Design Compiler FPGA Compiler II Standard* & Altera Edition* FPGA Express* Synplicity Synplify*

仿真工具

- ModelSim*
- •ModelSim OEM*
- •Cadence Verilog-XL
- Innoveda BLAST
- •PrimeTime*
- •Synopsys VCS
- •Synopsys VSS

Quartus II 驱动流程

| Project > EDA Tool Settings | EDA Tool Settings |
|--|--|
| 当选择内部链接的EDA工具,会自动产 生ATOM 网表,并且会自动选择数据格 式 | Specify the other EDA tools in additon to Quartus that you will use on this project. You can specify other companies' tools for design entry, synthesis, simulation, or timing analysis. Design entry/synthesis tool: Mou can override this setting for an individual design file with the File Properties command) Synplify Generate a compilable netlist automatically from the source files when they change |
| EDA Tool Input Settings Options for processing input files created by other Design entry/synthesis tool: Data format: Verilog HDL Signal names VCC: VCC GND: | er EDA tools. |
| Library Mapping File File name: synplcty.lmf Show information messages describing LM OK Cancel | IF mapping during compilation Reset |

EDA 驱动流程

文件驱动流程:非内部链接

如果用一个非内部链接的 EDA 工具产生 VHDL, Verilog, EDIF 文件, 就需要阐明 .lmf 文件来给定文件格式 可以是 EDIF,

VHDL, or Verilog 菜单Project > EDA Tool 选择自定义 Settings... 选择库涵数映射文 选择设置... 件 (Imf) EDA Tool Settings X Specify the other EDA tools -- in addition to Quartus -- that you will use on this project. You EDA Tool Input Settings X can specify other companies' tools for design entry, synthesis, signalation, or timing analysis. Options for processing input files created by other EDA tools. Design entry/synthesis tool: [You can override this setting for an individual design file with the File Properties command] Design entry/synthesis tool: Custom Settings. Custom EDIF Data format: Generate a compilable netlist automatically from the source files when they change Signal names Simulation tool: IVCC. VCC: None> \mathbf{T} GND GND: Run this tool automatically after compilation Library Mapping File Timing analysis tool: File <u>n</u>ame: ÷. <None> Show information messages describing LMF mapping during compilation Run this tool automatically after compilation 0K Cancel 0K Cancel Reset

项目菜单

- ■编辑项目的设置t
 - 增加/去除文件或库涵数
- 项目设置
 - HDL 类型界面
 - 第三方EDA工具设计流程
 - 定时设置
 - 版本控制

<u>注意:</u>

所有的项目设置中,除了项目名和顶层设计名不一样之外,其它的设置都保留上一个项目的设置

编辑项目设置

■ 改变项目的名字或顶层设计的名字

| 🖞 Quartus II - C:\qdesignsll\tutorial\fir_filte | ii da an | General Settings | | × |
|---|---|---|---|--|
| Elle View Project Processing Looks Window | Heb . | | · · · · · | |
| 🗅 😅 Project <u>W</u> izard | 🐼 🐦 🕨 🕷 🗉 filtref | General Add Files Use | r Libraries VHDL Input Ve | erilog HDL Input Toolset Directories |
| Add Current Fire to Project | | Project name: Project directory: | fir_filter C:\qdesignsll\tutorial\ | Rename |
| Archive Project Restore Archived Project | | Top-level design entity: | filtref Note: you can add more to <u>and Simulato</u> r settings for th | p-level entities and create Compiler nem with commands on the |
| Construction of the second secon | Rename Project / Top-Level Entity Enter the new project and an optional top-la rename a project within the same directory. database information from previous compila need to change the top-level entity name in entity. You can use the Compiler or Simulation help you compile or simulate any entity in you current project name: Current project name: filtref New groject name: filtref | evel entity name. Note: You ca Renaming a project will delete tions and simulations, if any. Y norder to compile or simulate a or Settings Wizard (Processing our project. | an only e the 'ou do not a different g menu) to | 点击Rename 按钮 去改变项目的名字 或顶层设计的名字 |
| Mode | New <u>t</u> op-level entity name: | current project name | | |

编辑项目设置

Quartus II 编译

编译设置指南

| s\qua | rtus\Designing_with_Quartus\Lab5\filtret Processing Insert Tools Window Help • Compile Mode Simulate Mode Simulate Mode Start Analysis & Elaboration Start Analysis & Elaboration Start Compilation Start Timing Analysis Stop Processing Compiler Settings Compiler Settings Wizard | - [filtref.bdf] Ctrl+K Ctrl+L Ctrl+Shift+L Ctrl+Scroll Lock | Compiler Settings V Which entity do yo specifying a top-lex specifying a lower- entity, include its fu <u>Focus point</u> Which Compiler se new settings, or se using a name that i Settings name: | Vizard: Entity and Settings Names u want to compile? You can compile a or rel design entity name, or compile only a level entity, as the "focus point." If you to all hierarchical pathname. Inel tings do you wish to edit? You can type lect an existing name from the drop-down includes the focus point name. Tref | (page 1 of 6) | |
|-------|--|---|---|---|--------------------|-------|
| | Set Compilation Focus to Current Entity Add Current Entity at Top Level & Set Focus Compiler Settings Wizard: Comp Which type of compilation do you C Netist extraction and cynthesis Full compilation, including neti- will generate actual timing value What are your goals for compilation (C Normal completion/less data a | Ctrl+J Ctrl+Shift+J ilation Mode (page 2 of want to perform? is only. ist extraction, synthesis, and uss and programming lifes, on speed versus disk space space. | 6 × | <u><</u> gerk <u>N</u> ewt > ! | 指定编译模 字 | 快及设定名 |
| | Smart compilation/more disk a make future re-compilation: ru re-compilation. Do you want to save disk space b when you enter assignments, sime Yes No | pace. The Compiler will say in faster and to support futur by reducing the number of m date, etc.? Next > Ein | e extra data to e incremental ode names available ish <u>Cancel</u> | •网表输出或完 •优化速度或资 •削减接点名字 | 全编译? 源利用率? ? | |
| C | 2001 Altera [®] Corporation | | | | | |

编译设置指南

| Compiler Settings Wizard: Device Family (page 3 of 6) Which device family do you wish to target? Eamly: AFEX20KE Do you want to assign a specific device? If Yes Image: More than to allow the Compiler to choose a device | Compiler Settings Wizard: Select a Target Device [page 4 of 6] X Use the Filters settings to control the devices that are displayed in the "Available devices" list. Select a device in the list, and click. Next to continue. Available devices: Available devices: Filters EP20K100EFC144-2 Beckage: EP20K100EFC144-3 Pin gount: EP20K100EQC208-1X Pin gount: EP20K100EQC208-2X Speed grade: EP20K100EQC208-2X Voltage: EP20K100EQC208-2X Speed grade: |
|--|---|
| 自动选择或给定器件? 《Eack Nest》 Do you want to run standard to ⑦ Teal ⑦ No Do you want to run a batch sin ⑦ No | EP20K100EQC20B3 EP20K100EQC20B3 EP20K100EQC20B3 EP20K100EQC20D3 EP20K100EQC20D2X EP20K100EQC20D3X Iming analyses at the end of compilation? •运行延时分析? •运行近时分析? •运行位真? |
| © Yes, use these previously i fither © 2001 Altera® Corporation | saved Simulator settings: |

■ 编译类型

- 只是综合并输出网表
 - •编译设计文件,综合产生门级代码
 - •编译器只运行到综合这步就停止了
 - 编译器只产生估算的延时数值
- 完全的编译,包括编译,网表输出,综合,配置器件
 - •编译器除了完成以上的步骤,还要将设计配置到ALTERA的器件 中去
 - 编译器根据器件特性产生真正的延时时间和给器件的配置文件

编辑编译选项

编译设置 - 芯片和器件

| Compiler Settings | C Device & Pin Options |
|--|--|
| General Chips & Devices Mode Synthesis & Fitting Verification | General Configuration Programming Files Unused Pins Dual-Purpose Pins Voltage |
| Select the family and device you want to target for compilation. | Specify general device options. These options are not dependent on the configuration scheme. |
| Changes apply to Compiler settings 'rfifo' | Changes apply to Compiler settings 'filtref' |
| Chip <u>n</u> ame: Ififo | Options: |
| Family: APEX20K ▼ Device & Pin <u>O</u> ptions | Release clears before tri-states Each (CLKUSE) |
| | Enable device-wide reset (DEV_CLRn) |
| C Auto devices selected by the Compiler from the 'Ausilable devices' list | Enable device-wide output enable (DEV_OE) |
| | Enable INIT_DONE output |
| Specific device selected in 'Available devices' list Assign Pins | |
| Available <u>d</u> evices: Show in 'Available devices' list | JTAG user code (32-bit hexadecimal) FFFFFFFF |
| EP20K100TC144-3 Package: Any | Description |
| EP20K100TC144-2 EP20K100TC144-1 EP20K100TC144-1 Pin <u>c</u> ount: Any | Directs the device to restart the configuration process automatically if a data error is encountered. If this option is turned off, you must externally direct the device to |
| EFF20K1000C240-3 EFF20K1000C240-3 EFF20K1000C240-3 EFF20K1000C240-3 Speed grade: Any | 说明器件和引脚选项 |
| EF 也非命作关望 | │ <mark>●概要</mark> · · · · · · · · · · · · · · · · · · · |
| | ● 配置 |
| OK Cancel Apply | - ●下载文件 |
| | - ●不用的引脚 |
| | ■双种田诠的引脚 |
| | |
| | ●电压值 |

编译设置 - 芯片和器件

| ■ <u>Device & Pin Options</u> 1. 选择引脚号 | | | | | |
|--|---|--|--|--|--|
| the Available device 197 ces' list Assign Bins | 2. 调用引脚查找器去查找引脚名 或类型 | | | | |
| Select a device pin and the type of assignment you with to make. You can also make pin assignments in the Assignment Organizer and the El optian Edicor. You can reserve unused pins on a device-wide basis with the Unused Pins tab in the Device & Pin Options dialog box. Changes apply to Complex settings Titref' Available Pins & Existing Assignments: Nu Name: 1/0 1/0 1/0 1/0 2 3 LVTTL Row 1/0 3 3 LVTTL Row 1/0 3 3 LVTTL Row 1/0 3 LVTTL Row 1/0 6 3 LVTTL Row 1/0 3 LVTTL Row 1/0 8 3 LVTTL Row 1/0 Row 1/0 Row 1/0 Row 1/0 | 3. 增加到指定列表 Node Field | | | | |
| 9 3 LVTTL Row I/O 3 LVTTL Row I/O 9 Show 'no connect' pins Assignment Pin game: | Image: Construction of the second | | | | |

| Compiler Settings | APEX™ 配置器: |
|---|---|
| Specify options for logic synthesis and fitting. These options apply to all logic within the entity that is the current compilation focus. Note: The availability of some options depends on the current device family. Changes apply to Compiler settings 'filtref' APEX Fitter APEX Fitter Advanced PowerFit Fitter (better fmax and compilation time) Standard Fitter (required if design contains product terms) | PowerFit配置器 更好的Fmax和编译时间 对打包(Cliques)有限制 标准配置器 PTERM 模式 |
| Timing-driven compilation Optimize [/O timing Optimize internal timing Normal compilation | 定时驱动式编译: •优化 I/O 引脚的延时 •优化内部的延时 |
| OK Cancel Apply | |

Quartus II 编译界面(开始)

Quartus II 编译

配置组织器的构成

■ 定位

■ 定时

- 增加定时设置来提高特性
- 打包
 - 将选择好的逻辑模块放在一起来提高性能
- I/O 标准
- 局部走线
- 单独的逻辑选项
 - 利用Quartus II 的综合/配置的特殊选项,或ALTERA的器件特性s
 - 3 种类型
- 有参数限制的仿真

编译报告

■ 包含了怎样将一个设计放到一个器件中的所有信息

- 器件使用统计
- 编译设置
- 底层显示
- 器件资源利用率
- 状态机的实现
- 方程式
- 延时分析结果
- CPU 使用资源
- 这是一个只读的窗口

Quartus II 的延时分析

特点

- Quartus II 支持对单个时钟或多个时钟的延时分析
- 单个时钟的延时分析
 - Fmax (最大时钟频率)
 - Tsu, Th, Tco (建立时间, 保持时间, 时钟到输出时间)
 - 整个系统的Fmax (包括引脚上的输入输出延时)
- 多个时钟的延时分析
 - 可以支持客户分析由不同时钟控制的寄存器之间的延时
 - 运用Slack进行分析
- 组合逻辑电路检测
 - Quartus II 会自动检测组合逻辑电路

特点

■ 不同类型的延时信息 (请参考编译部分)

- 没有布局步线的延时信息
- 经过布局步线的延时信息
- 混合的树状层次型设计
- 在缺省情况下,在编译之后一般自动调用延时分析
 - 也可以禁止调用
- 生成的延时信息也可以以VHDL, Verilog 或标准延时文件 (SDF)的格式输出到第三方的EDA工具中

报告延时分析

■ 所有的延时分析信息都包含在编译报告中

- 总结
- 延时分析
- 内部fmax (不包括引脚上的输入输出延时 系统fmax (包括引脚上的输入输出延时)
- 寄存器到寄存器的延时报表
- tsu (输入建立时间)
- th (输入保持时间)
- tco (时钟到输出时间)
- tpd (引脚到引脚的延时)

例如:Fmax (包含输入输出引脚的延时)

| 缺省情况下最坏的 ■ Completion Hierarchies | 内 fmax 放在最上面 | Imax [incl. delays to/from pins] Clock Name Destination Register Name Source Register Name | Required fmax | Actual Imax (period) |
|---|---|---|--|--|
| acc:int4 hvalues:inst3 multinst6 state_minst2 tap:int1 选择 fmax (包 含输入输出引 脚的延时) odule Progress % Time + hocessing Total hocessing Total 100 % 00:0 Initialization 100 % 00:0 Complet Total 100 % 00:0 | Hesuits for "hitref" Complet Settings Complet Settings Complet Settings Prospler View Prospler Prospl | ck input inpu | None None None None None None None None | 37.65 MHz [period = 26.551 ns] 37.65 MHz [period = 25.939 ns] 38.55 MHz [period = 25.932 ns] 37.55 MHz [period = 13.634 ns] 75.53 MHz [period = 13.239 ns] 75.53 MHz [period = 13.237 ns] 75.55 MHz [period = 13.237 ns] 75.55 MHz [period = 13.237 ns] 75.55 MHz [period = 13.237 ns] 75.56 MHz [period = 13.237 ns] 75.57 MHz [period = 13.237 ns] 75.58 MHz [period = 13.237 ns] 75.59 MHz [period = 13.237 ns] 75.56 MHz [period = 13.237 ns] 75.57 MHz [period = 13.237 ns] 75.58 MHz [period = 13.237 ns] 75.59 MHz [period = 13.237 ns] 75 change the limit use Timing Settings |
| Lunic Sunthesizer 1002 000 | | • | | |
| + Micro setup delay of destination Cock clk has System fmax of 37.66 Solution + Longest clock path from clock + Micro clock to output delay of s + Longest register to pin delay is + Longest register to pin delay is + External delay of pin is 20.0 ns | nis 0.159 ns MHz between source register state_minst2filter~19 a clk to source register is 2.770 ns ource is 0.275 ns 3.505 ns | nd designation pin next (period= 26.551 ns) | | |

Quartus II 仿真

支持多种防真方法

- 波形方式输入
 - .vwf (向量波形文件) 是 Quartus II 中最主要的波形文件
 - .vec (向量文件) 是MAX+PLUS II 中的文件. 主要是为了向下兼容
 - .tbl (列表文件) 用来将MAX+PLUS II 中的.scf 文件输入到 Quartus II 中.
- 支持Testbench
 - Tcl/TK 脚本文件
- 第三方的仿真工具
 - Verilog/VHDL Testbench

描绘仿真波形

先选中准备要赋值的部分添入初始值

利用第三方的仿真工具进行仿真

- Model Technology (ModelSim)
- Cadence (VERILOG-XL)
- Synopsys (VCS)
- Synopsys (VSS)

■ 从project 菜单中选择 EDA 工具设置

| | EDA Tool Settings Specify the other EDA tools in addition to Quartus that you will use on this project. You can specify other companies' tools for design entry, synthesis, simulation, or timing analysis. | torial\fir_filter - [filtref Compilation |
|-------|---|---|
| | Design entry/synthesis tool: (You can override this setting for an individual design file with the File Properties command) | P <u>r</u> ocessing <u>T</u> ools <u>W</u> indow <u>H</u> elp iject <u>W</u> izard |
| | Kone> Settings Generate a compilable netlist automatically from the source files when they change Simulation tool: | d Current File to Project d Files to Project load <u>P</u> roject |
| | <none> Settings Settings Settings</none> | :hive Project s <u>t</u> ore Archived Project |
| 择仿真工具 | ModeBim (Verilog HDL output from Quartus) ModelSim DEM (VHDL output from Quartus) ModelSim DEM (Verilog HDL output from Quartus) SpeedWave Run this tool automatically after compilation | en Current Focus Entity Ctrl+E en Selected Entity Ctrl+D en Parent Entity Ctrl+U en Top-Level File in Hierarchy Ctrl+T |
| | OK Cancel | neral Settings ming Settings ming Wizard ption & Parameter Settings DA Tool Settings |
| | Logic Synthesizer | evision Control Settings |

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诜

第三方仿真工具

- VHDL 仿真器
 - 利用 Quartus II 产生.VHO 和 .SDO 文件
 - 利用在sim_lib 目录中的APEX20K_ATOMs.VHD 和 APEX20K_COMPONENTS.VHD 文件
- Verilog 仿真器
 - 利用 Quartus II 产生.VO 和 .SDO
 - 利用在sim_lib APEX20K_ATOMS.VO

Quartus II 下载

打开下载窗口

Processing Open Programmer

| 🎆 Quartus - d: \project | \testing\ram_test | |
|---|--|--------------------------------|
| <u>File</u> <u>E</u> dit <u>V</u> iew <u>P</u> roject | P <u>rocessing</u> <u>D</u> ebug <u>T</u> ools <u>W</u> indow <u>H</u> elp | |
| 🛛 🗅 🖨 🗐 🍯 | • <u>S</u> imulate Mode <u>C</u> ompile Mode | |
| <u> ♥ ⊠ </u> | Initialize Simulation <u>R</u> un Simulation Stop Processing | Ctrl+K Ctrl+L Ctrl+Break |
| | Sjmulator Settings Simulator Settings <u>W</u> izard | |
| | Set Simulation <u>F</u> ocus to Current Entity Add Current Entity at Top Level & Set Focus | Ctrl+J Ctrl+Shift+J |
| 或 使用打开下载快捷 | Open Simulation Report | |
| 方式 | Open Last Compilation Floorplan Open Current Assignments Floorplan <u>B</u> ack-Annotate Assignments Demote Assignments | |
| | Open Last Simulation Vector Outputs Open Current Vector Inputs Overwrite Vector Inputs with Simulation Output | 5 |
| | Purge Simulator Results from <u>D</u> atabase | |
| | Open Programmer | |

| | 远挥Setup进行反直 |
|---|---|
| | |
| data_counters.cdf | |
| Mode: Passive Serial Progress: 0% | Programming Hardware Start Type: No Hardware Stop |
| File Device | Add File |
| 1. d: \training\data_counters.sof EP20K400BC652 | <u>A</u> dd Device |
| Hardware Setup | Remo <u>v</u> e |
| Hardware Type: No Hardware | |
| Port: No Hardware ByteBlaster(MV) | Down |
| Baud rate: | Properties |
| OK I | Cancel |

当你的下载链中的文件与下载电缆已经设置好 了之后,点击开始按钮开始下载

| data_counters.cdf | | | | _ 🗆 🗵 |
|----------------------------------|---------------|---|-------|-----------------------|
| Mode: Passive Serial | ▼ Progress: | 0% Programming Hardware Type: No Hardware | Setup | <u>S</u> tart Stop |
| File | | | | Add File |
| I. d:\training\data_counters.sof | EP20K400BC652 | | | Add Device |
| | | | I | |
| | | | | |
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| | | | | |
| | 进度表中显 | 示目前完成下载的比率 | | |

