PMU FOR PROCESSOR POWER

Check for Samples: TPS659122

1 INTRODUCTION

1.1 Features

- 4 Step-Down Converters:
  - V_{IN} Range From 2.7V to 5.5V
  - Power Save Mode at Light Load Current
  - Output Voltage Accuracy in PWM Mode ±2%
  - Typical 26 µA Quiescent Current per Converter
  - Dynamic Voltage Scaling
  - 100% Duty Cycle for Lowest Dropout
- 10 LDOs:
  - 8 General Purpose LDOs
  - Output Voltage Range 0.8V to 3.3V
  - 2 Low Noise RF-LDOs
  - Output Voltage Range 1.6V to 3.3V
  - 32 µA Quiescent Current
  - Pre-Regulation Support by Separate Power Inputs
  - ECO mode
  - V_{IN} Range of LDOs:
    - 1.8V to 3.6V or
    - 3.0V to 5.5V, respectively
- 3 LED Outputs:
  - Internal Dimming Using I2C
  - Multiplexed with GPIOs
  - Up to 20mA per Current Sink
- Thermal Monitoring
  - High Temperature Warning
  - Thermal Shutdown
- Bypass Switch
  - Used with DCDC4 in Applications Powering an RF-PA
  - As Supply Switch for e.g. SD cards
- Interface
  - I^2C Interface
  - Power I^2C Interface for Dynamic Voltage Scaling
  - SPI
- 32kHz RC Oscillator
- Undervoltage Lockout and Battery Fault Comparator
- Long Button-Press Detection
- Flexible Power-Up and Power-Down Sequencing
- 3.6mm x 3.6mm WCSP Package with 0.4mm pitch

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1.2 Applications

- Data cards
- Smartphones

1.3 Description

The TPS659122 device provides four configurable step-down converters with up to 2.5A output current for memory, processor core, I/O, or pre-regulation of LDOs. It also contains 10 LDO regulators for external usage which can be supplied from either a battery or a pre-regulated supply. Power-up/power-down controller is configurable and can support any power-up/power-down sequences (OTP based). TPS659122 integrate a 32 kHz RC Oscillator to sequence all resources during Power up / down. All LDOs and DCDC converters can be controlled by I2C/SPI interface or Basic ENABLE Balls. In addition, an Independent automatic Voltage Scaling interface allows transitioning DCDC to different voltage by I2C or basic Roof/Floor Control. 3 RGB LED with advanced dimming feature are integrated inside the device. GPIO functionality is multiplexed with LED/ENBLE/SPI when not used. Each GPIO can be configured as part of the Power up sequence to control external resources. One Sleep pin enables power mode control between ACTIVE and pre-programmed SLEEP mode for power optimization. For system control the TPS659122 has 1 comparator for system state management. The TPS659122 comes in a 9 ball x 9 ball WCSP package (3.6mm x 3.6mm) with a 0.4mm pitch. To request a full data sheet, please send an email to: *pmu_contact@list.ti.com*.

1.4 Block Diagram & Pin Functions

1.4.1 Functional Block Diagram

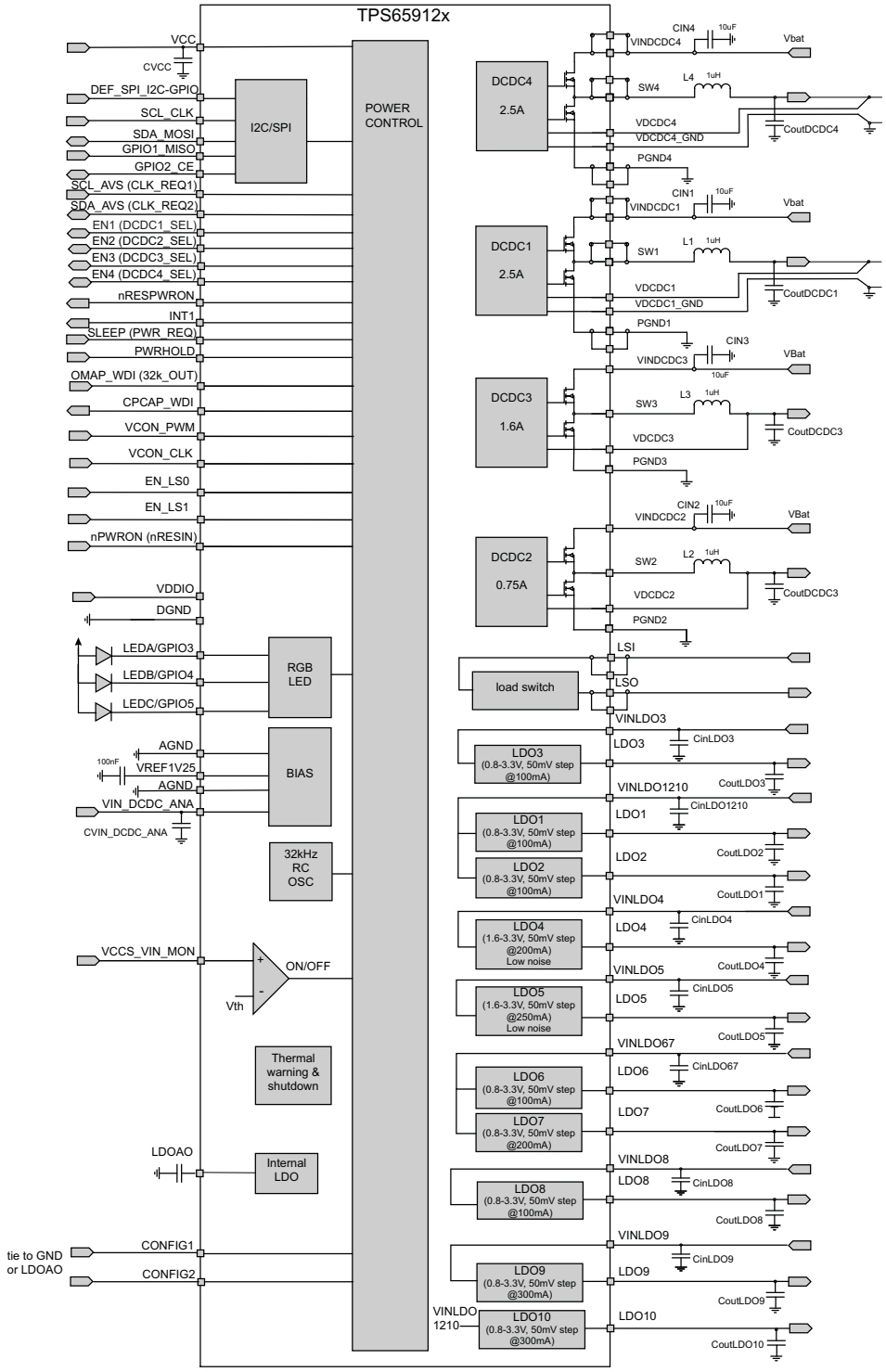

Figure 1-1. TPS65912x Block Diagram

1.4.2 Pinout

YFF PACKAGE
(BOTTOM VIEW)

TPS65912 (bottom view)

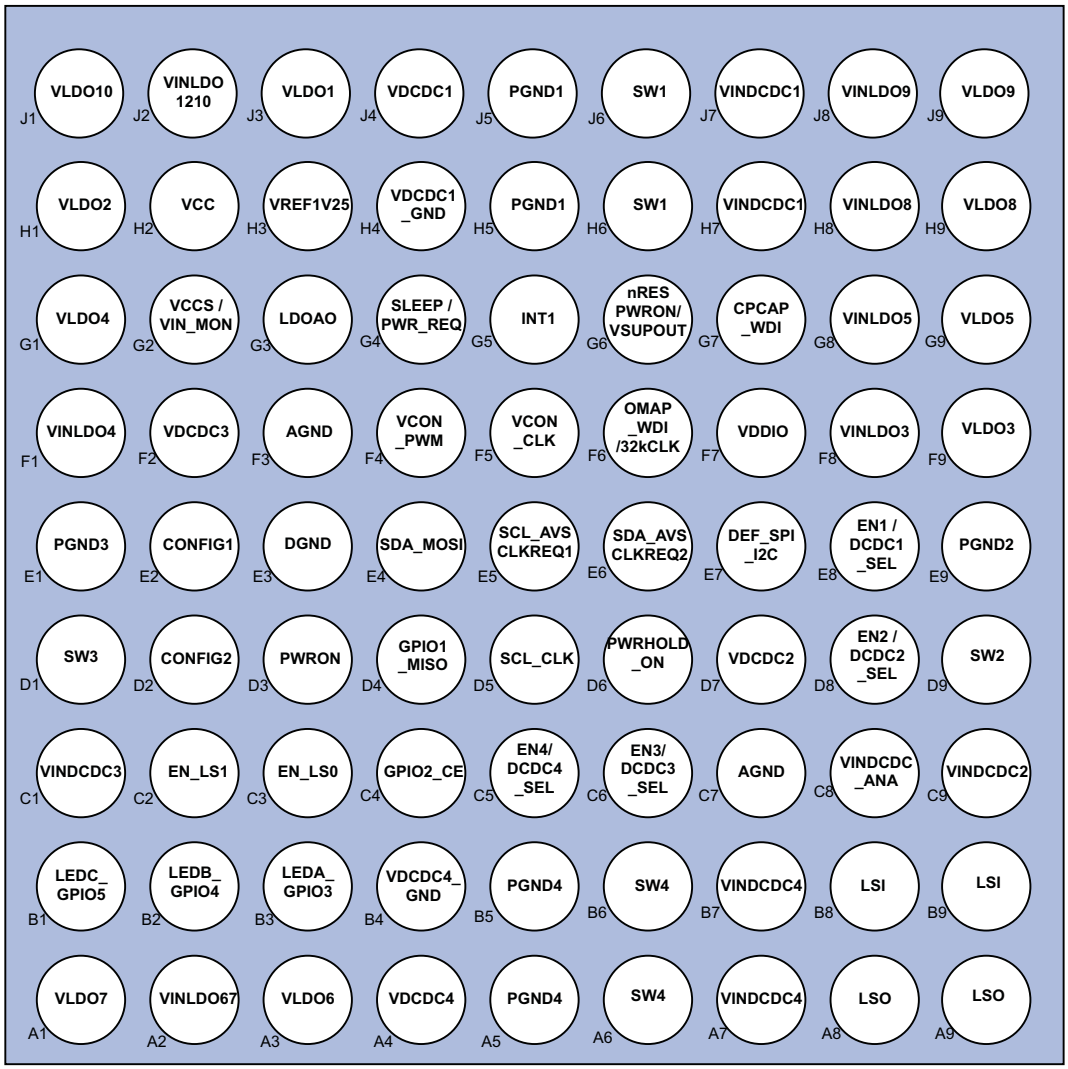

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Table 1-1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
TPS659121			
REFERENCE			
VREF1V25	H3	O	
AGND	F3, C7	-	analog ground connection; connect to PGND on the PCB
DRIVERS / LIGHTING			
LEDA/GPIO3	B3	I/O	general purpose I/O or LED driver output
LEDB/GPIO4	B2	I/O	general purpose I/O or LED driver output
LEDC/GPIO5	B1	I/O	general purpose I/O or LED driver output
STEP_DOWN CONVERTERS			
VINDCDC_ANA	C8	I	analog supply input for DCDC converters; needs to be connected to VINDCDC1, VINDCDC2, VINDCDC3 and VINDCDC4
VINDCDC1	H7, J7	I	power input to DCDC1 converter; connect to VINDCDC2, VINDCDC3, VINDCDC4 and VINDCDC_ANA
VDCDC1	J4	I	voltage sense (feedback) input "+" for DCDC1
VDCDC1_GND	H4	I	voltage sense (feedback) input "GND" for DCDC1
SW1	H6, J6	O	switch node of DCDC1; connect output inductor
PGND1	H5, J5	-	power GND connection for DCDC1 converter
VCON_PWM	F4	I	PWM period signal for dynamic voltage scaling on DCDC1
VCON_CLK	F5	I	clock signal for dynamic voltage scaling on DCDC1
VINDCDC2	C9	I	power input to DCDC2 converter; connect to VINDCDC1, VINDCDC3, VINDCDC4 and VINDCDC_ANA
VDCDC2	D7	I	voltage sense (feedback) input for DCDC2
SW2	D9	O	switch node of DCDC2; connect output inductor
PGND2	E9	-	power GND connection for DCDC2 converter
VINDCDC3	C1	I	power input to DCDC3 converter; connect to VINDCDC1, VINDCDC2, VINDCDC4 and VINDCDC_ANA
VDCDC3	F2	I	voltage sense (feedback) input for DCDC3
SW3	D1	O	switch node of DCDC3; connect output inductor
PGND3	E1	-	power GND connection for DCDC3 converter
VINDCDC4	A7, B7	I	power input to DCDC4 converter; connect to VINDCDC1, VINDCDC2, VINDCDC3 and VINDCDC_ANA
VDCDC4	A4	I	voltage sense (feedback) input "+" for DCDC4
VDCDC4_GND	B4	I	voltage sense (feedback) input "GND" for DCDC4
SW4	A6, B6	O	switch node of DCDC4; connect output inductor
PGND4	A5, B5	-	power GND connection for DCDC4 converter
LOAD SWITCH			
LSI	B8, B9	I	input of the load switch
LSO	A8, A9	O	output of the load switch
EN_LS0	C3	I	load switch enable pin; the status is copied to Bit [LOADSWITCH:ENABLE0] in state CONFIG
EN_LS1	C2	I	load switch enable pin; the status is copied to Bit [LOADSWITCH:ENABLE1] in state CONFIG
LOW DROPOUT REGULATORS			
VINLDO1210	J2	I	power input for LDO1, LDO2 and LDO10
VINLDO3	F8	I	power input for LDO3
VINLDO4	F1	I	power input for LDO4
VINLDO5	G8	I	power input for LDO5
VINLDO67	A2	I	power input for LDO6 and LDO7
VINLDO8	H8	I	power input for LDO8
VINLDO9	J8	I	power input for LDO9

Table 1-1. TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
TPS659121			
LDOAO	G3	O	"LDO always on" internal supply; connect buffer capacitor
VLDO1	J3	O	LDO1 output
VLDO2	H1	O	LDO2 output
VLDO3	F9	O	LDO3 output
VLDO4	G1	O	LDO4 output
VLDO5	G9	O	LDO5 output
VLDO6	A3	O	LDO6 output
VLDO7	A1	O	LDO7 output
VLDO8	H9	O	LDO8 output
VLDO9	J9	O	LDO9 output
VLDO10	J1	O	LDO10 output
STANDARD INTERFACE			
DEF_SPI_I2C-GPIO	E7	I	digital input that defines whether SPI or I2C and GPIOs is available on pins C4, D4, E4, D5: 0=SPI; 1=I2C and GPIO1 and GPIO2
SCK	D5	I	I2C SCL for DEF_SPI_I2C=1 or SPI SCK for DEF_SPI_I2C=0
MOSI	E4	I/O	I2C SDA for DEF_SPI_I2C=1 or SPI MASTER OUT SLAVE IN (MOSI) for DEF_SPI_I2C=0
MISO	D4	I/O	GPIO1 for DEF_SPI_I2C=1 or SPI MASTER IN SLAVE OUT (MISO) for DEF_SPI_I2C=0
CE	C4	I/O	GPIO2 for DEF_SPI_I2C=1 or SPI CHIP ENABLE (CE) active HIGH for DEF_SPI_I2C=0
ENABLE / VOLTAGE SCALING			
			DCDCx_SEL is selected by pulling pin CONFIG2 to GND; this also selects CLK_REQx and PWR_REQ as enable resources
DCDC1_SEL	E8	I	enable pin or voltage scaling pin changing the output of a converter or a group of converters between 2 pre-defined values
DCDC2_SEL	D8	I	enable pin or voltage scaling pin changing the output of a converter or a group of converters between 2 pre-defined values
DCDC3_SEL	C6	I	enable pin or voltage scaling pin changing the output of a converter or a group of converters between 2 pre-defined values
DCDC4_SEL	C5	I	enable pin or voltage scaling pin changing the output of a converter or a group of converters between 2 pre-defined values
			CLK-REQ1, CLK_REQ2 and PWR_REQ is selected by puling pin CONFIG2 to GND
CLK_REQ1	E5	I	power I2C for dynamic voltage scaling: clock pin or clock request signal1 used to enable and disable power resources
CLK_REQ2	E6	I/O	power I2C for dynamic voltage scaling; data pin or clock request signal2 used to enable and disable power resources
PWR_REQ	G4	I	SLEEP mode input or CLK request input
VSUP_OUT	G6	O	Reset output or output of voltage monitor
VIN_MON	G2	I	voltage sense for input voltage monitor; output on pin VSUP_OUT
ON	D6	I	POWERHOLD or ON; enable input
INT1	G5	O	interrupt output
$\overline{\text{RESIN}}$ (optional)	D3	I	active low, debounced power-on input or power request input to start power-up sequencing; alternatively active low reset input to TPS65912x; debounced by 10ms(OTP option); tie to LDOAO for a logic high if not used.
OMAP_WDI_32k_OUT	F6	I	input from OMAP WDI pin to AND gate; alternatively 32kHz RC oscillator output. The option is
CPCAP_WDI	G7	O	push-pull output at VDDIO level of AND gate; connect to CPCAP WDI input
CONFIG1	E2	I	selects pre-defined startup options and default voltages; chooses from two internal OTP settings; tie to GND or LDOAO
CONFIG2	D2	I	selects pre-defined startup options; configures pins as DCDC1_SEL, DCDC2_SEL, DCDC3_SEL and DCDC4_SEL as well as CLK_REQ and PWR_REQ signals with CONFIG2 tied to GND. Tie to LDOAO for a logic high level.

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Table 1-1. TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
TPS659121			
VCC	H2	I	digital supply input
VDDIO	F7	I	supply voltage input for GPIOs and output stages that sets the HIGH level voltage (I/O voltage)
DGND	E3	-	digital GND connection, tie to AGND and PGNDx on the pcb

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS659122YFFR	ACTIVE	DSBGA	YFF	81	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
TPS659122YFFT	ACTIVE	DSBGA	YFF	81	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

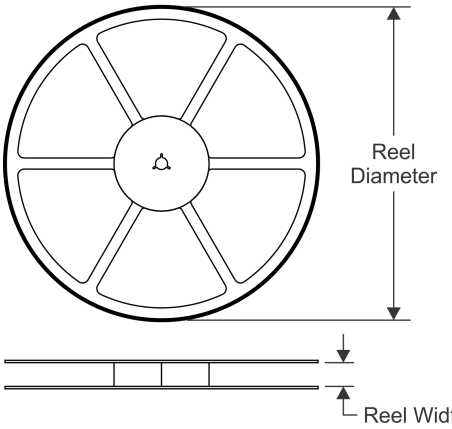
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

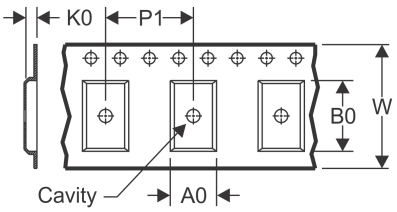
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

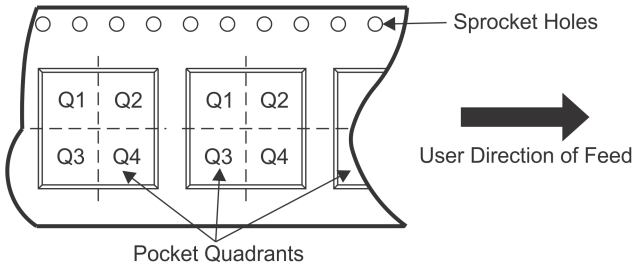


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

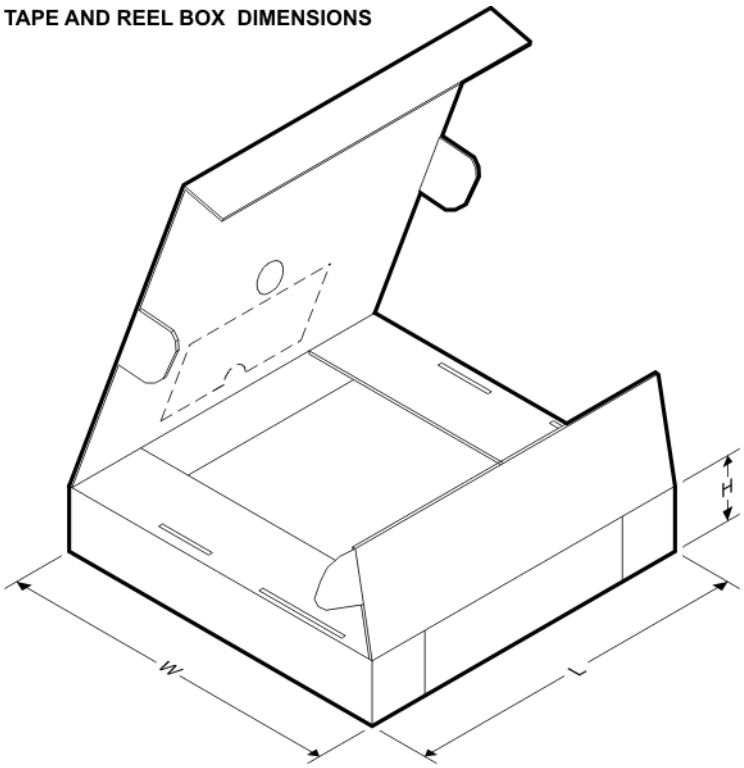
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS659122YFFR	DSBGA	YFF	81	1500	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1
TPS659122YFFT	DSBGA	YFF	81	250	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS659122YFFR	DSBGA	YFF	81	1500	210.0	185.0	35.0
TPS659122YFFT	DSBGA	YFF	81	250	210.0	185.0	35.0

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