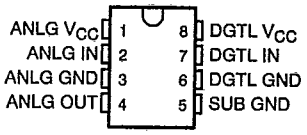
TL1591
SAMPLE-AND-HOLD CIRCUIT FOR CCD IMAGERS

D3327, SEPTEMBER 1989

T-77-17

- 15-MHz Sampling Rate
- 30-ns Acquisition Time
- Diode-Bridge Switch
- 25-MHz Bandwidth
- Low-Voltage Supply

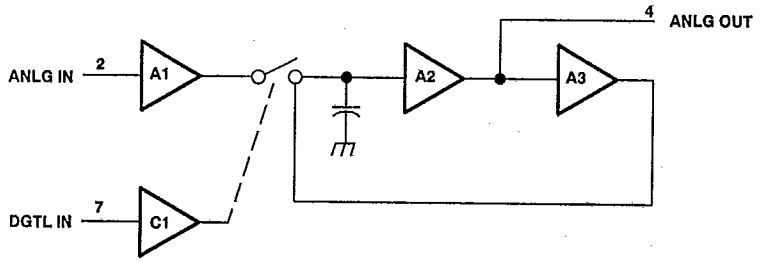
D OR P PACKAGE
(TOP VIEW)



description

The TL1591 is a monolithic integrated sample-and-hold circuit with excellent performance features using the BiFET process with Schottky-barrier diodes and designed for use with CCD area imagers. This device consists of an ultra-fast input buffer amplifier, a digital-controlled diode-bridge switch, and a high-impedance output buffer amplifier. The electronic switch is controlled by an LS-TTL-compatible logic input.

functional block diagram



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Digital input voltage ..... 0 to V_{CC}
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −25°C to 80°C
Storage temperature range ..... −55°C to 150°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 80°C$ POWER RATING
D	725 mW	5.8 mW/°C	406 mW
P	1000 mW	8.0 mW/°C	560 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.5	V
V_{IH}	High-level digital input voltage	2			V
V_{IL}	Low-level digital input voltage			0.8	V
$V_{I(PP)}$	Peak-to-peak analog input voltage			0.8	V

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage					−1.5	V
$V_{O(PP)}$	Analog peak-to-peak output voltage				1.1		V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_{IH} = 2.7 V			20	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_{IL} = 0.4 V		−0.28	−0.4	mA
I_O	Analog output current				0.6		mA
I_{CC}	Supply current	V_{CC} = 5.5 V			15	20	mA
r_i	Input resistance				10		kΩ
r_o	Analog output resistance				50		Ω

operating characteristics

PARAMETER		MIN	TYP†	MAX	UNIT
	Linearity		0.7%	2%	
A_v	Voltage amplification		0.8	0.9	V/V
	Sample-to-hold offset error		15		mV
	Sample-mode offset error		−50	50 −150	mV
	Hold-mode feedthrough			−50	dB
	Hold-mode droop			100	µV/µs

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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dynamic characteristics (see Figure 1)

PARAMETER	MIN	TYP†	MAX	UNIT
Acquisition time 0.6 V to 2% (see Note 1)		18		ns
Acquisition time 0.6 V to 1% (see Note 1)		31		ns
Hold-mode settling time (see Note 2)		35		ns
Sampling-mode bandwidth		25		MHz
Sampling rate			15	MHz

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

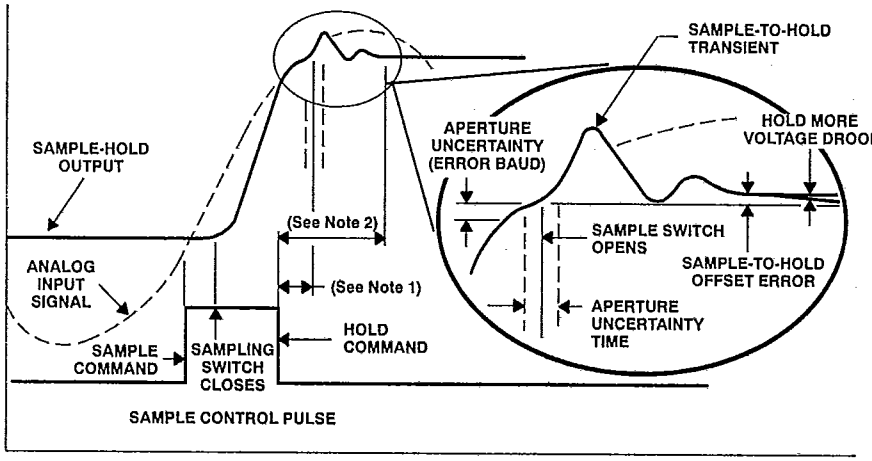

FIGURE 1. SAMPLE-HOLD DEFINITIONS

NOTES: 1. Acquisition time is the time required, after the closing of the sampling switch, for the hold capacitor to charge to a full-scale voltage change and then remain within a specified error band around the final value.
2. Hold-mode settling time is the time from the hold command transistion until the output has settled within a specified error band around the final value.

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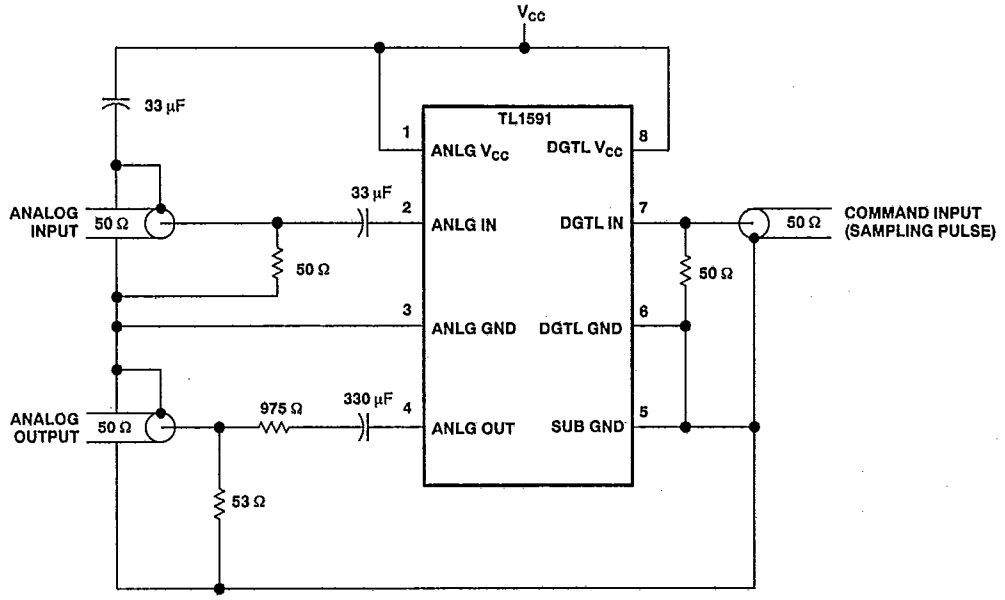

FIGURE 2. TEST CIRCUIT

TYPICAL CHARACTERISTICS

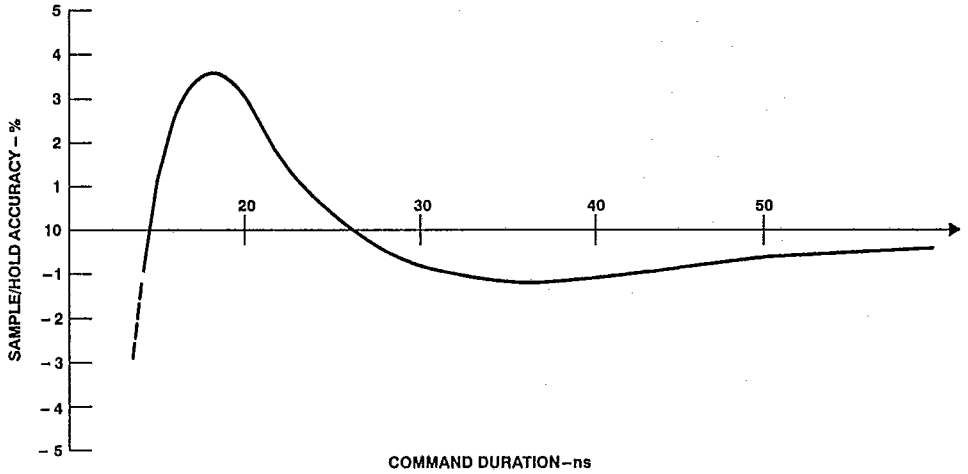

FIGURE 3. SAMPLE/HOLD ACCURACY VS COMMAND DURATION

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