

# TL1454, TL1454Y DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM) CONTROL CIRCUIT

SLVS086B – APRIL 1995 – REVISED NOVEMBER 1997

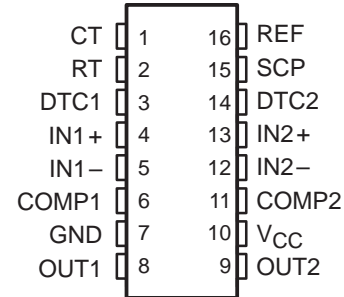
- Two Complete PWM Control Circuits
- Outputs Drive MOSFETs Directly
- Oscillator Frequency . . . 50 kHz to 2 MHz
- 3.6-V to 20-V Supply-Voltage Range
- Low Supply Current . . . 3.5 mA Typ
- Adjustable Dead-Time Control, 0% to 100%
- 1.25-V Reference

## description

The TL1454 is a dual-channel pulse-width-modulation (PWM) control circuit, primarily intended for low-power, dc/dc converters. Applications include LCD displays, backlight inverters, notebook computers, and other products requiring small, high-frequency, dc/dc converters. Each PWM channel has its own error amplifier, PWM comparator, dead-time control comparator, and MOSFET driver. The voltage reference, oscillator, undervoltage lockout, and short-circuit protection are common to both channels.

Channel 1 is configured to drive n-channel MOSFETs in step-up or flyback converters, and channel 2 is configured to drive p-channel MOSFETs in step-down or inverting converters. The operating frequency is set with an external resistor and an external capacitor, and dead time is continuously adjustable from 0 to 100% duty cycle with a resistive divider network. Soft start can be implemented by adding a capacitor to the dead-time control (DTC) network. The error-amplifier common-mode input range includes ground, which allows the TL1454 to be used in ground-sensing battery chargers as well as voltage converters.

D, N OR PW PACKAGE  
(TOP VIEW)



## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES†			CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
–20°C to 85°C	TL1454CD	TL1454CN	TL1454CPWLE	TL1454Y
–40°C to 85°C	TL1454ID	TL1454IN	—	—

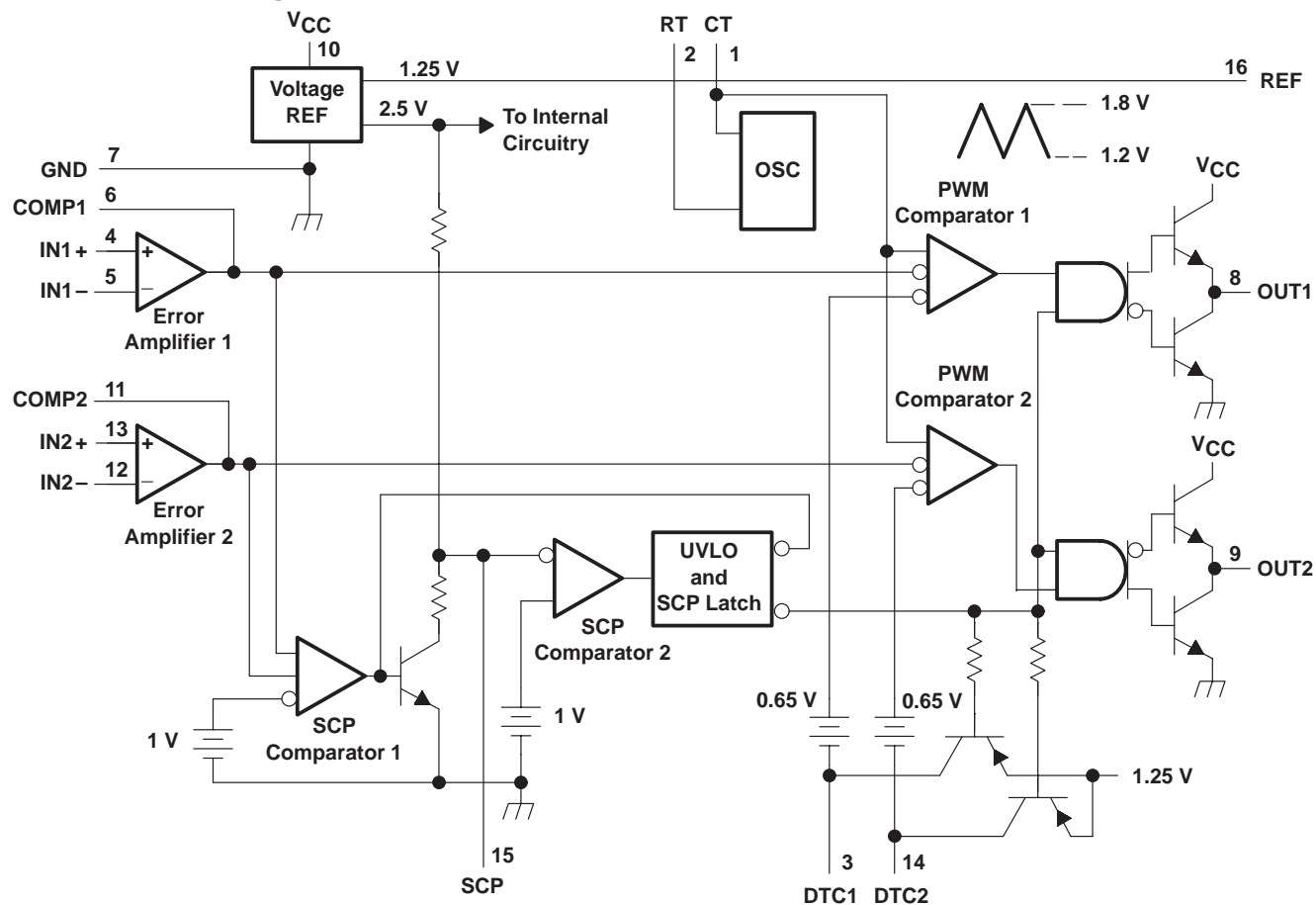
† The D package is available taped and reeled. Add the suffix R to the device name (e.g., TL1454CDR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TL1454CPWLE).

# TL1454, TL1454Y

## DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM) CONTROL CIRCUIT

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### functional block diagram



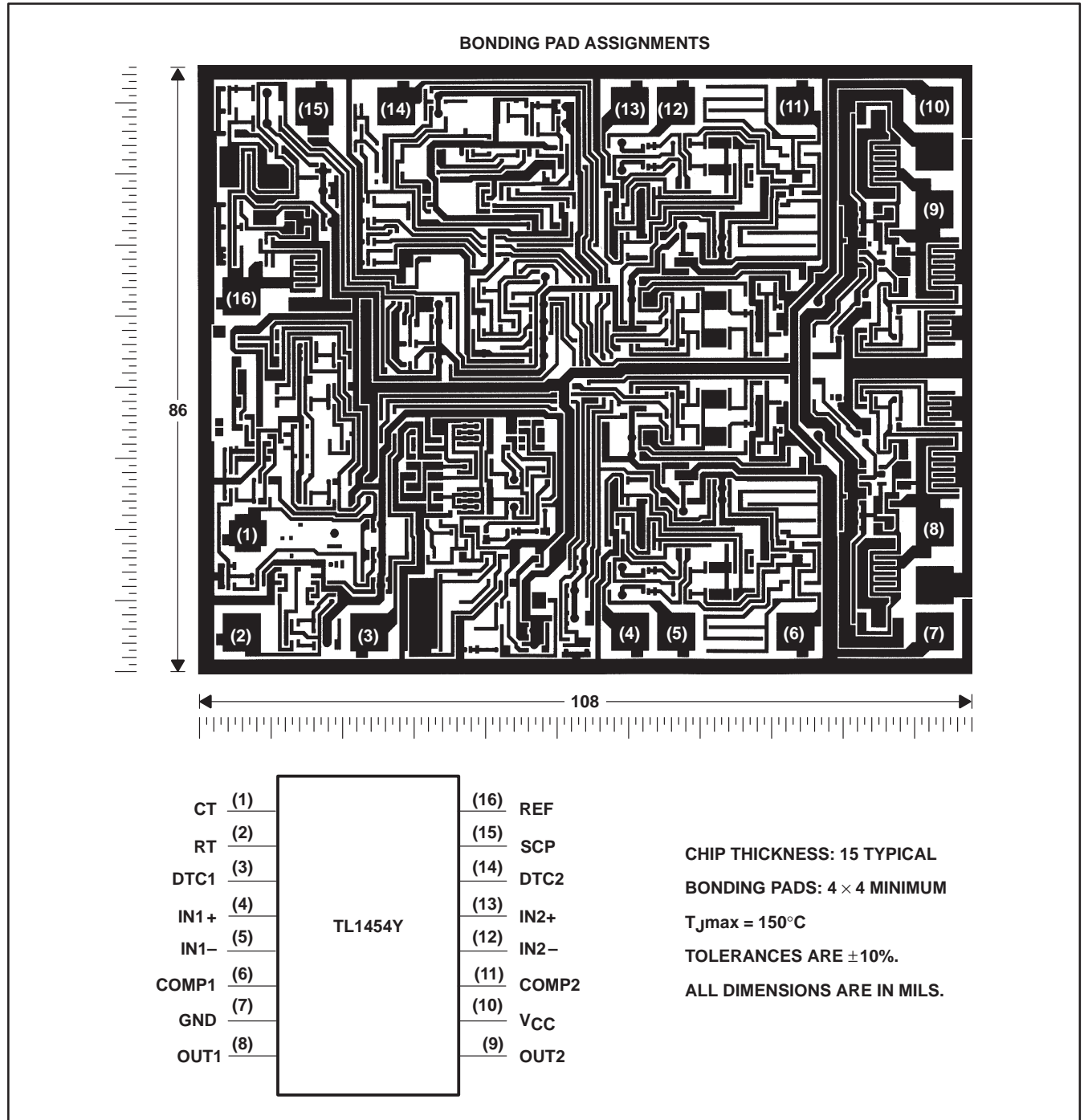
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# TL1454, TL1454Y DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM) CONTROL CIRCUIT

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## TL1454Y chip information

This chip, when properly assembled, displays characteristics similar to the TL1454C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



# TL1454, TL1454Y

## DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM) CONTROL CIRCUIT

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### theory of operation

#### reference voltage

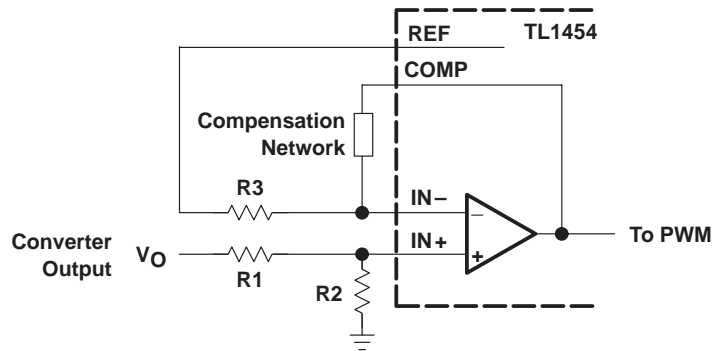
A linear regulator operating from  $V_{CC}$  generates a 2.5-V supply for the internal circuits and the 1.25-V reference, which can source a maximum of 1 mA for external loads. A small ceramic capacitor (0.047  $\mu$ F to 0.1  $\mu$ F) between REF and ground is recommended to minimize noise pickup.

#### error amplifier

The error amplifier generates the error signal used by the PWM to adjust the power-switch duty cycle for the desired converter output voltage. The signal is generated by comparing a sample of the output voltage to the voltage reference and amplifying the difference. An external resistive divider connected between the converter output and ground, as shown in Figure 1, is generally required to obtain the output voltage sample.

The amplifier output is brought out on COMP to allow the frequency response of the amplifier to be shaped with an external RC network to stabilize the feedback loop of the converter. DC loading on the COMP output is limited to 45  $\mu$ A (the maximum amplifier source current capability).

Figure 1 illustrates the sense-divider network and error-amplifier connections for converters with positive output voltages. The divider network is connected to the noninverting amplifier input because the PWM has a phase inversion; the duty cycle decreases as the error-amplifier output increases.



**Figure 1. Sense Divider/Error Amplifier Configuration for Converters with Positive Outputs**

The output voltage is given by:

$$V_O = V_{\text{ref}} \left( 1 + \frac{R_1}{R_2} \right)$$

where  $V_{\text{ref}} = 1.25$  V.

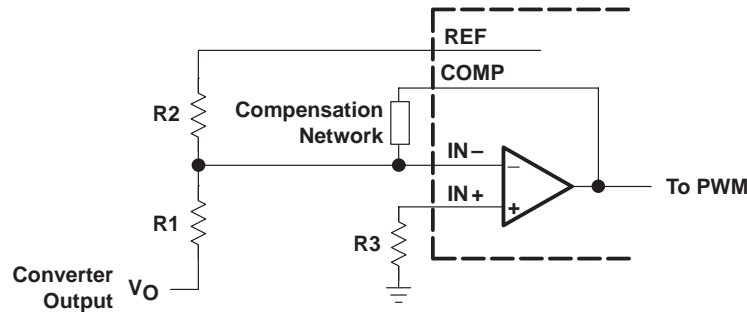
The dc source resistance of the error-amplifier inputs should be 10 k $\Omega$  or less and approximately matched to minimize output voltage errors caused by the input-bias current. A simple procedure for determining appropriate values for the resistors is to choose a convenient value for  $R_3$  (10 k $\Omega$  or less) and calculate  $R_1$  and  $R_2$  using:

$$R_1 = \frac{R_3 V_O}{V_O - V_{\text{ref}}}$$

$$R_2 = \frac{R_3 V_O}{V_{\text{ref}}}$$

### error amplifier

R1 and R2 should be tight-tolerance ( $\pm 1\%$  or better) devices with low and/or matched temperature coefficients to minimize output voltage errors. A device with a  $\pm 5\%$  tolerance is suitable for R3.



**Figure 2. Sense Divider/Error Amplifier Configuration for Converters with Negative Outputs**

Figure 2 shows the divider network and error-amplifier configuration for negative output voltages. In general, the comments for positive output voltages also apply for negative outputs. The output voltage is given by:

$$V_O = -\frac{R_1 V_{\text{ref}}}{R_2}$$

The design procedure for choosing the resistor value is to select a convenient value for R2 (instead of R3 in the procedure for positive outputs) and calculate R1 and R3 using:

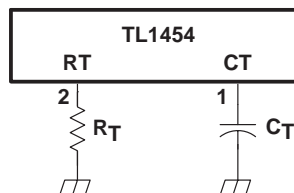
$$R_1 = -\frac{R_2 V_O}{V_{\text{ref}}}$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

Values in the 10-k $\Omega$  to 20-k $\Omega$  range work well for R2. R3 can be omitted and the noninverting amplifier connected to ground in applications where the output voltage tolerance is not critical.

### oscillator

The oscillator frequency can be set between 50 kHz and 2 MHz with a resistor connected between RT and GND and a capacitor between CT and GND (see Figure 3). Figure 6 is used to determine  $R_T$  and  $C_T$  for the desired operating frequency. Both components should be tight-tolerance, temperature-stable devices to minimize frequency deviation. A 1% metal-film resistor is recommended for  $R_T$ , and a 10%, or better, NPO ceramic capacitor is recommended for  $C_T$ .



**Figure 3. Oscillator Timing**

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## DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM) CONTROL CIRCUIT

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### dead-time control (DTC) and soft start

The two PWM channels have independent dead-time control inputs so that the maximum power-switch duty cycles can be limited to less than 100%. The dead-time is set with a voltage applied to DTC; the voltage is typically obtained from a resistive divider connected between the reference and ground as shown in Figure 4. Soft start is implemented by adding a capacitor between REF and DTC.

The voltage,  $V_{DT}$ , required to limit the duty cycle to a maximum value is given by:

$$V_{DT} = V_{O(max)} - D(V_{O(max)} - V_{O(min)}) - 0.65$$

where  $V_{O(max)}$  and  $V_{O(min)}$  are obtained from Figure 9, and  $D$  is the maximum duty cycle.

Predicting the regulator startup or rise time is complicated because it depends on many variables, including: input voltage, output voltage, filter values, converter topology, and operating frequency. In general, the output will be in regulation within two time constants of the soft-start circuit. A five-to-ten millisecond time constant usually works well for low-power converters.

The DTC input can be grounded in applications where achieving a 100% duty cycle is desirable, such as a buck converter with a very low input-to-output differential voltage. However, grounding DTC prevents the implementation of soft start, and the output voltage overshoot at power-on is likely to be very large. A better arrangement is to omit  $R_{DT1}$  (see Figure 4) and choose  $R_{DT2} = 47\text{ k}\Omega$ . This configuration ensures that the duty cycle can reach 100% and still allows the designer to implement soft start using  $C_{SS}$ .

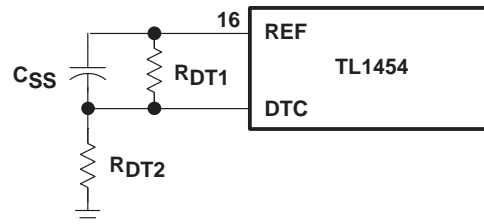


Figure 4. Dead-Time Control and Soft Start

### PWM comparator

Each of the PWM comparators has dual inverting inputs. One inverting input is connected to the output of the error amplifier; the other inverting input is connected to the DTC terminal. Under normal operating conditions, when either the error-amplifier output or the dead-time control voltage is higher than that for the PWM triangle wave, the output stage is set inactive (OUT1 low and OUT2 high), turning the external power stage off.

### undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output circuit off and resets the SCP latch whenever the supply voltage drops too low (to approximately 2.9 V) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

### short-circuit protection (SCP)

The TL1454 SCP function prevents damage to the power switches when the converter output is shorted to ground. In normal operation, SCP comparator 1 clamps SCP to approximately 185 mV. When one of the converter outputs is shorted, the error amplifier output (COMP) will be driven below 1 V to maximize duty cycle and force the converter output back up. When the error amplifier output drops below 1 V, SCP comparator 1 releases SCP, and capacitor,  $C_{SCP}$ , which is connected between SCP and GND, begins charging. If the error-amplifier output rises above 1 V before  $C_{SCP}$  is charged to 1 V, SCP comparator 1 discharges  $C_{SCP}$  and normal operation resumes. If  $C_{SCP}$  reaches 1 V, SCP comparator 2 turns on and sets the SCP latch, which turns off the output drives and resets the soft-start circuit. The latch remains set until the supply voltage is lowered to 2 V or less, or  $C_{SCP}$  is discharged externally.



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### short-circuit protection (SCP) (continued)

The SCP time-out period must be greater than the converter start-up time or the converter will not start. Because high-value capacitor tolerances tend to be  $\pm 20\%$  or more and IC resistor tolerances are loose as well, it is best to choose an SCP time-out period 10-to-15 times greater than the converter startup time. The value of  $C_{SCP}$  may be determined using Figure 6, or it can be calculated using:

$$C_{SCP} = \frac{T_{SCP}}{80.3}$$

where  $C_{SCP}$  is in  $\mu F$  and  $T_{SCP}$  is the time-out period in ms.

### output stage

The output stage of the TL1454 is a totem-pole output with a maximum source/sink current rating of 40 mA and a voltage rating of 20 V. The output is controlled by a complementary output AND gate and is turned on (sourcing current for OUT1, sinking current for OUT2) when all the following conditions are met: 1) the oscillator triangle wave voltage is higher than both the DTC voltage and the error-amplifier output voltage, 2) the undervoltage-lockout circuit is inactive, and 3) the short-circuit protection circuit is inactive.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ (see Note 1)	23 V
Error amplifier input voltage: IN1+, IN1–, IN2+, IN2–	23 V
Output voltage: OUT1, OUT2	20 V
Continuous output current: OUT1, OUT2	$\pm 200$ mA
Peak output current: OUT1, OUT2	1 A
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : C suffix	–20°C to 85°C
I suffix	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW
PW	500 mW	4.0 mW/°C	320 mW	260 mW

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### CONTROL CIRCUIT

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#### recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC}$		3.6	20	V
Error amplifier common-mode input voltage		–0.2	1.45	V
Output voltage, $V_O$			20	V
Output current, $I_O$			±40	mA
COMP source current			–45	μA
COMP sink current			100	μA
Reference output current			1	mA
COMP dc load resistance		100		kΩ
Timing capacitor, $C_T$		10	4000	pF
Timing resistor, $R_T$		5.1	100	kΩ
Oscillator frequency		50	2000	kHz
Operating free-air temperature, $T_A$	TL1454C	–20	85	°C
	TL1454I	–40	85	

electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 500\text{ kHz}$  (unless otherwise noted)

#### reference

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
$V_{ref}$	Output voltage, REF	$I_O = 1\text{ mA}$ , $T_A = 25^\circ\text{C}$	1.23	1.25	1.28	V
		$I_O = 1\text{ mA}$	1.2		1.31	
	Input regulation	$V_{OC} = 3.6\text{ V to }20\text{ V}$ , $I_O = 1\text{ mA}$		2	6	mV
	Output regulation	$I_O = 0.1\text{ mA to }1\text{ mA}$		1	7.5	mV
	Output voltage change with temperature	$T_A = T_{A(min)} \text{ to } 25^\circ\text{C}$ , $I_O = 1\text{ mA}$	–12.5	–1.25	12.5	mV
		$T_A = 25^\circ\text{C to } 85^\circ\text{C}$ , $I_O = 1\text{ mA}$	–12.5	–2.5	12.5	
$I_{OS}$	Short-circuit output current	$V_{ref} = 0\text{ V}$		30		mA

#### undervoltage lockout (UVLO)

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
$V_{IT+}$	Positive-going threshold voltage	$T_A = 25^\circ\text{C}$		2.9		V
$V_{IT-}$	Negative-going threshold voltage			2.7		V
$V_{hys}$	Hysteresis, $V_{IT+} - V_{IT-}$		100	200		mV

#### short-circuit protection (SCP)

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
$V_{IT}$	Input threshold voltage	$T_A = 25^\circ\text{C}$	0.95	1	1.05	V
$V_{stby}^\dagger$	Standby voltage	No pullup	140	185	230	mV
$V_{I(latched)}$	Latched-mode input voltage			60	120	mV
$V_{IT(COMP)}$	Comparator threshold voltage	COMP1, COMP2		1		V
	Input source current	$T_A = 25^\circ\text{C}$ , $V_O(SCP) = 0$	–5	–15	–20	μA

<sup>†</sup> This symbol is not presently listed within EIA/JEDEC standards for semiconductor symbology.



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**electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 500\text{ kHz}$  (unless otherwise noted) (continued)**

**oscillator**

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
$f_{osc}$	Frequency	$C_T = 120\text{ pF}$ , $R_T = 10\text{ k}\Omega$		500		kHz
	Standard deviation of frequency			50		kHz
	Frequency change with voltage	$V_{CC} = 3.6\text{ V}$ to $20\text{ V}$ , $T_A = 25^\circ\text{C}$		5		kHz
	Frequency change with temperature	$T_A = T_{A(\min)}$ to $25^\circ\text{C}$		-2	$\pm 20$	kHz
		$T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$		-10	$\pm 20$	
	Maximum ramp voltage			1.8		V
	Minimum ramp voltage			1.1		V

**dead-time control (DTC)**

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
$V_{IT}$	Input threshold voltage	Duty cycle = 0%	1	1.1	1.2	V
		Duty cycle = 100%	0.4	0.5	0.6	
$V_{I(\text{latched})}$	Latched-mode input voltage			1.2		V
$I_{IB}$	Common-mode input bias current	DTC1, $IN1+ \approx 1.2\text{ V}$			4	$\mu\text{A}$
	Latched-mode (source) current	$T_A = 25^\circ\text{C}$		-100		$\mu\text{A}$

**error-amplifier**

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_O = 1.25\text{ V}$ , $V_{IC} = 1.25\text{ V}$			6	mV
$I_{IO}$	Input offset current				100	nA
$I_{IB}$	Input bias current			-160	-500	nA
$V_{ICR}$	Input voltage range	$V_{CC} = 3.6\text{ V}$ to $20\text{ V}$	-0.2	1.40		V
$A_V$	Open-loop voltage gain	$R_{FB} = 200\text{ k}\Omega$	70	80		dB
	Unity-gain bandwidth			3		MHz
CMRR	Common-mode rejection ratio		60	80		dB
$V_{OM(\text{max})}$	Positive output voltage swing		2.3	2.43		V
$V_{OM(\text{min})}$	Negative output voltage swing			0.63	0.8	
$I_{O+}$	Output sink current	$V_{ID} = -0.1\text{ V}$ , $V_O = 1.20\text{ V}$	0.1	0.5		mA
$I_{O-}$	Output source current	$V_{ID} = 0.1\text{ V}$ , $V_O = 1.80\text{ V}$	-45	-70		$\mu\text{A}$

**output**

PARAMETER		TEST CONDITIONS	TL1454			UNIT
			MIN	TYP	MAX	
$V_{OH}$	High-level output voltage	$I_O = -8\text{ mA}$	$V_{CC}-2$	4.5		V
		$I_O = -40\text{ mA}$	$V_{CC}-2$	4.4		
$V_{OL}$	Low-level output voltage	$I_O = 8\text{ mA}$		0.1	0.4	V
		$I_O = 40\text{ mA}$		1.8	2.5	
$t_{rv}$	Output voltage rise time	$C_L = 2000\text{ pF}$ , $T_A = 25^\circ\text{C}$		220		ns
$t_{fv}$	Output voltage fall time			220		



# TL1454, TL1454Y

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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 500\text{ kHz}$  (unless otherwise noted) (continued)

#### supply current

PARAMETER	TEST CONDITIONS	TL1454			UNIT
		MIN	TYP	MAX	
$I_{CC(stby)}$ Standby supply current	$R_T$ open, $C_T = 1.5\text{ V}$ , No load, $V_O$ (COMP1, COMP2) = 1.25 V,		3.1	6	mA
$I_{CC(average)}$ Average supply current	$R_T = 10\text{ k}\Omega$ , $C_T = 120\text{ pF}$ , 50% duty cycle, Outputs open		3.5	7	mA

electrical characteristics,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 500\text{ kHz}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

#### reference

PARAMETER	TEST CONDITIONS	TL1454Y			UNIT
		MIN	TYP	MAX	
$V_{ref}$ Output voltage, REF	$I_O = 1\text{ mA}$ ,		1.25		V
Input regulation	$V_{OC} = 3.6\text{ V to }20\text{ V}$ , $I_O = 1\text{ mA}$		2		mV
Output regulation	$I_O = 0.1\text{ mA to }1\text{ mA}$		1		mV
Output voltage change with temperature	$I_O = 1\text{ mA}$		-1.25		mV
	$I_O = 1\text{ mA}$		-2.5		
$I_{OS}$ Short-circuit output current	$V_{ref} = 0\text{ V}$		30		mA

#### undervoltage lockout (UVLO)

PARAMETER	TEST CONDITIONS	TL1454Y			UNIT
		MIN	TYP	MAX	
$V_{IT+}$ Positive-going threshold voltage			2.9		V
$V_{IT-}$ Negative-going threshold voltage			2.7		V
$V_{hys}$ Hysteresis, $V_{IT+} - V_{IT-}$			200		mV

#### short-circuit protection (SCP)

PARAMETER	TEST CONDITIONS	TL1454Y			UNIT
		MIN	TYP	MAX	
$V_{IT}$ Input threshold voltage	No pullup		1		V
$V_{stby}^\dagger$ Standby voltage			185		mV
$V_{I(latched)}$ Latched-mode input voltage			60		mV
$V_{IT(COMP)}$ Comparator threshold voltage	COMP1, COMP2		1		V
Input source current	$V_{O(SCP)} = 0$		-15		$\mu\text{A}$

$^\dagger$  This symbol is not presently listed within EIA/JEDEC standards for semiconductor symbology.

#### oscillator

PARAMETER	TEST CONDITIONS	TL1454Y			UNIT
		MIN	TYP	MAX	
$f_{osc}$ Frequency	$C_T = 120\text{ pF}$ , $R_T = 10\text{ k}\Omega$		500		kHz
Standard deviation of frequency			50		kHz
Frequency change with voltage	$V_{CC} = 3.6\text{ V to }20\text{ V}$		5		kHz
Frequency change with temperature			-2		kHz
			-10		
Maximum ramp voltage			1.8		V
Minimum ramp voltage			1.1		V



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**electrical characteristics,  $V_{CC} = 6\text{ V}$ ,  $f_{osc} = 500\text{ kHz}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted) (continued)**

**dead-time control (DTC)**

PARAMETER	TEST CONDITIONS	TL1454Y			UNIT
		MIN	TYP	MAX	
$V_{IT}$ Input threshold voltage	Duty cycle = 0%		1.1		V
	Duty cycle = 100%		0.5		
$V_{I(latched)}$ Latched-mode input voltage			1.2		V
Latched-mode (source) current			–100		$\mu\text{A}$

**error-amplifier**

PARAMETER	TEST CONDITIONS	TL1454Y			UNIT
		MIN	TYP	MAX	
$I_{IB}$ Input bias current	$V_O = 1.25\text{ V}$ , $V_{IC} = 1.25\text{ V}$		–160		nA
$A_V$ Open-loop voltage gain	$R_{FB} = 200\text{ k}\Omega$		80		dB
Unity-gain bandwidth			3		MHz
CMRR Common-mode rejection ratio			80		dB
$V_{OM(max)}$ Positive output voltage swing			2.43		V
$V_{OM(min)}$ Negative output voltage swing			0.63		
$I_{O+}$ Output sink current	$V_{ID} = -0.1\text{ V}$ , $V_O = 1.20\text{ V}$		0.5		mA
$I_{O-}$ Output source current	$V_{ID} = 0.1\text{ V}$ , $V_O = 1.80\text{ V}$		–70		$\mu\text{A}$

**output**

PARAMETER	TEST CONDITIONS	TL1454Y			UNIT
		MIN	TYP	MAX	
$V_{OH}$ High-level output voltage	$I_O = -8\text{ mA}$		4.5		V
	$I_O = -40\text{ mA}$		4.4		
$V_{OL}$ Low-level output voltage	$I_O = 8\text{ mA}$		0.1		V
	$I_O = 40\text{ mA}$		1.8		
$t_{rv}$ Output voltage rise time	$C_L = 2000\text{ pF}$		220		ns
$t_{fv}$ Output voltage fall time			220		

**supply current**

PARAMETER	TEST CONDITIONS	TL1454Y			UNIT
		MIN	TYP	MAX	
$I_{CC(stby)}$ Standby supply current	RT open, $C_T = 1.5\text{ V}$ , No load, $V_O$ (COMP1, COMP2) = 1.25 V,		3.1		mA
$I_{CC(average)}$ Average supply current	$R_T = 10\text{ k}\Omega$ , $C_T = 120\text{ pF}$ , 50% duty cycle, Outputs open		3.5		mA



# TL1454, TL1454Y

## DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM) CONTROL CIRCUIT

SLVS086B – APRIL 1995 – REVISED NOVEMBER 1997

### PARAMETER MEASUREMENT INFORMATION

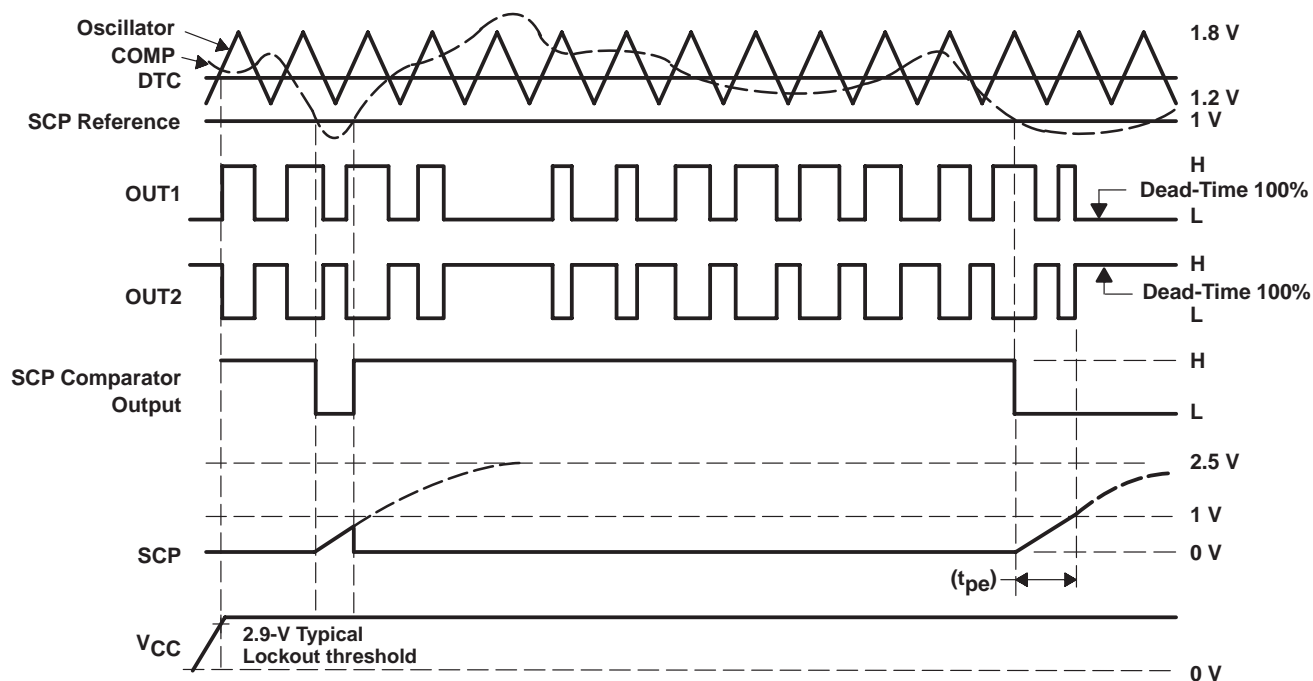


Figure 5. Timing Diagram



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## TYPICAL CHARACTERISTICS

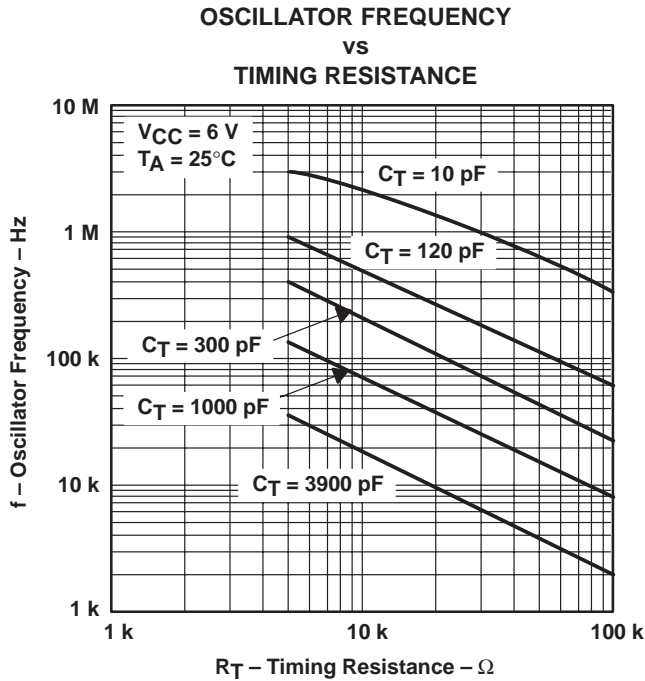


Figure 6

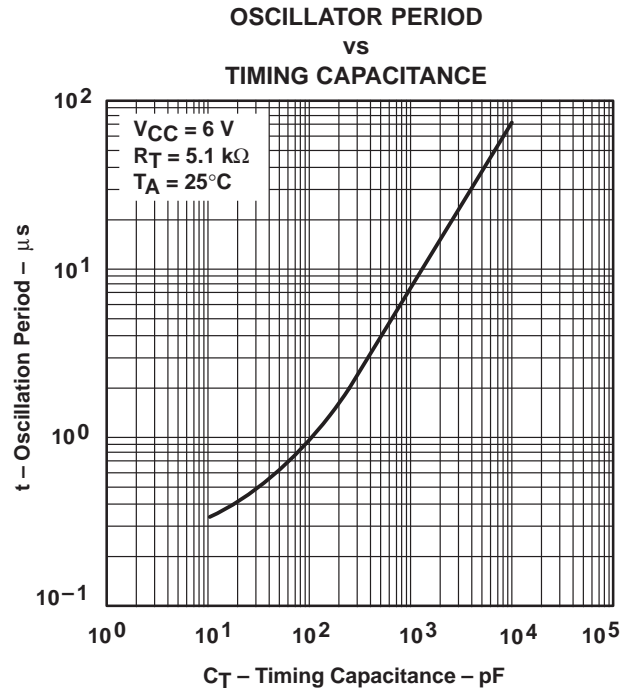


Figure 7

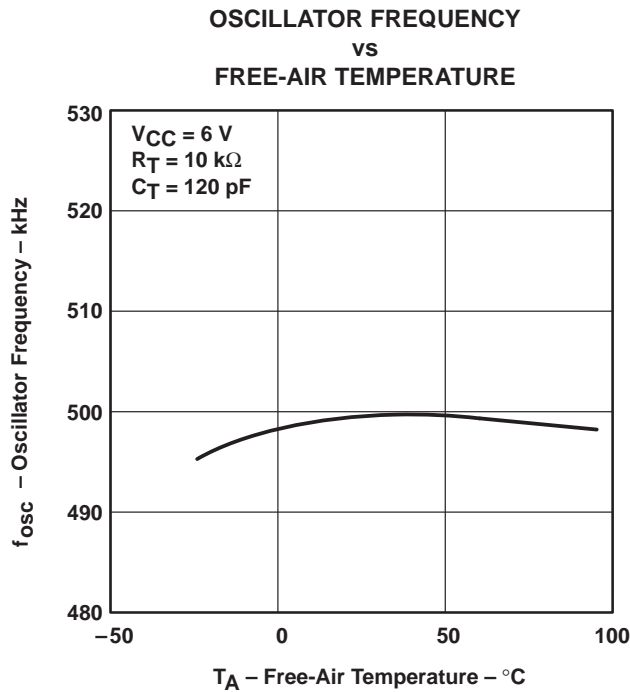


Figure 8

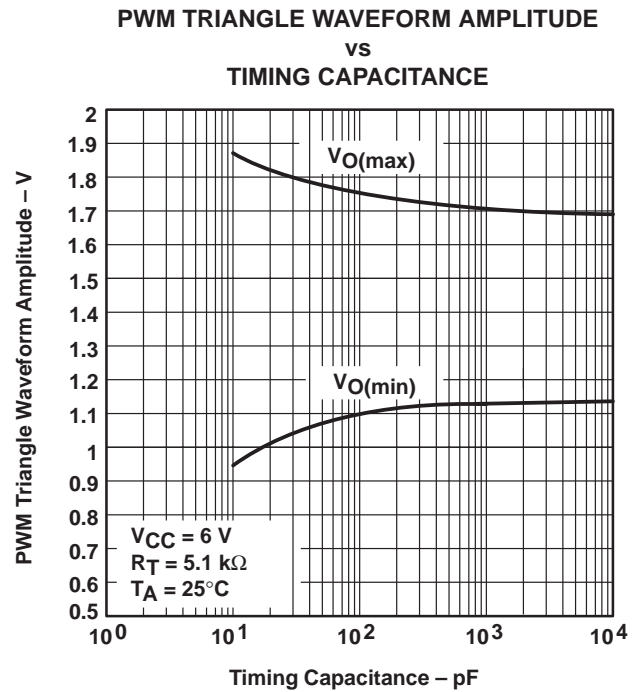


Figure 9

# TL1454, TL1454Y

## DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM)

### CONTROL CIRCUIT

SLVS086B – APRIL 1995 – REVISED NOVEMBER 1997

#### TYPICAL CHARACTERISTICS

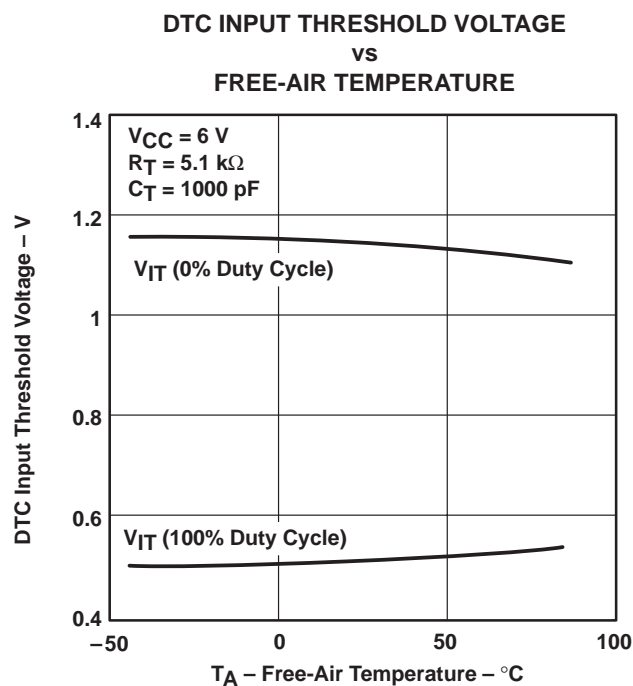


Figure 10

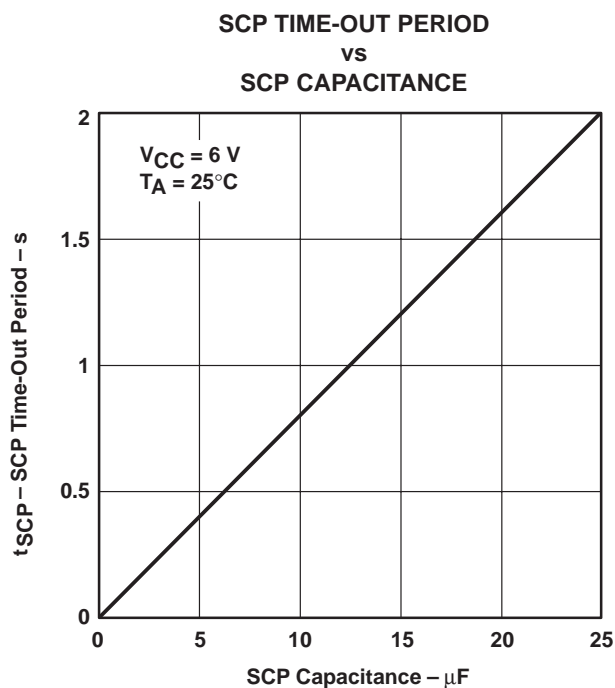


Figure 11

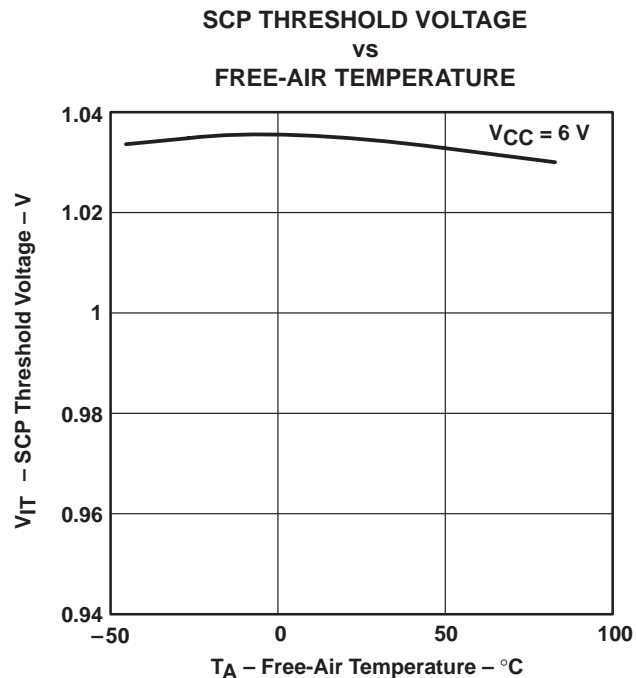


Figure 12

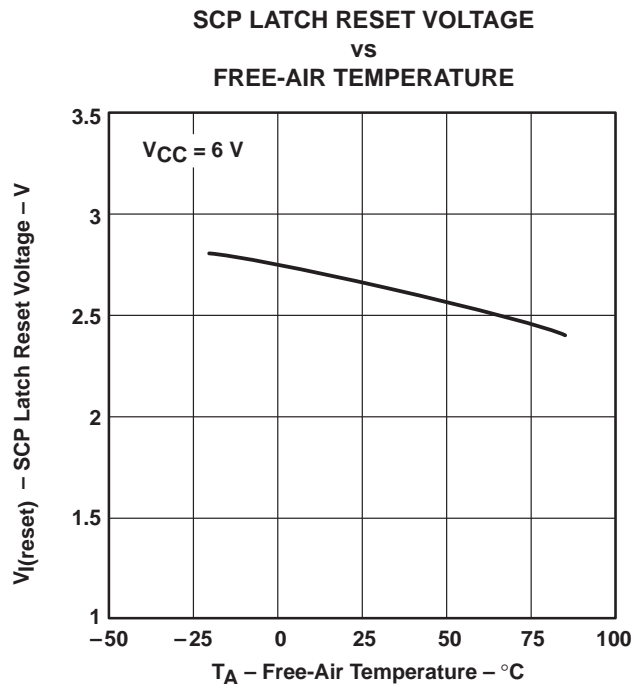


Figure 13



## TYPICAL CHARACTERISTICS

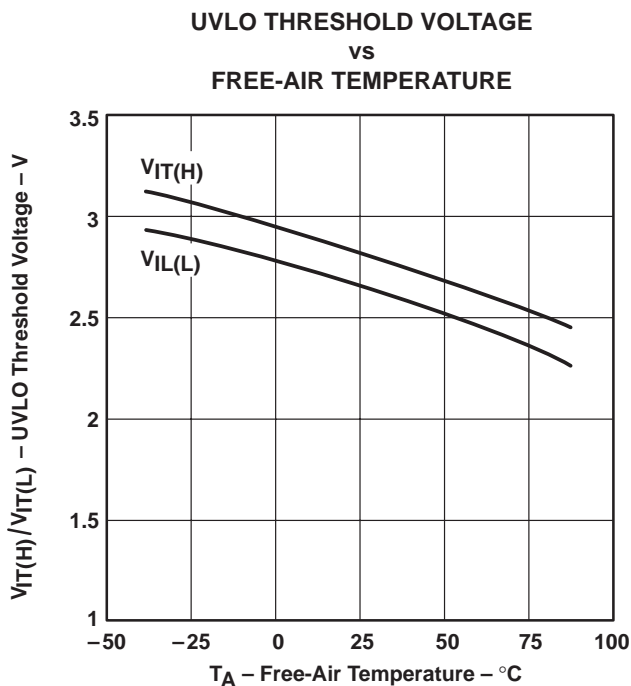


Figure 14

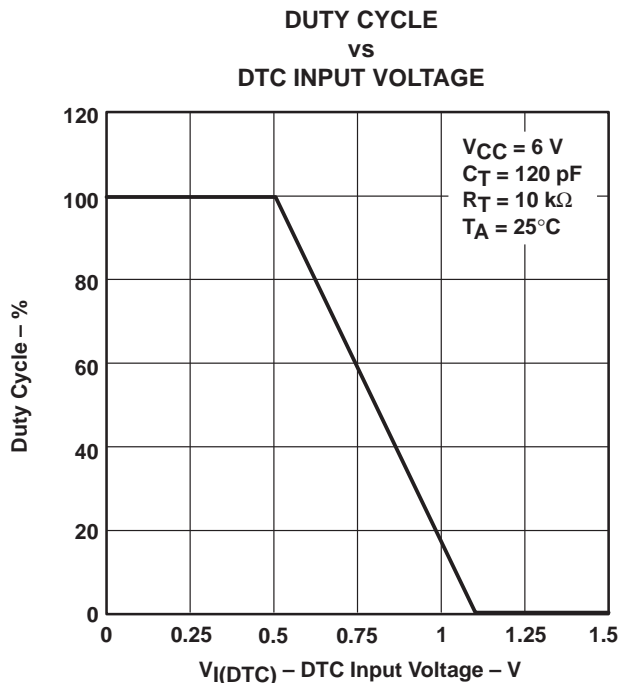


Figure 15

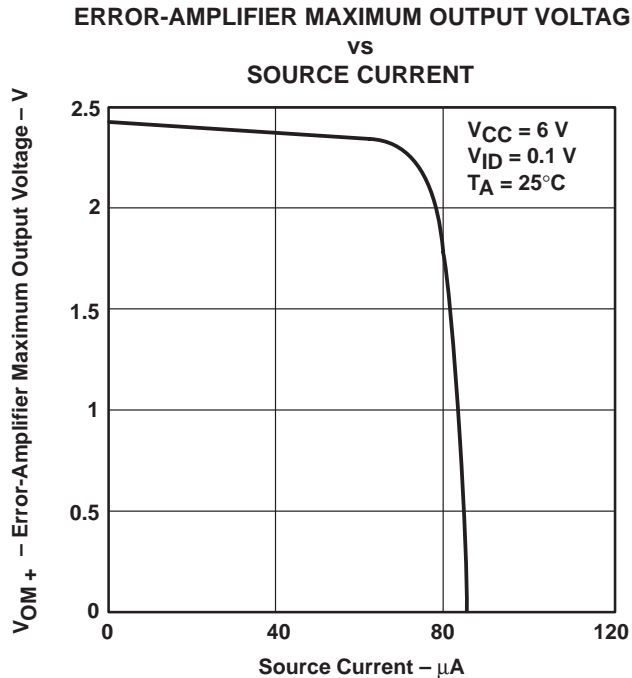


Figure 16

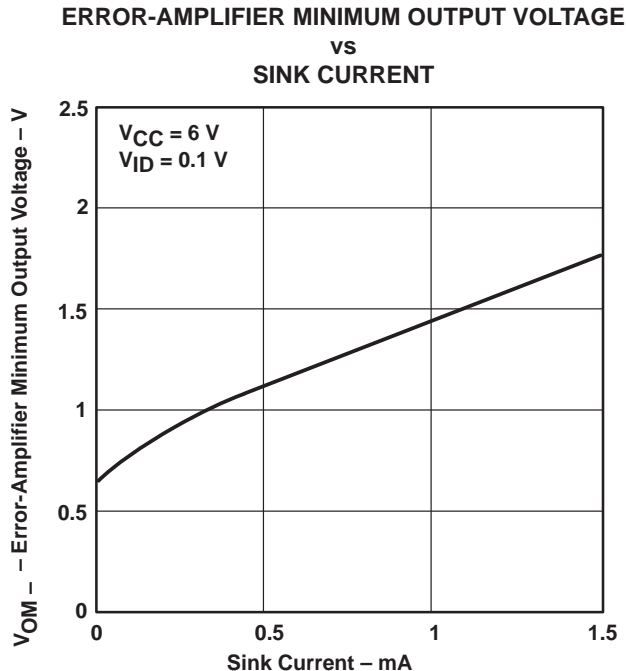


Figure 17

# TL1454, TL1454Y

## DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM)

### CONTROL CIRCUIT

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#### TYPICAL CHARACTERISTICS

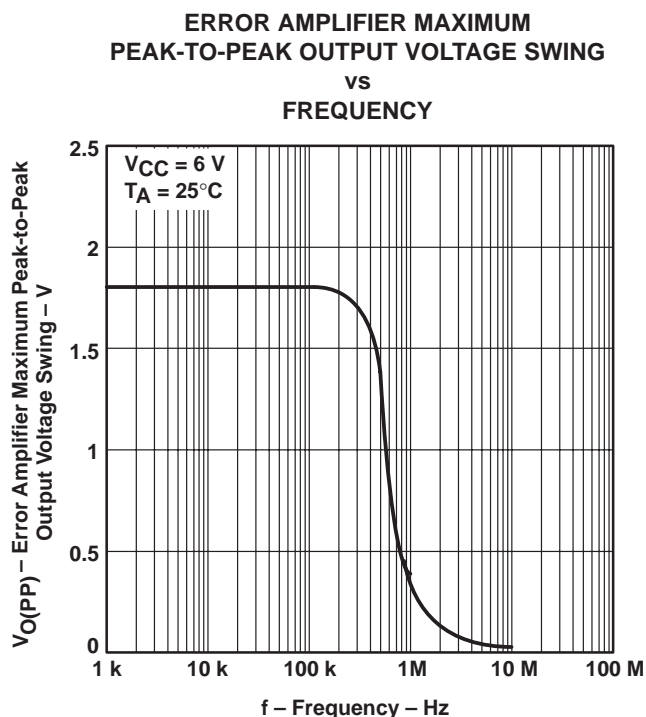


Figure 18

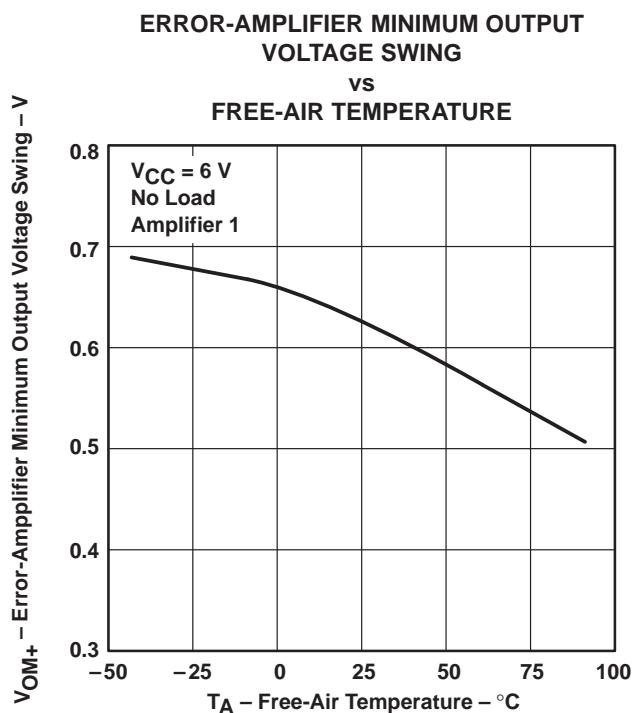


Figure 19

#### ERROR AMPLIFIER OPEN-LOOP GAIN AND PHASE SHIFT

vs  
**FREQUENCY**

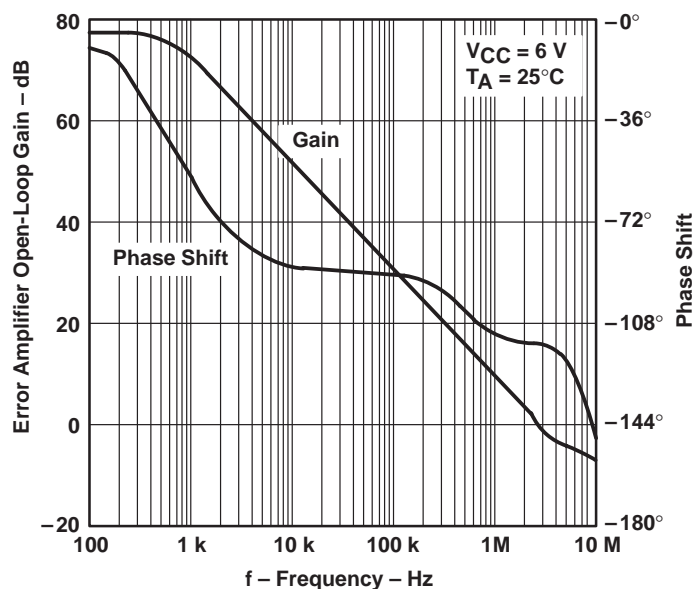


Figure 20





## TYPICAL CHARACTERISTICS

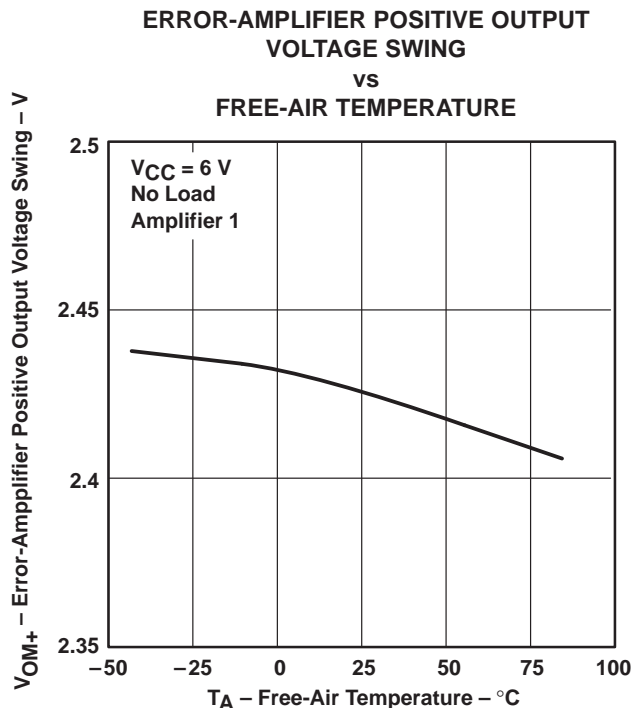


Figure 21

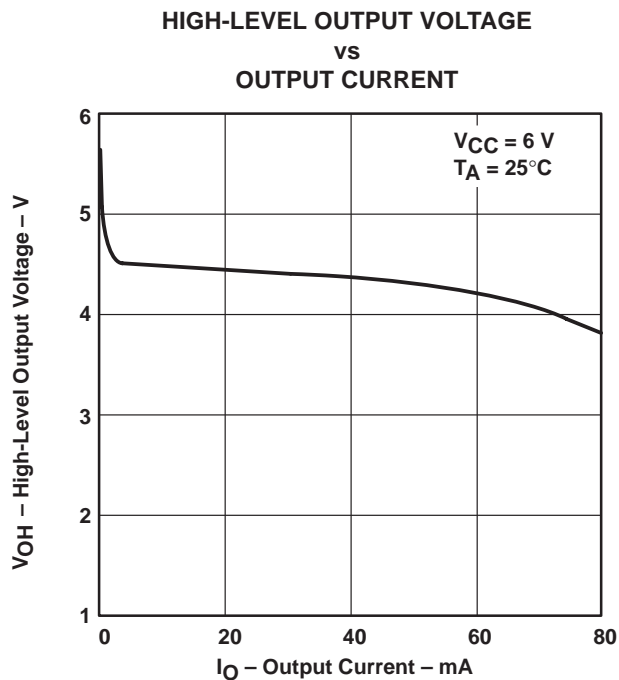


Figure 22

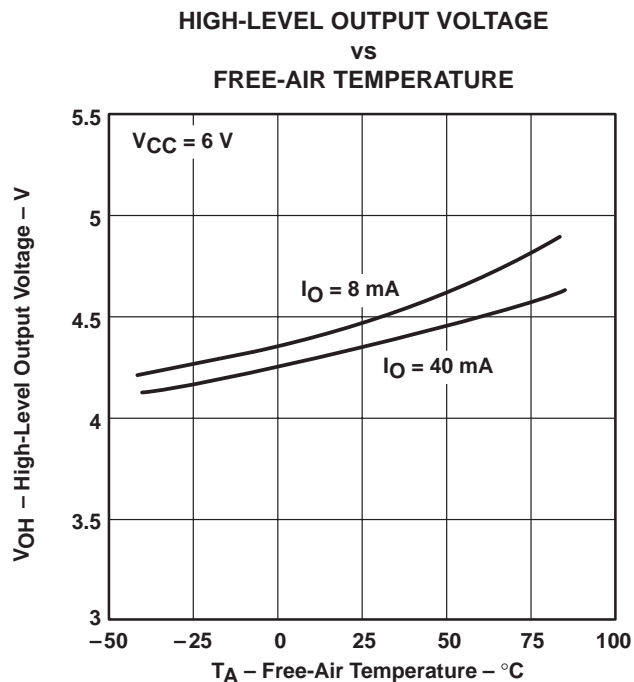


Figure 23

# TL1454, TL1454Y

## DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM)

### CONTROL CIRCUIT

SLVS086B – APRIL 1995 – REVISED NOVEMBER 1997

#### TYPICAL CHARACTERISTICS

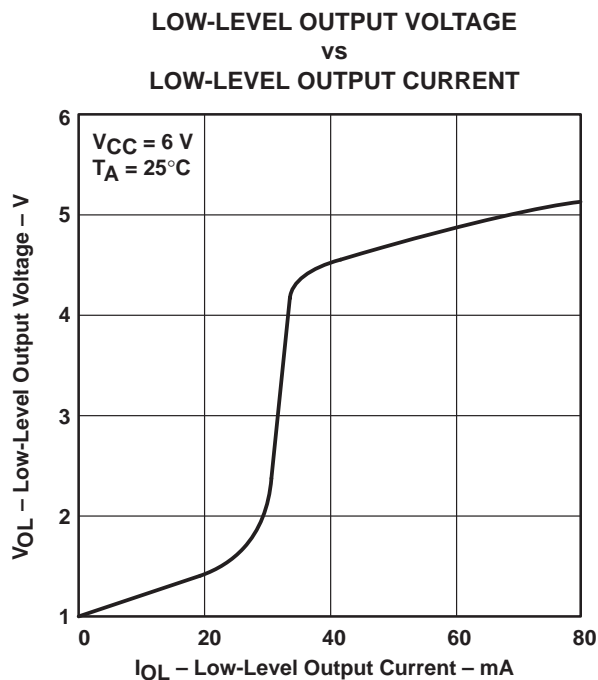


Figure 24

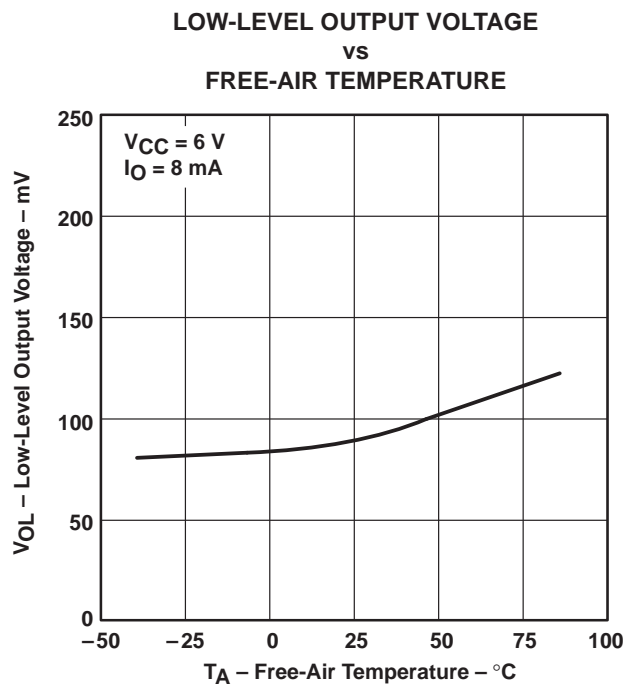


Figure 25

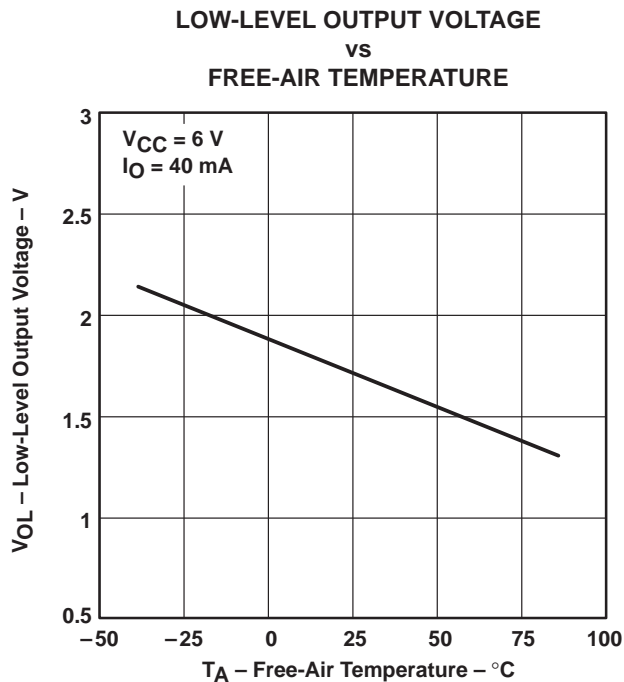


Figure 26

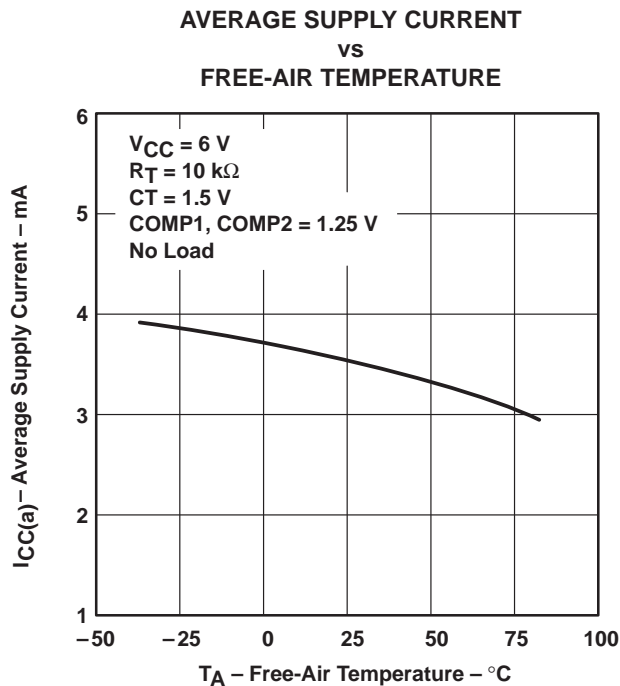


Figure 27

## TYPICAL CHARACTERISTICS

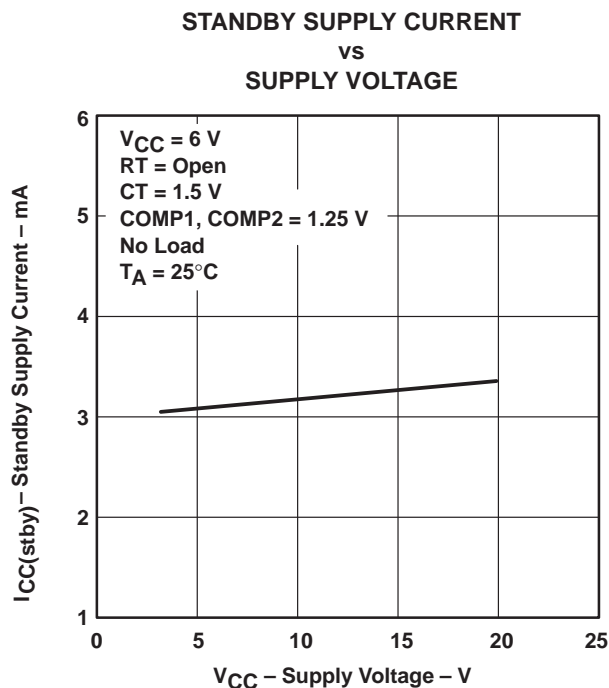


Figure 28

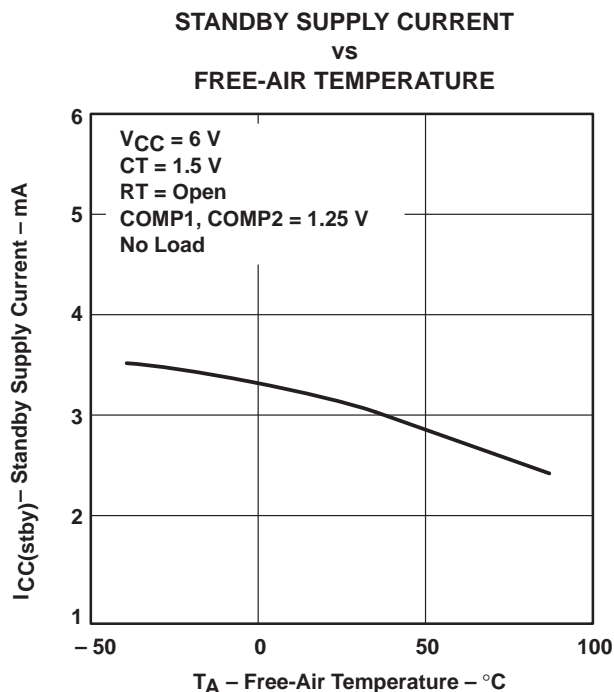


Figure 29

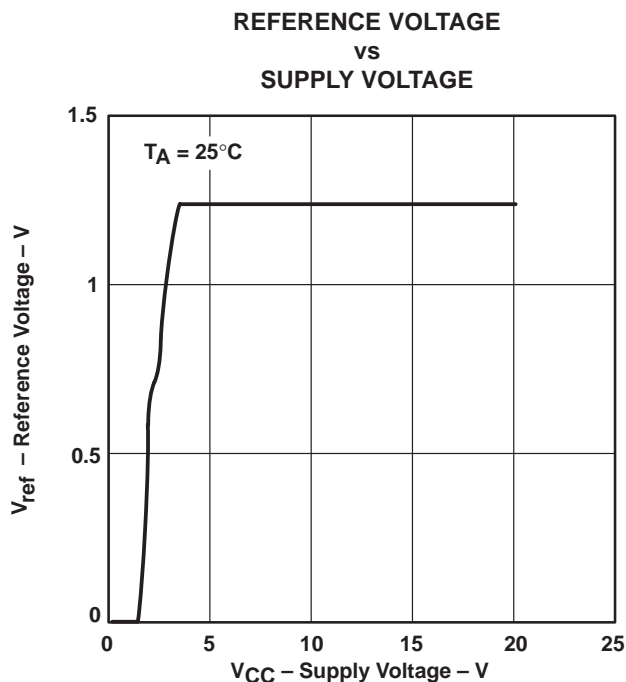


Figure 30

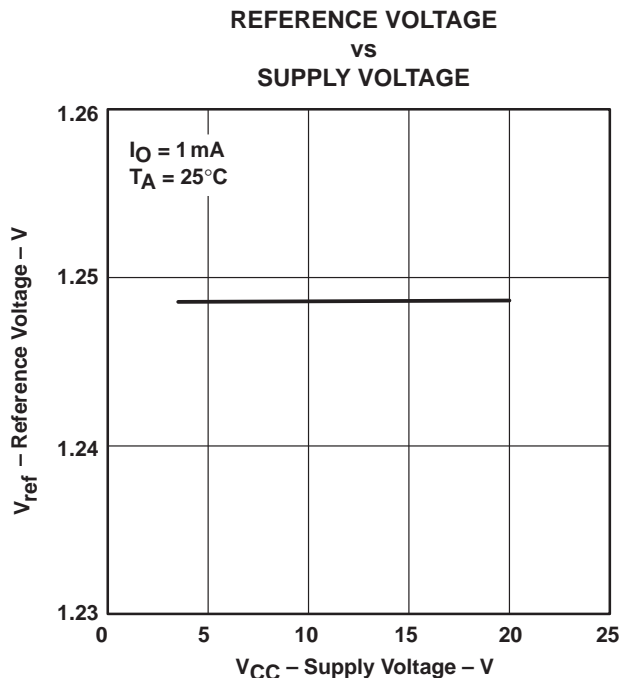


Figure 31

TL1454, TL1454Y  
DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM)  
CONTROL CIRCUIT

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TYPICAL CHARACTERISTICS

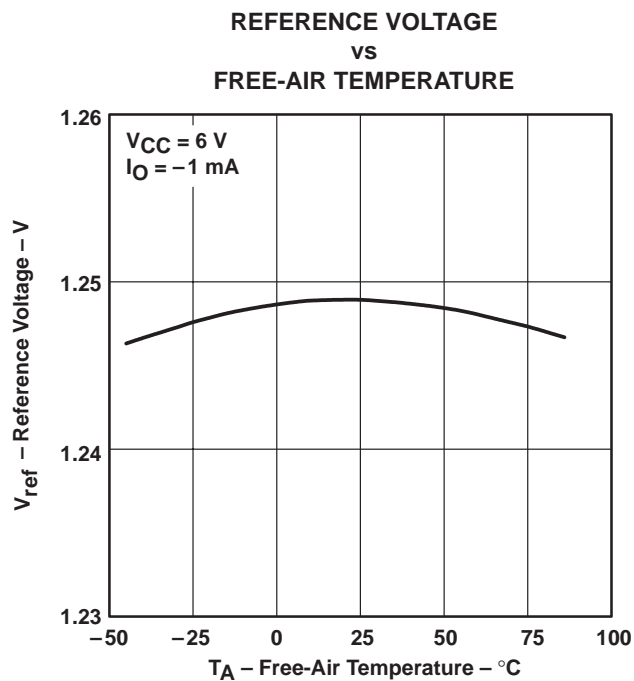


Figure 32

TL1454, TL1454Y  
DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM)  
CONTROL CIRCUIT

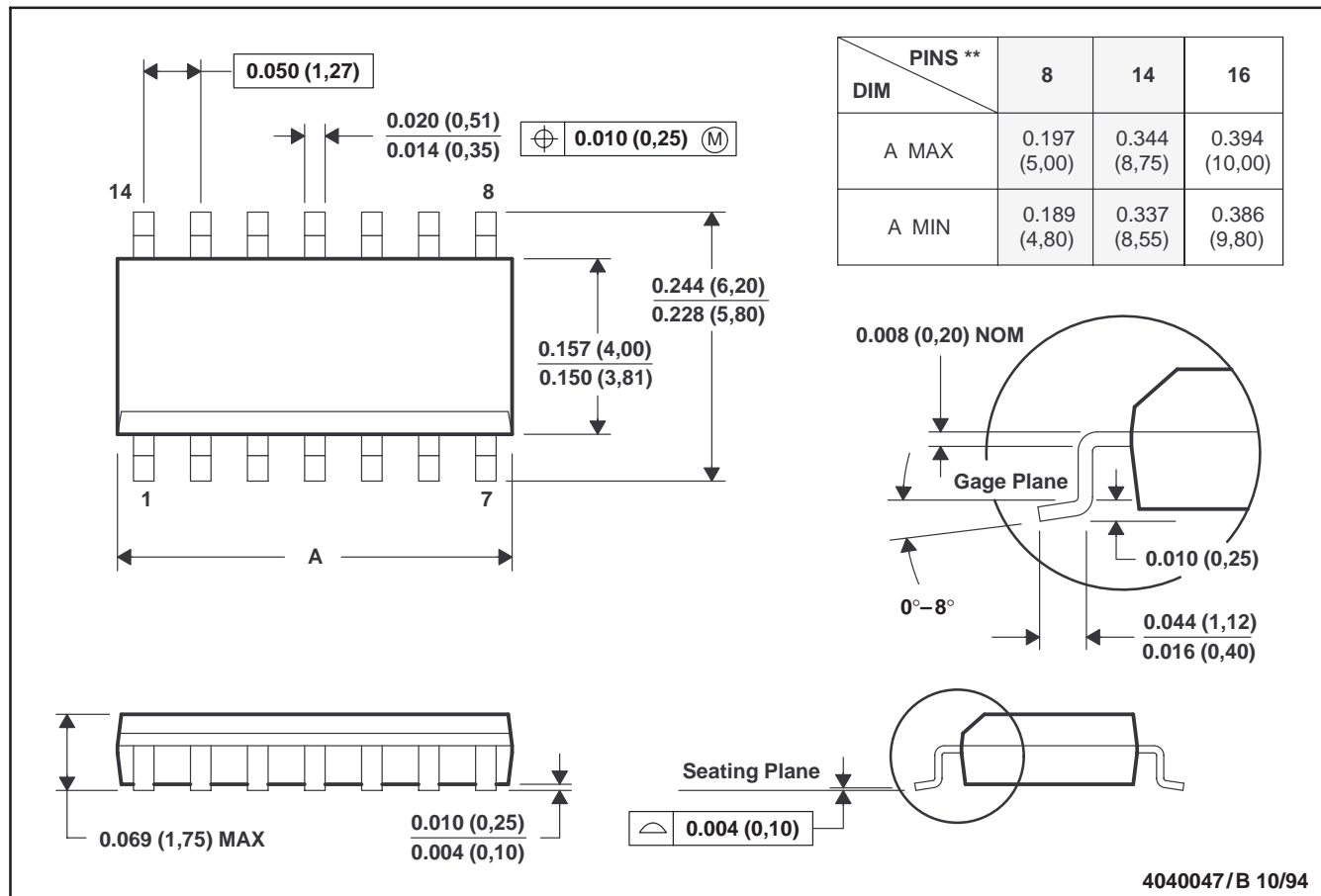
SLVS086B – APRIL 1995 – REVISED NOVEMBER 1997

## MECHANICAL DATA

**D (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Four center pins are connected to die mount pad
  - Falls within JEDEC MS-012

# TL1454, TL1454Y

## DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM)

### CONTROL CIRCUIT

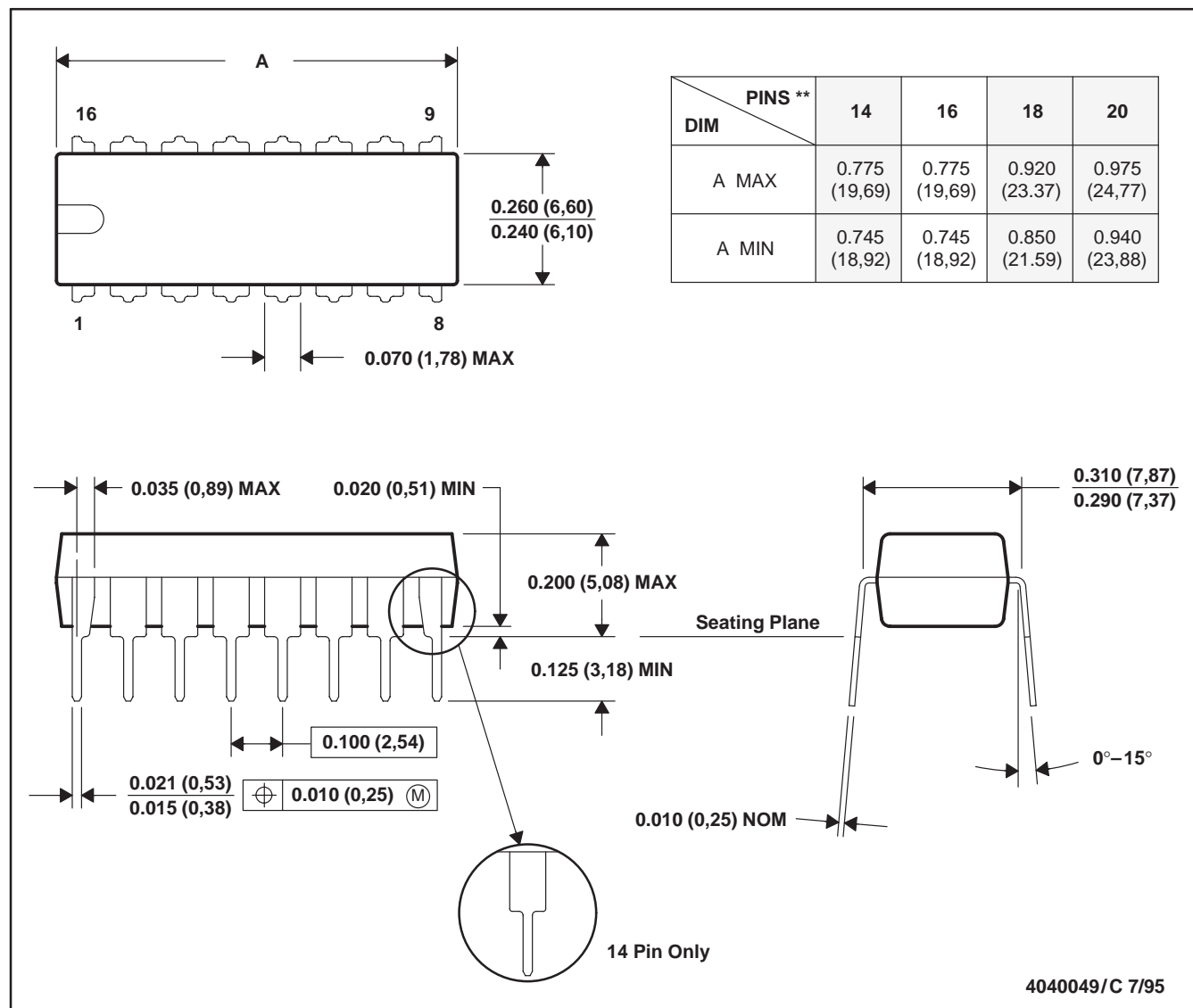
SLVS086B – APRIL 1995 – REVISED NOVEMBER 1997

#### MECHANICAL DATA

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

TL1454, TL1454Y  
DUAL-CHANNEL PULSE-WIDTH-MODULATION (PWM)  
CONTROL CIRCUIT

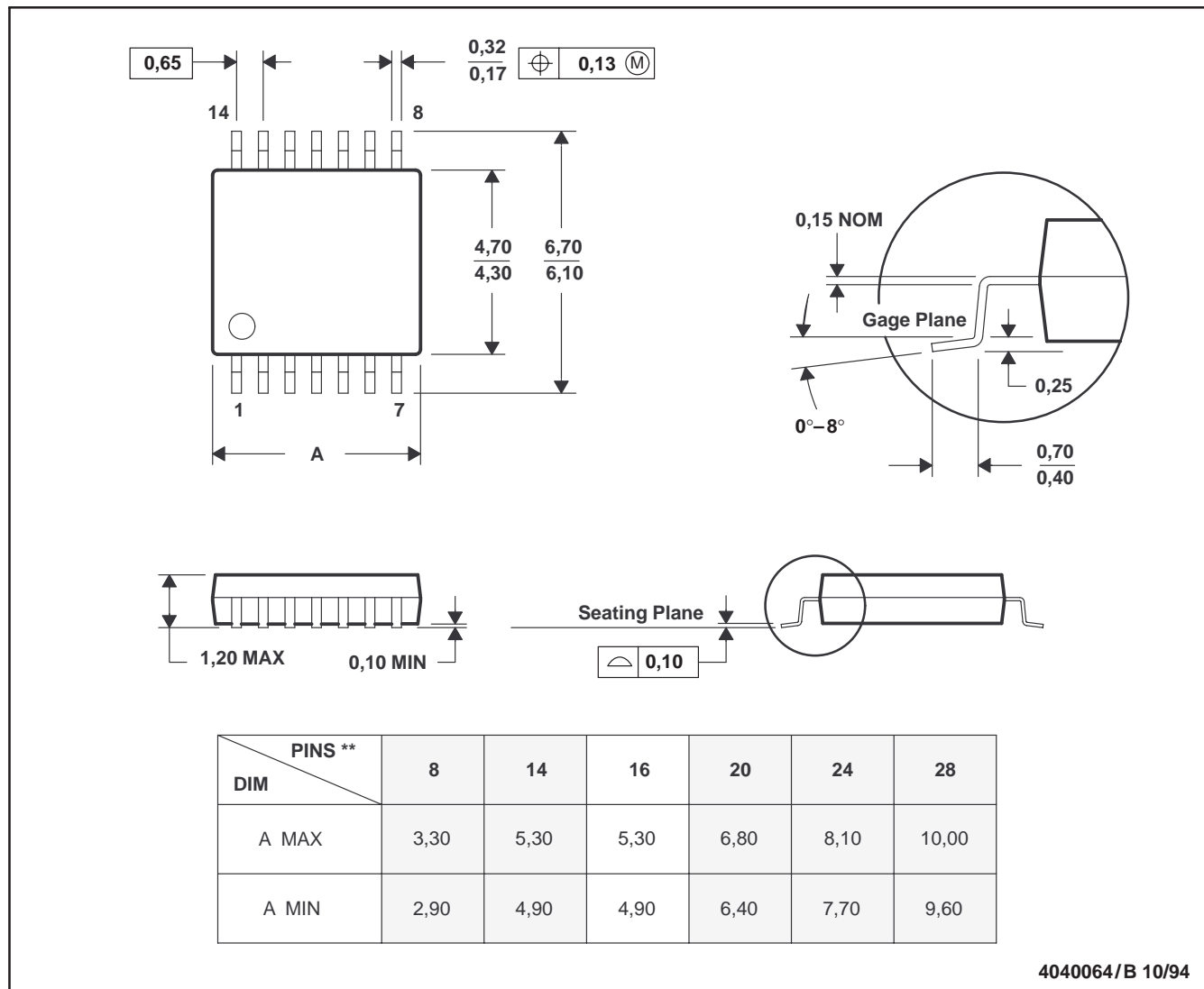
SLVS086B – APRIL 1995 – REVISED NOVEMBER 1997

## MECHANICAL DATA

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

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