SBAS239 – MAY 2002

Self-Calibrating, 16-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE DATA ACQUISITION SYSTEM IN A TINY SOT23-6 PACKAGE
- 16-BITS NO MISSING CODES
- INL: 0.0125% of FSR MAX
- CONTINUOUS SELF-CALIBRATION
- SINGLE-CYCLE CONVERSION
- PROGRAMMABLE GAIN AMPLIFIER GAIN = 1, 2, 4, OR 8
- LOW NOISE: 4μVp-p
- PROGRAMMABLE DATA RATE: 8SPS to 128SPS
- INTERNAL SYSTEM CLOCK
- I²C™ INTERFACE
- POWER SUPPLY: 2.7V TO 5.5V
- LOW CURRENT CONSUMPTION: 90μA

APPLICATIONS

- PORTABLE INSTRUMENTATION
- INDUSTRIAL PROCESS CONTROL
- SMART TRANSMITTERS
- CONSUMER GOODS
- FACTORY AUTOMATION
- TEMPERATURE MEASUREMENT

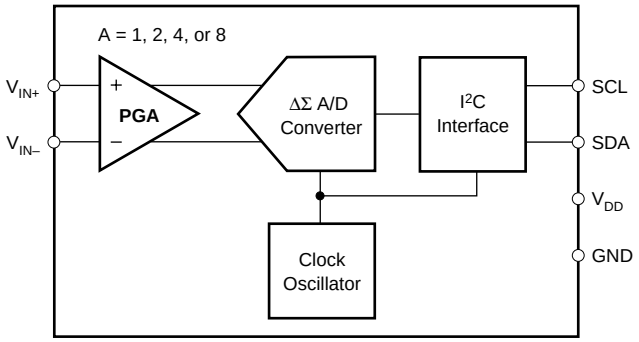
I²C is a registered trademark of Philips Incorporated.

DESCRIPTION

The ADS1100 is a precision, continuously self-calibrating Analog-to-Digital (A/D) converter with differential inputs and up to 16 bits of resolution in a small SOT23-6 package. Conversions are performed ratiometrically, using the power supply as the reference voltage. The ADS1100 uses an I²C-compatible serial interface and operates from a single power supply ranging from 2.7V to 5.5V.

The ADS1100 can perform conversions at rates of 8, 16, 32, or 128 samples per second. The onboard programmable-gain amplifier, which offers gains of up to 8, allows smaller signals to be measured with high resolution. In single-conversion mode, the ADS1100 automatically powers down after a conversion, greatly reducing current consumption during idle periods.

The ADS1100 is designed for applications requiring high-resolution measurement, where space and power consumption are major considerations. Typical applications include portable instrumentation, industrial process control and smart transmitters.



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	–0.3V to +6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
Voltage to GND, V_{IN}+, V_{IN}–	–0.3V to V_{DD} + 0.3V
Voltage to GND, SDA, SCL	–0.5V to 6V
Maximum Junction Temperature	+150°C
Operating Temperature	–40°C to +85°C
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

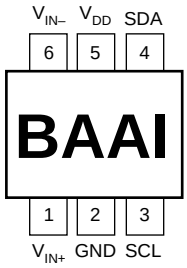
PACKAGE/ORDERING INFORMATION

PRODUCT	I^2C ADDRESS(1)	PACKAGE-LEAD	PACKAGE DESIGNATOR(2)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1100	1001 000	SOT23-6	DBV	–40°C to +85°C	BAAI	ADS1100IDBVT	Tape and Reel, 250
"	"	"	"	"	"	ADS1100IDBVR	Tape and Reel, 3000

NOTES: (1) Contact TI or your local sales representative for more information on the availability of other addresses. (2) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATION

Top View **SOT**



NOTE: Marking text direction indicates pin 1.

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +85°C, V_{DD} = 5V, GND = 0V, all PGAs, unless otherwise noted.

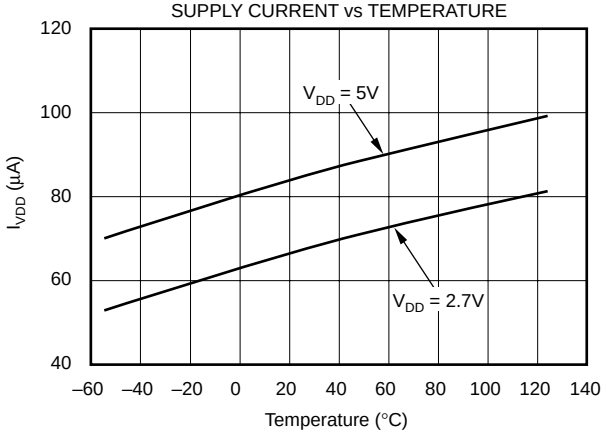
PARAMETER	CONDITIONS	ADS1100 MIN	ADS1100 TYP	ADS1100 MAX	UNITS
ANALOG INPUT					
Full-Scale Input Voltage	$(V_{IN}+) – (V_{IN}–)$		$\pm V_{DD}$/PGA		V
Analog Input Voltage	$V_{IN}+$, $V_{IN}–$ to GND	GND – 0.2		V_{DD} + 0.2	V
Differential Input Impedance			2.4/PGA		MΩ
Common-Mode Input Impedance			8		MΩ
SYSTEM PERFORMANCE					
Resolution and No Missing Codes	DR = 00	12		12	Bits
	DR = 01	14		14	Bits
	DR = 10	15		15	Bits
	DR = 11	16		16	Bits
Conversion Rate	DR = 00	104	128	184	SPS
	DR = 01	26	32	46	SPS
	DR = 10	13	16	23	SPS
	DR = 11	6.5	8	11.5	SPS
Output Noise	See Typical Characteristic Curves				
Integral Nonlinearity	DR = 11, PGA = 1, End Point Fit(1)		±0.003	±0.0125	% of FSR(2)
Offset Error			±2.5/PGA	±5/PGA	mV
Offset Drift	PGA = 1		1.5	8	µV/°C
	PGA = 2		1.0	4	µV/°C
	PGA = 4		0.7	2	µV/°C
	PGA = 8		0.6	2	µV/°C
Gain Error			0.01	0.1	%
Gain Error Drift			2		ppm/°C
Common-Mode Rejection	At DC, PGA = 8	94	100		dB
	At DC, PGA = 1		85		dB
DIGITAL INPUT/OUTPUT					
Logic Level					
V_{IH}		0.7 • V_{DD}		6	V
V_{IL}		GND – 0.5		0.3 • V_{DD}	V
V_{OL}	I_{OL} = 3mA	GND		0.4	V
Input Leakage					
I_{IH}	V_{IH} = 5.5V			10	µA
I_{IL}	V_{IL} = GND	–10			µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	V_{DD}	2.7		5.5	V
Supply Current	Power Down		0.05	2	µA
	Active Mode		90	150	µA
Power Dissipation					
	V_{DD} = 5.0V		450	750	µW
	V_{DD} = 3.0V		210		µW

NOTES: (1) 99% of full-scale. (2) FSR = Full-Scale Range = 2 • V_{DD}/PGA.

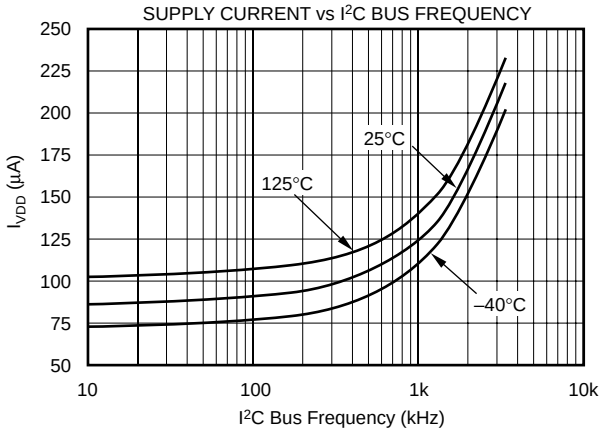
TYPICAL CHARACTERISTICS

At T_A = 25°C, V_{DD} = 5V, unless otherwise noted.

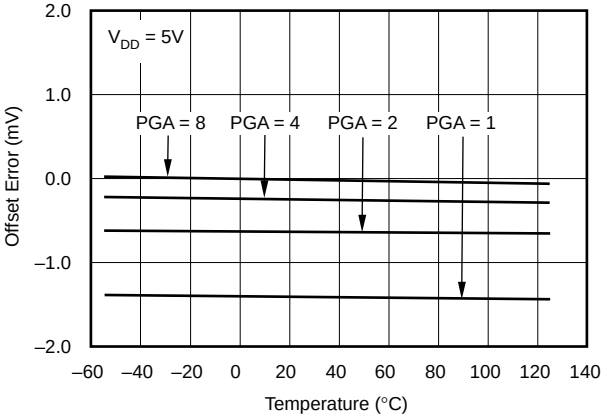
SUPPLY CURRENT vs TEMPERATURE



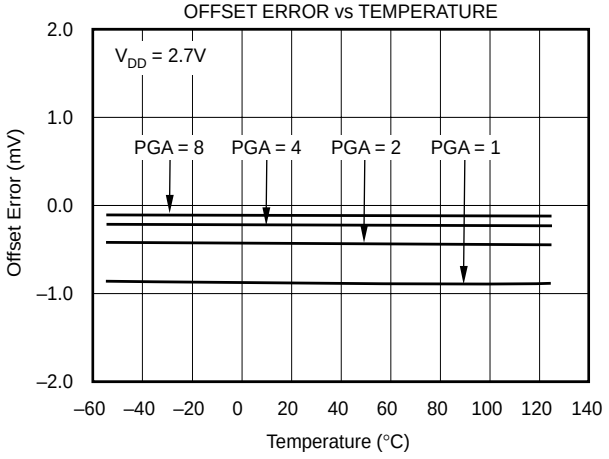
SUPPLY CURRENT vs I^2C BUS FREQUENCY



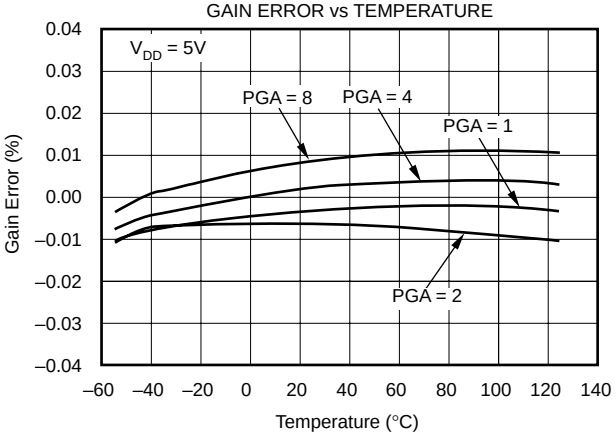
OFFSET ERROR vs TEMPERATURE



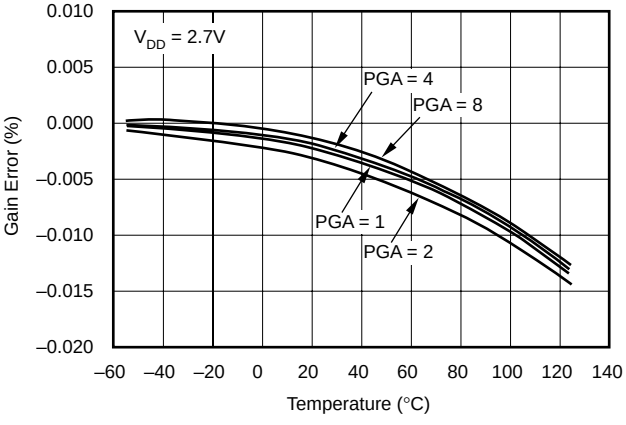
OFFSET ERROR vs TEMPERATURE



GAIN ERROR vs TEMPERATURE



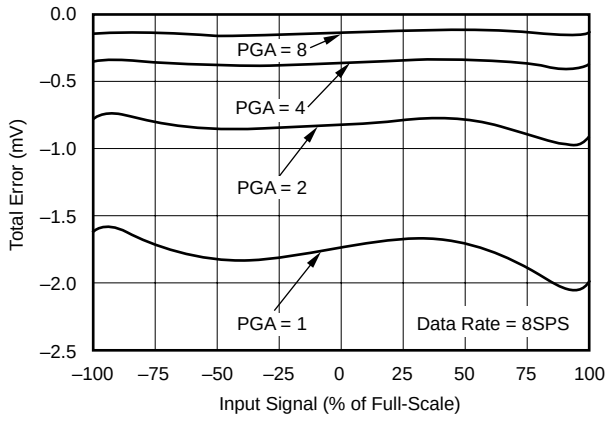
GAIN ERROR vs TEMPERATURE



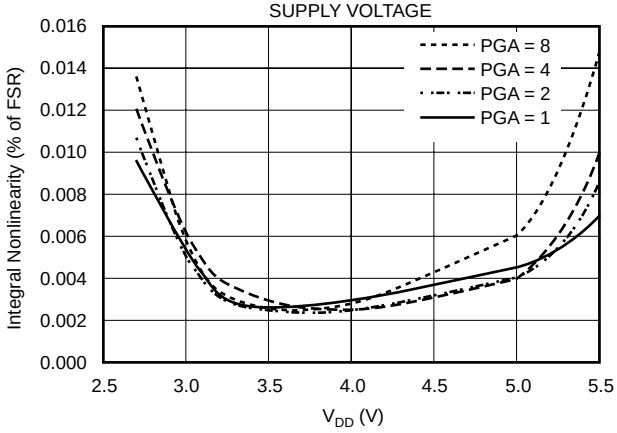
TYPICAL CHARACTERISTICS

At T_A = 25°C, V_{DD} = 5V, unless otherwise noted.

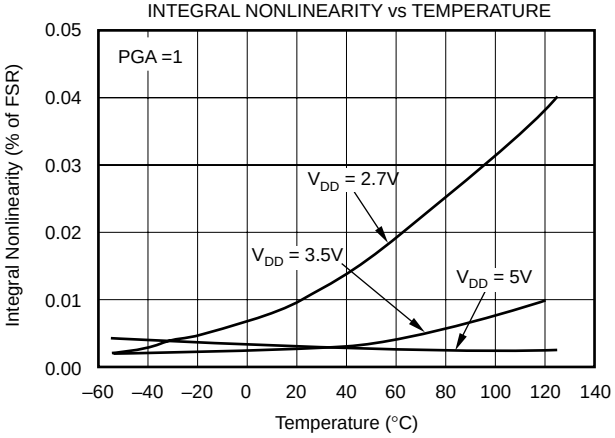
TOTAL ERROR vs INPUT SIGNAL



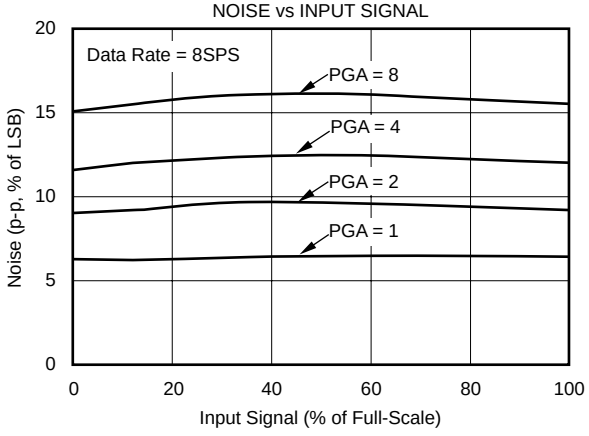
INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE



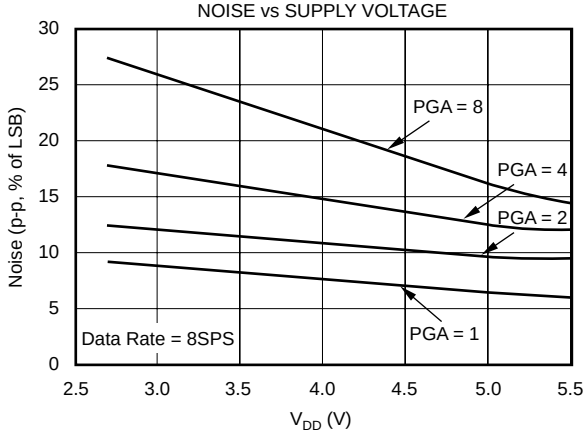
INTEGRAL NONLINEARITY vs TEMPERATURE



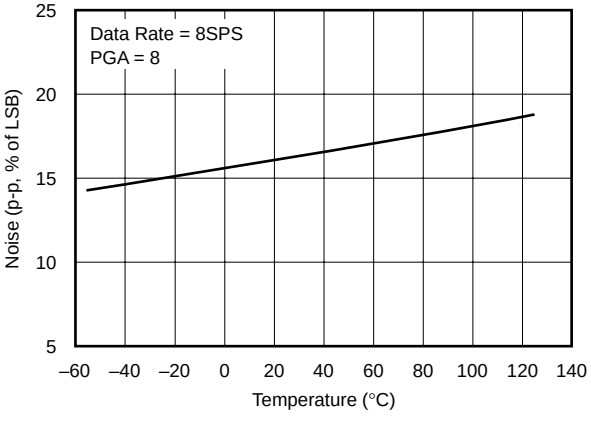
NOISE vs INPUT SIGNAL



NOISE vs SUPPLY VOLTAGE

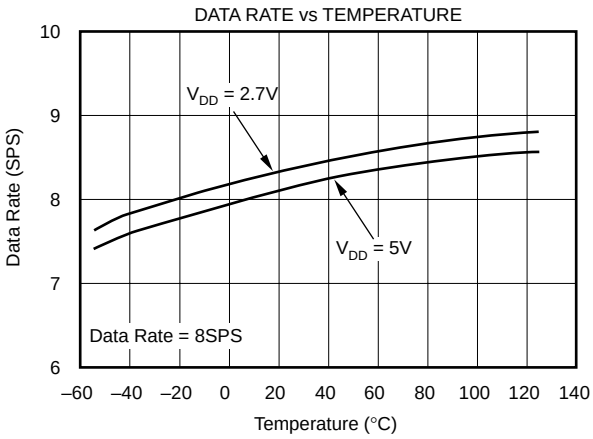


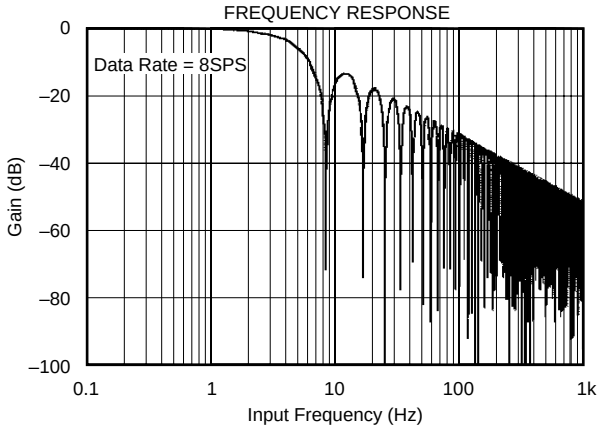
NOISE vs TEMPERATURE



TYPICAL CHARACTERISTICS

At T_A = 25°C, V_{DD} = 5V, unless otherwise noted.





THEORY OF OPERATION

The ADS1100 is a fully differential, 16-bit, self-calibrating, delta-sigma A/D converter. Extremely easy to design with and configure, the ADS1100 allows you to take high-quality measurements with a minimum of effort.

The ADS1100 consists of a delta-sigma A/D converter core with adjustable gain, a clock generator, and an I²C interface. Each of these blocks are described in detail in the sections that follow.

ANALOG-TO-DIGITAL CONVERTER

The ADS1100's A/D converter core consists of a differential switched-capacitor delta-sigma modulator followed by a digital filter. The modulator measures the difference between the positive and negative analog inputs and compares this to a reference voltage, which, in the ADS1100, is the power supply. The digital filter receives a high-speed bitstream from the modulator and outputs a *code*, which is a number proportional to the input voltage.

OUTPUT CODE CALCULATION

The output code is a scalar value which is (except for clipping) proportional to the voltage difference between the two analog inputs. The output code is confined to a finite range of numbers; this range depends on the number of bits needed to represent the code. The number of bits needed to represent the output code for the ADS1100 depends on the data rate, as shown in Table I.

Data rate	Number of Bits	Minimum Code	Maximum Code
8SPS	16	–32768	32767
16SPS	15	–16384	16383
32SPS	14	–8192	8191
128SPS	12	–2048	2047

TABLE I. Minimum and Maximum Codes.

For a minimum output code of Min Code, gain setting of PGA, positive and negative input voltages of V_{IN+} and V_{IN-}, and power supply of V_{DD}, the output code is given by the expression:

$$\text{Output Code} = -1 \bullet \text{Min Code} \bullet \text{PGA} \bullet \frac{(V_{IN+}) - (V_{IN-})}{V_{DD}}$$

In the above expression, it is important to note that the *negated minimum* output code is used. The ADS1100 outputs codes in binary two's complement format, so the absolute values of the minima and maxima are not the same; the maximum n-bit code is $2^{n-1} - 1$, while the minimum n-bit code is $-1 \bullet 2^{n-1}$.

For example, the ideal expression for output codes with a data rate of 16SPS and PGA = 2 is:

$$\text{Output Code} = 16384 \bullet 2 \bullet \frac{(V_{IN+}) - (V_{IN-})}{V_{DD}}$$

The ADS1100 outputs all codes right-justified and sign-extended. This arrangement makes it possible to perform averaging on the higher data rate codes using only a 16-bit accumulator.

Output codes for various input levels are shown in Table II.

SELF-CALIBRATION

The previous expressions for the ADS1100's output code do not account for the gain and offset errors in the modulator. To compensate for these, the ADS1100 incorporates self-calibration circuitry.

The self-calibration system operates continuously, and requires no user intervention. No adjustments can be made to the self-calibration system, and none need to be made. The self-calibration system cannot be deactivated.

The offset and gain error figures shown in the specifications table include the effects of calibration.

CLOCK GENERATOR

The ADS1100 features an onboard clock generator, which drives the operation of the modulator and digital filter. The Typical Characteristics show varieties in data rate over supply voltage and temperature.

It is not possible to operate the ADS1100 with an external modulator clock.

INPUT IMPEDANCE

The ADS1100 uses a switched-capacitor input stage. To external circuitry, it looks roughly like a resistance. The resistance value, as with all switched-capacitor circuits, depends on the capacitor values and the rate at which they are switched. The switching frequency is the same as the modulator frequency; the capacitor values depend on the PGA setting. The switching clock is generated by the onboard clock generator, so its frequency, nominally 275 kHz, is somewhat dependent on supply voltage and temperature.

	Input Signal				
Data Rate	Negative Full-Scale	–1 LSB	Zero	+1 LSB	Positive Full-Scale
8 SPS	8000_H	$FFFF_H$	0000_H	0001_H	$7FFF_H$
16 SPS	$C000_H$	$FFFF_H$	0000_H	0001_H	$3FFF_H$
32 SPS	$E000_H$	$FFFF_H$	0000_H	0001_H	$1FFF_H$
128 SPS	$F800_H$	$FFFF_H$	0000_H	0001_H	$07FF_H$

TABLE II. Output Codes for Different Input Signals.

The common-mode and differential input impedances are different. For a gain setting of PGA, the differential input impedance is typically:

$$2.4M\Omega / PGA$$

The common mode impedance is typically 8MΩ.

The typical value of the input impedance often cannot be neglected. Unless the input source has a low impedance, the ADS1100's input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Bear in mind, however, that active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock generator frequency drifts slightly with temperature, the input impedances will also drift. For many applications, this input impedance drift can be neglected, and the typical impedance values above can be used.

ALIASING

If frequencies are input to the ADS1100 which exceed half the data rate, aliasing will occur. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited, for example, a thermocouple's output, which has a limited rate of change, but may nevertheless contain noise and interference components. These can fold back into the sampling band just as any other signal can.

The ADS1100's digital filter provides some attenuation of high frequency noise, but the filter's $sinc^1$ frequency response cannot completely replace an anti-aliasing filter; some external filtering may still be needed. For many applications, a simple RC filter will suffice.

When designing an input filter circuit, remember to take the interaction between the filter network and the input impedance of the ADS1100 into account.

USING THE ADS1100

OPERATING MODES

The ADS1100 operates in one of two modes: *continuous conversion* and *single conversion.*

In continuous conversion mode, the ADS1100 continuously performs conversions. Once a conversion has been completed, the ADS1100 places the result in the output register, and immediately begins another conversion. When the ADS1100 is in continuous conversion mode, the ST/BSY bit in the configuration register always reads 1.

In single conversion mode, the ADS1100 waits until the ST/BSY bit in the conversion register is set to 1. When this happens, the ADS1100 powers up and performs a single conversion. After the conversion completes, the ADS1100 places the result in the output register, resets the ST/BSY bit to 0 and powers down. Writing a 1 to ST/BSY while a conversion is in progress has no effect.

When switching from continuous conversion mode to single conversion mode, the ADS1100 will complete the current conversion, reset the ST/BSY bit to 0 and power down.

RESET AND POWER-UP

When the ADS1100 powers up, it automatically performs a reset. As part of the reset, the ADS1100 sets all of the bits in the configuration register to their default setting.

The ADS1100 responds to the I^2C General Call Reset command. When the ADS1100 receives a General Call Reset, it performs an internal reset, exactly as though it had just been powered on.

I^2C INTERFACE

The ADS1100 communicates through an I^2C (Inter-Integrated Circuit) interface. The I^2C interface is a 2-wire open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW, by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pull-up resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the *master* and the other acting as the *slave.* Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the ADS1100 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the bit's level while SCL is LOW. (A LOW on SDA indicates a zero bit; a HIGH indicates a one bit.) Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1100 never drives SCL, because it cannot act as a master. On the ADS1100, SCL is an input only.

Most of the time the bus is *idle,* no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is *active*. Only master devices can start a communication. They do this by causing a *start condition* on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a *start condition* or its counterpart, a *stop condition.* A start condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A stop condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a start condition, it sends a byte which indicates which slave device it wants to communicate with. This byte is called the *address byte.* Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specifi-

cation for details.) The master sends an address in the address byte, together with a bit which indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I²C bus, whether it be address or data, is acknowledged with an *acknowledge bit.* When a master has finished sending a byte, eight data bits, to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (Remember that the master *always* drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not-acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a stop condition. When a stop condition is issued, the bus becomes idle again. A master may also issue another start condition. When a start condition is issued while the bus is active, it is called a *repeated start condition.*

A timing diagram for an ADS1100 I²C transaction is shown in Figure 1. Table III gives the parameters for this diagram.

ADS1100 I²C ADDRESS

The ADS1100's I²C address is 1001*aaa*, where *aaa* are bits set at the factory. The ADS1100 is shipped with *aaa* set to zero, so its address is 1001000.

Contact Texas Instruments for information about the availability of other addresses.

I²C GENERAL CALL

The ADS1100 responds to General Call Reset, which is an address byte of 00_H followed by a data byte of 06_H. The ADS1100 acknowledges both bytes.

On receiving a General Call Reset, the ADS1100 performs a full internal reset, just as though it had been powered off and then on. If a conversion is in process, it is interrupted; the output register is set to zero; and the configuration register is set to its default setting.

The ADS1100 always acknowledges the General Call address byte of 00_H, but it does not acknowledge any General Call data bytes other than 04_H or 06_H.

I²C DATA RATES

The I²C bus operates in one of three speed modes: Standard, which allows a clock frequency of up to 100kHz; Fast, which allows a clock frequency of up to 400kHz; and High-

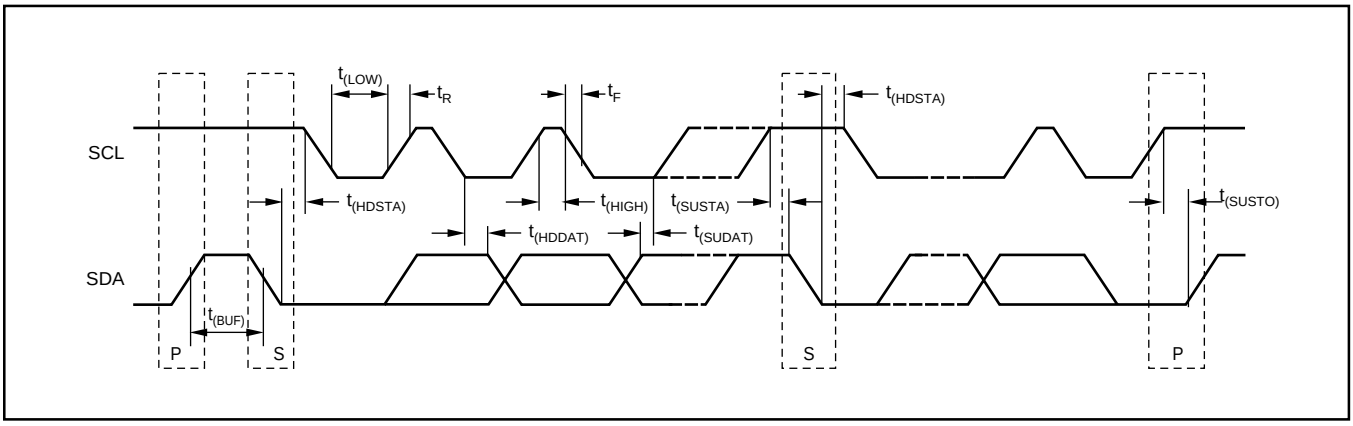


FIGURE 1. I²C Timing Diagram.

PARAMETER		FAST MODE MIN	FAST MODE MAX	HIGH-SPEED MODE MIN	HIGH-SPEED MODE MAX	UNITS
SCLK Operating Frequency	$f_{(SCLK)}$		0.4		3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold Time After Repeated START Condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	600		160		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	600		160		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	600		160		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCLK Clock LOW Period	$t_{(LOW)}$	1300		160		ns
SCLK Clock HIGH Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns

TABLE III. Timing Diagram Definitions.

speed mode (also called Hs mode), which allows a clock frequency of up to 3.4MHz. The ADS1100 is fully compatible with all three modes.

No special action needs to be taken to use the ADS1100 in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001XXX following the start condition, where the XXX bits are unique to the Hs-capable master. This byte is called the Hs master code. (Note that this is different from normal address bytes: the low bit does not indicate read/write status.) The ADS1100 will not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. On receiving a master code, the ADS1100 will switch on its High-speed mode filters, and will communicate at up to 3.4MHz. The ADS1100 switches out of Hs mode with the next stop condition.

For more information on High-speed mode, consult the I²C specification.

REGISTERS

The ADS1100 has two registers which are accessible via its I²C port. The *output register* contains the result of the last conversion; the *configuration register* allows you to change the ADS1100's operating mode and query the status of the device.

OUTPUT REGISTER

The 16-bit output register contains the result of the last conversion in binary two's complement format. Following reset or power-up, the output register is cleared to zero; it remains zero until the first conversion is completed. Therefore, if you read the ADS1100 just after reset or power-up, you will read zero from the output register.

The output register's format is shown in Table V.

CONFIGURATION REGISTER

You can use the 8-bit configuration register to control the ADS1100's operating mode, data rate, and PGA settings. The configuration register's format is shown in Table IV. The default setting is 8CH.

BIT	7	6	5	4	3	2	1	0
NAME	ST/BSY	0	0	SC	DR1	DR0	PGA1	PGA0

TABLE IV. Configuration Register.

Bit 7: ST/BSY

The meaning of the ST/BSY bit depends on whether it is being written to or read from.

In single conversion mode, writing a 1 to the ST/BSY bit causes a conversion to start, and writing a 0 has no effect. In continuous conversion mode, the ADS1100 ignores the value written to ST/BSY.

When read in single conversion mode, ST/BSY indicates whether the A/D converter is busy taking a conversion. If ST/BSY is read as 1, the A/D converter is busy, and a conversion is taking place; if 0, no conversion is taking place, and the result of the last conversion is available in the output register.

In continuous mode, ST/BSY is always read as 1.

Bits 6-5: Reserved

Bits 6 and 5 must be set to zero.

Bit 4: SC

SC controls whether the ADS1100 is in continuous conversion or single conversion mode. When SC is 1, the ADS1100 is in single conversion mode; when SC is 0, the ADS1100 is in continuous conversion mode. The default setting is 0.

Bits 3-2: DR

Bits 3 and 2 control the ADS1100's data rate, as shown in Table VI.

DR1	DR0	DATA RATE
0	0	128SPS
0	1	32SPS
1	0	16SPS
1(1)	1(1)	8SPS(1)
NOTE: (1) Default Setting		

TABLE VI. DR Bits.

Bits 1-0: PGA

Bits 1 and 0 control the ADS1100's gain setting, as shown in Table VII.

PGA1	PGA0	GAIN
0(1)	0(1)	1(1)
0	1	2
1	0	4
1	1	8
NOTE: (1) Default Setting.		

TABLE VII. PGA Bits.

READING FROM THE ADS1100

You can read the output register and the contents of the configuration register from the ADS1100. To do this, address the ADS1100 for reading, and read three bytes from the device. The first two bytes are the output register's contents; the third byte is the configuration register's contents.

You do not always have to read three bytes from the ADS1100. If you want only the contents of the output register, read only two bytes.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

TABLE V. Output Register.

Reading more than three bytes from the ADS1100 has no effect. All of the bytes beginning with the fourth will be FF_H.

A timing diagram for an ADS1100 read operation is shown in Figure 2.

WRITING TO THE ADS1100

You can write new contents into the configuration register (you cannot change the contents of the output register). To do this, address the ADS1100 for writing, and write one byte to it. This byte is written into the configuration register.

Writing more than one byte to the ADS1100 has no effect. The ADS1100 will ignore any bytes sent to it after the first one, and it will only acknowledge the first byte.

A timing diagram for an ADS1100 write operation is shown in Figure 3.

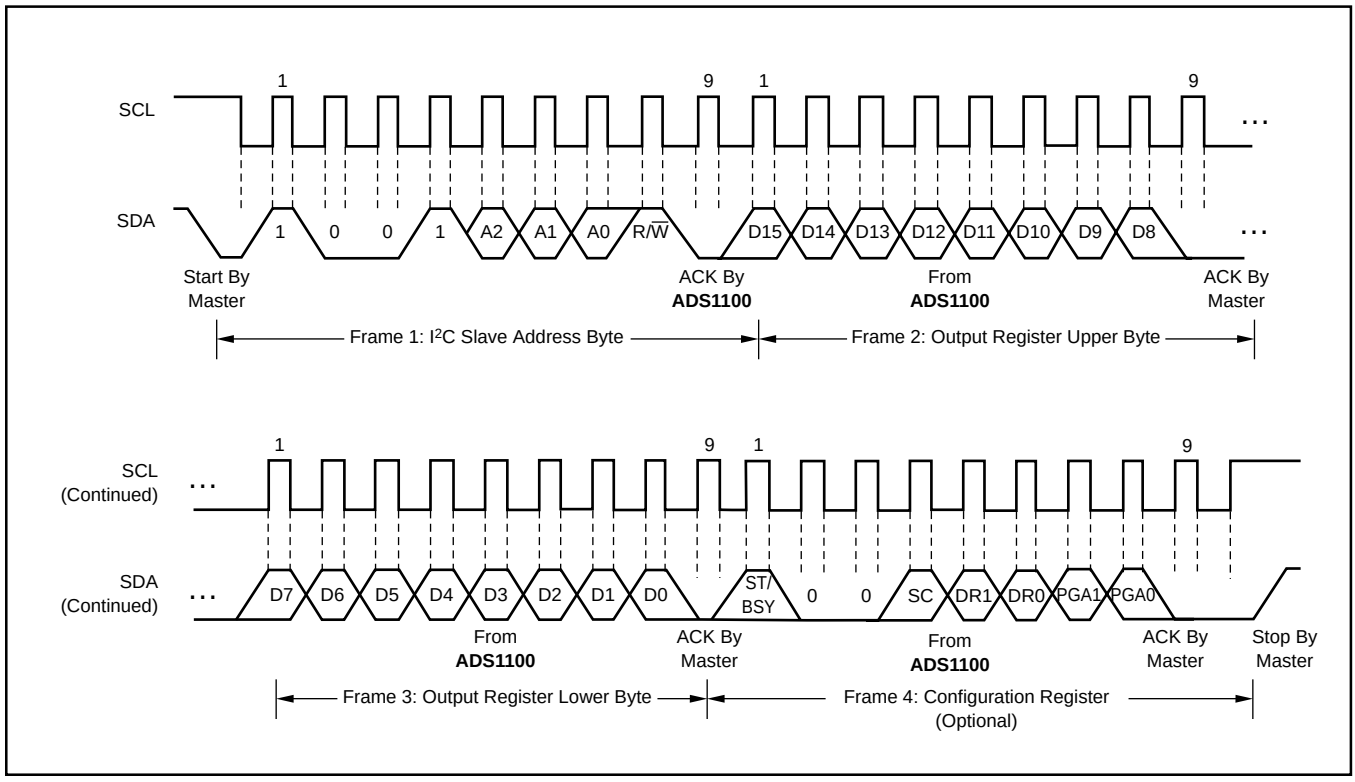


FIGURE 2. Timing Diagram for Reading From the ADS1100.

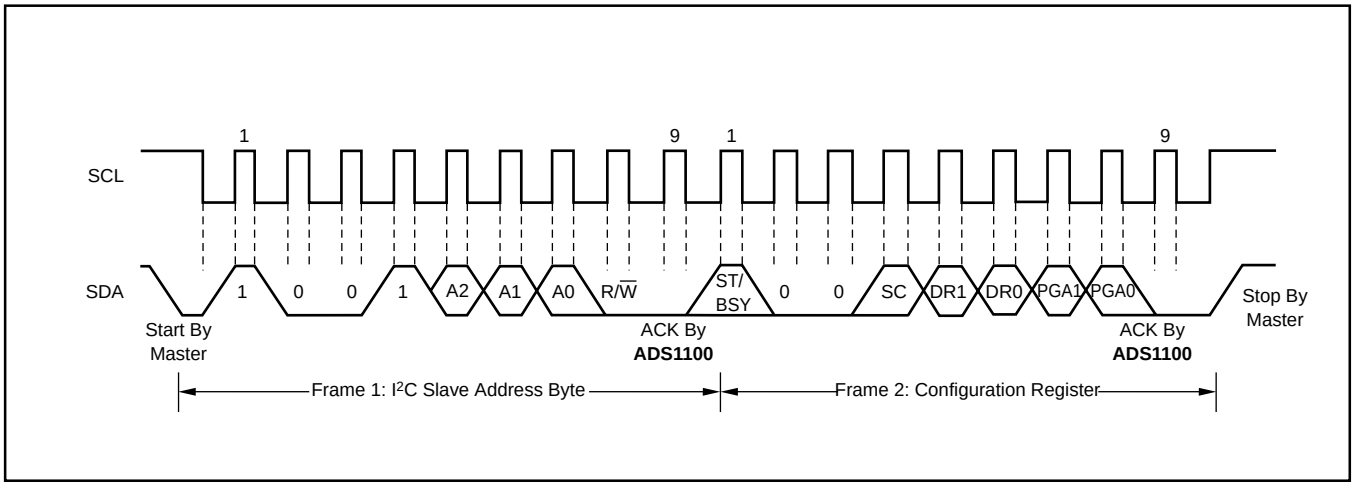
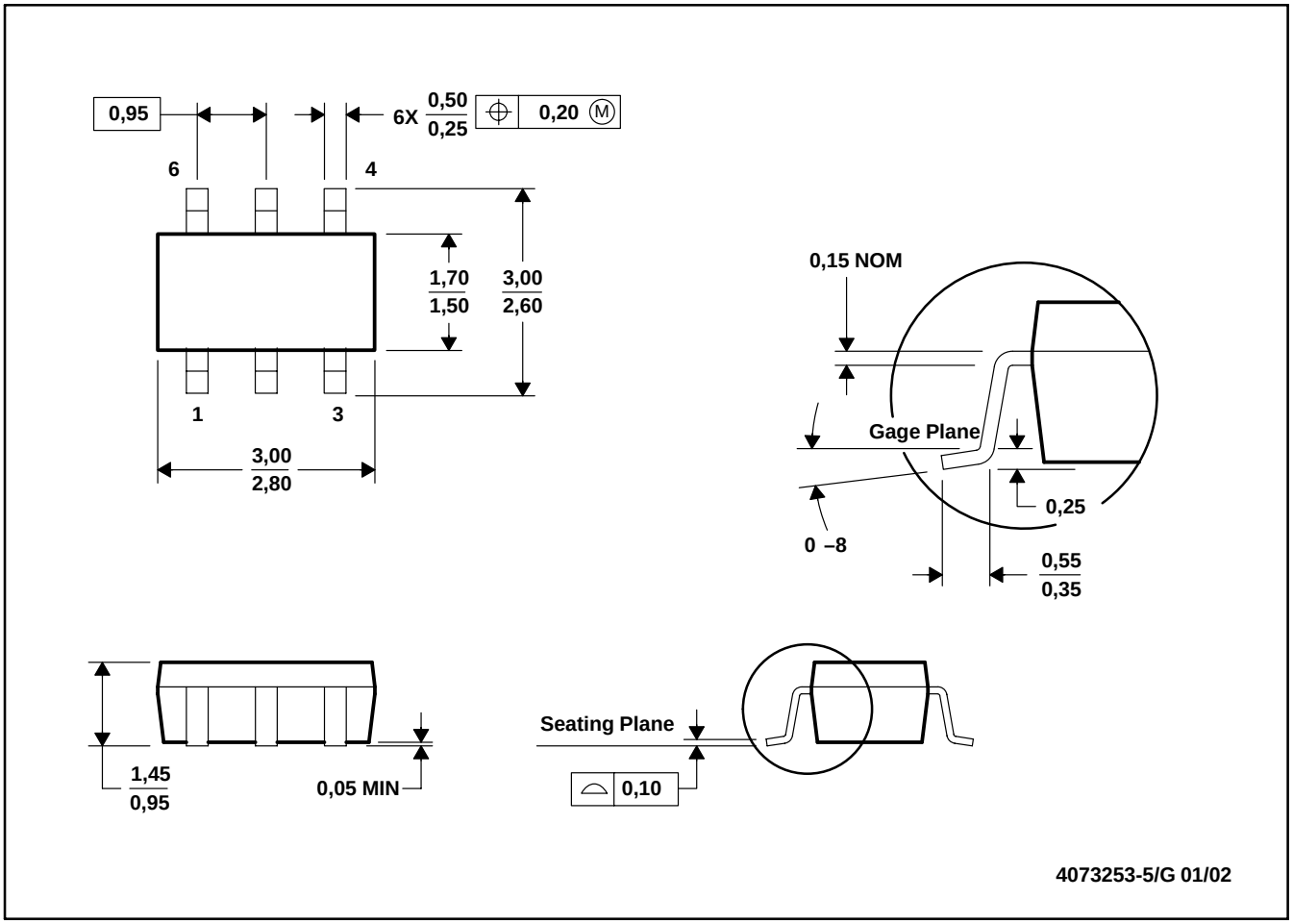


FIGURE 3. Timing Diagram for Writing to the ADS1100.

DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265