SUN MICROELECTRONICS

STP1021A

July 1997

SuperSPARC™-II

DATA SHEET — SPARC v8 32-Bit Superscalar Microprocessor

DESCRIPTION

The STP1021A is a new member of the SuperSPARC-II family of microprocessor products. Like its predecessors (STP1020N, STP1020 and STP1021) this new part is fully SPARC Version 8 compliant and is completely upward compatible with the earlier SPARC Version 7 implementations running over 9,400 SPARC applications and development tools.

The STP1021A is a highly integrated, high performance superscalar microprocessor designed using a state-of-the-art BiCMOS process. Through this high integration the entire processor subsystem is implemented on a single chip, including integer and floating point execution units, separate instruction and data memory management units (MMU), large level-1 instruction and data caches (total of 36 KBytes of cache memory), and a bus interface unit for supporting VBus are implemented on a single chip. This high level of integration reduces the cost of the processor subsystem and increases the overall system reliability by reducing the total number of devices required in the system.

Features	*Benefits*
• High performance superscalar engine with 75 and 85 operating frequency	• Delivers 140 SPECint92 and 135 SPECfp92 at 85MHz
• Large register window (8 windows / 136 registers)	• Fewer loads/stores, fast procedure calls/context switches
• On-chip SPARC Reference MMU	• Support for virtual memory and protection
• High performance IEEE754 floating-point unit	• Increased performance for floating-point intensive applications
• Large on-chip instruction and data caches (20 KByte I-cache and 16 KByte D-cache)	• Increased performance for variety of applications by decoupling processor from slower main memory
• Large store buffer	• Reduces processor wait cycles on store operations
• Hardware integer multiply and divide	• Increased performance for many applications
• Cache coherency support for multi-processing	• Allows a wide range of scalable systems to be built
• Built-In Self Test (BIST) logic	• Provides quick check of device integrity
• Full JTAG interface (IEEE1149.1)	• Provides better testability at the board/system level
• Enhanced boundary scan	• Combines SRAM test mode, BSCAN and functional test to provide module and system level testing and debug
• Stop mode	• Stop at any desired cycle, scan dump
• Performance Monitoring	• Provides counter for instructions and cycle count

The STP1021A is intended for use in a broad range of applications from uniprocessor systems to large multiprocessor systems. Uniprocessor and multiprocessor systems can be built with STP1021A processor in VBus mode with the use of an external cache controller, such as the STP1091 Multi-Cache Controller. The STP1091 external cache controller supports multiprocessor configurations using either MBus or XBus™ interfaces with up to 2 MBytes of secondary cache. All references to STP1091 in this document also apply to STP1090A.

Figure 1 shows an STP1021A-based system using the STP1091 Multi-Cache Controller

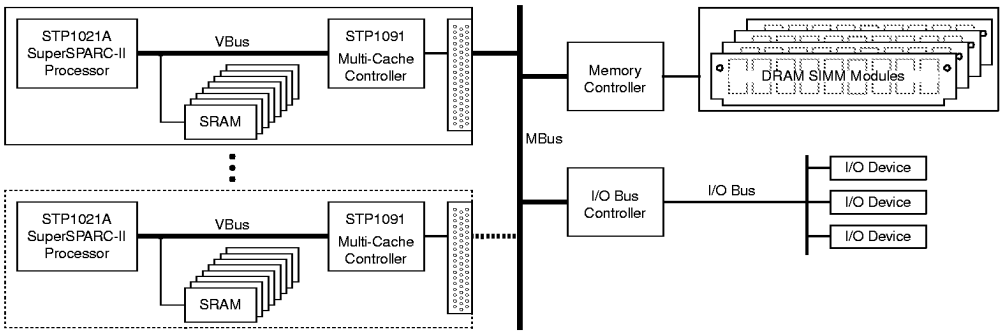


Figure 1. Typical STP1021A Uniprocessor / Multiprocessor System with External Cache Controller

TECHNICAL OVERVIEW

Figure 2 shows an overview of the STP1021A processor microarchitecture. The SuperScalar Integer Execution Unit performs instruction grouping and then decodes/executes arithmetic, shift, branch, and load/store instructions. There are 3 ALUs in the Integer Execution Unit which are dynamically configured as two independent or cascadable ALUs depending on the instruction stream.

The Floating-Point Unit consists of the floating-point register file, double precision adder/multiplier arrays, and the control logic.This unit also performs integer multiply/divide operation. The Memory Management Unit performs virtual to physical address translations. It consists of a 64-entry fully associative data TLB and a 16-entry fully associative instruction TLB, both with hardware table walk for TLB miss processing.

The STP1021A has separate on-chip instruction and data caches that provide fast access to code and data. The 20 KByte instruction cache is a 5-way set-associative and allows fetching 4 instructions on every access using a 128 bit wide bus. The data cache is 16 KBytes and is 4-way set-associative. Both caches are physical caches.

The STP1021A also integrates BIST (Built-In-Self-Test) logic, JTAG interface, and has features that support system and software debugging including hardware break-points.

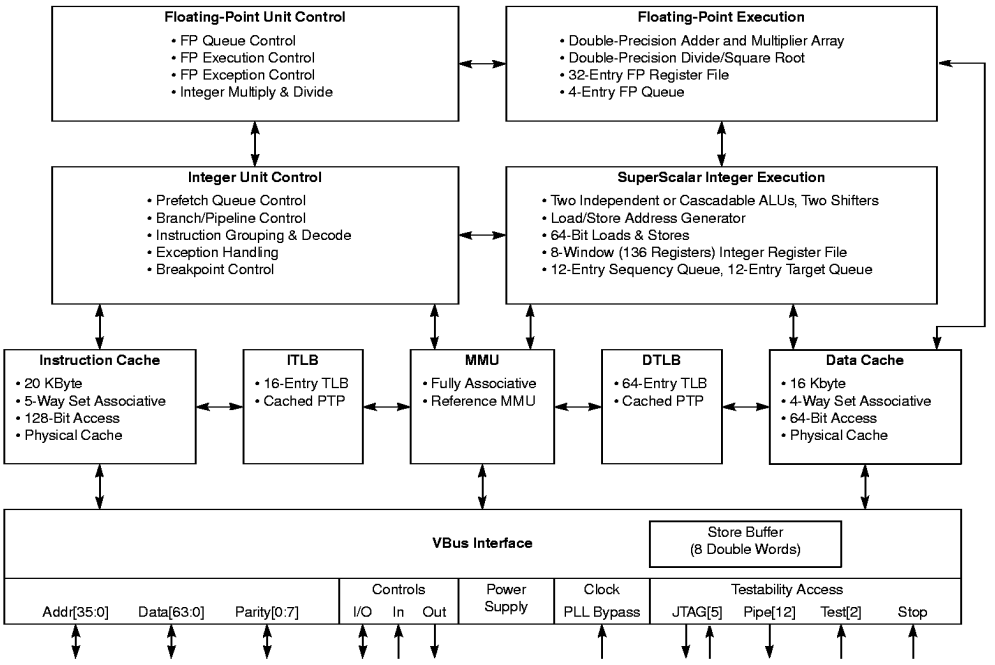


Figure 2. STP1021A SuperSPARC-II Functional Block Diagram

VBus is a non-multiplexed synchronous bus. It is especially tailored to provide an efficient connection between the STP1021A, the STP1091 external cache controller, and the external cache memories made up of synchronous SRAMs. It has a 36-bit address bus, and a 64-bit data bus. All transactions on the VBus are synchronized with the STP1021A clock. The arbiter for the VBus transactions is integrated on the STP1091 chip. The STP1091 supports up to 2 MBytes of external cache and multiprocessing.

In the VBus mode, the STP1021A provides an $\overline{\text{ADDR20}}$ signal besides the ADDR20 signal, just like with STP1020A and STP1021. The STP1020N and STP1020 do not drive this signal. The $\overline{\text{ADDR20}}$ is useful in systems that incorporate 2 MB of external cache (in XBus mode only), and its integration onto the CPU eliminates an external inverter.

MBus is a SPARC International standard bus designed to function as a processor-independent bus between one or more processors and memory. It is a 64-bit multiplexed high-performance bus. It is fully synchronous with all the transfers controlled by an MBus clock. It supports block transfers in sizes up to 128 bytes with a peak transfer rate of 320 MBytes/s. All transactions on the MBus are arbitrated by an external arbiter. The arbitration algorithm is not included in the MBus definition to allow flexibility in system design. MBus is defined for uniprocessor and multiprocessor systems. The uniprocessor form of MBus is termed “Level1”, and the multiprocessor version is called “Level2”. The arbiter for the MBus transactions is integrated on the STP1091 chip. The STP1091 supports up to 1 MByte of external cache and multiprocessing in MBus mode.

SIGNAL DESCRIPTIONS

Signal	Type	Description
ADDR[35:0]	I/O	Physical address bus.
$\overline{\text{ADDR20}}$	O	Inverted physical address ADDR20. Eliminates an external inverter for 2MB cache systems.
BURST	O	This signal is used to indicate that the current address on the bus is part of a burst bus cycle. H = Part of multi-cycle burst. L = Not part of multi-cycle burst.
$\overline{\text{CCHBL}}$	O	This signal indicates that the current transaction is internally cacheable. H = Non-cacheable transaction. L = Cacheable transaction.
$\overline{\text{CMDS}}$	I/O	Command strobe. Indicates the beginning of a bus cycle. When the STP1021A is not in bus master mode, as indicated by $\overline{\text{WGRT}}$ and $\overline{\text{RGRT}}$ being asserted, $\overline{\text{CMDS}}$ is used as an input to initiate external snoop transaction (including invalidates and demaps). H = Not a command word. L = VBus command word on ADDR[35:00], $\overline{\text{CCHBL}}$, $\overline{\text{CSA}}$, $\overline{\text{DEMAP}}$, $\overline{\text{LDST}}$, SIZE[1:0], $\overline{\text{SU}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$. When the STP1021A is a bus master, it asserts this signal for the first cycle of VBus transactions. H = Not a command word. L = VBus command word on ADDR[35:00], $\overline{\text{CCHBL}}$, $\overline{\text{CSA}}$, $\overline{\text{DEMAP}}$, $\overline{\text{LDST}}$, SIZE[1:0], $\overline{\text{SU}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.
$\overline{\text{CSA}}$	O	This signal indicates that the current bus transaction is a control space access. It is asserted for the address space identifier (ASI) transactions to ASI space 0x02. H = Normal memory of ASI access. L = Control space access (to ASI 0x02).
DATA[63:00]	I/O	Data bus.
$\overline{\text{DEMAP}}$	I/O	Asserted with $\overline{\text{CMDS}}$ to indicate demap cycle. As an input indicates an external demap cycle. When output: H = Normal command word. L = demap cycle system (system should remove TLB entries matching request). When input: H = Non-demap cycle. L = Demap cycle from system. The TLB entries matching request will be removed.
DPAR[0:7] [1]	I/O	Data bus parity. When parity is enabled (by setting the parity bits in the MCNTL register), even parity is generated and checked. When parity is disabled, odd parity is generated but parity is not checked. DPAR0 is parity for bits DATA63-DATA56, etc., as listed: DPAR0: DATA[63:56] DPAR1: DATA[55:48] DPAR2: DATA[47:40] DPAR3: DATA[39:32] DPAR4: DATA[31:24] DPAR5: DATA[23:16] DPAR6: DATA[15:08] DPAR7: DATA[07:00]

SIGNAL DESCRIPTIONS (CONTINUED)

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>$\overline{\text{ERROR}}$</td><td>O</td><td>This signal indicates that the STP1021A has entered an error mode state and will take a watchdog reset trap.
H = Normal operation.
L = Error mode.</td></tr>
<tr><td>IRL[3:0]</td><td>I</td><td>Interrupt request level. This field specifies the level of the highest priority interrupt request that is currently pending. If IRL3-IRL0 = 0000, no interrupts are pending.
Level 15 (IRL[3:0] = 1111) is a NMI (disable all traps)
Level 14 Highest maskable interrupt
Level 1 Lowest maskable interrupt
Level 0 No interrupts pending</td></tr>
<tr><td>$\overline{\text{LDST}}$</td><td>O</td><td>This signal indicates an atomic load/store (LDSTUB, LDSTUBA, SWAP or SWAPA) operation. It is equivalent to the logical OR of $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals.
H = No LDST.
L = Atomic Load/Store (LDST) cycle.</td></tr>
<tr><td>$\overline{\text{MEXC}}$</td><td>I</td><td>This signal is encoded with $\overline{\text{RRDY}}$ or $\overline{\text{WRDY}}$ and with $\overline{\text{RETRY}}$ to indicate the type of acknowledgment.
<table>
<tr><th>$\overline{\text{MEXC}}$</th><th>$\overline{\text{RRDY}}$/$\overline{\text{WRDY}}$</th><th>$\overline{\text{RETRY}}$</th><th>Description</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No Reply</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Retry</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Data Transfer Complete</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Undefined Error (UD)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Bus Error (BE)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Timeout Error (TO)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{OE}}$</td><td>I/O</td><td>As an output, this signal controls the pipelined output enable of external cache SRAM. It is used as an input to prevent bus collisions.
H = SRAM outputs disables.
L = SRAM outputs enabled.</td></tr>
<tr><td>$\overline{\text{PEND}}$</td><td>I</td><td>This signal indicates that at least one outstanding write operation has not completed.
H = System has no incomplete write operations outstanding from this processor.
L = System has write operations that were issued by this processor that are not yet complete.</td></tr>
<tr><td>PIPESEL[1:0]</td><td>I</td><td>Select 1 of 4 PIPE combinations.
00 = Performance Group
01 = Bus Group
10 = Test Debug Group
11 = Miscellaneous Group</td></tr>
<tr><td>PIPE[11:0]</td><td>O</td><td>Monitor internal states of STP1021A processor. See tables 2 through 5 for PIPE pin description</td></tr>
<tr><td>PLLBYP [1]</td><td>I</td><td>This pin is used to bypass the internal phase lock loop. When this pin is asserted, the external clock input will be routed directly to internal clock distribution with no delay compensation.
H = PLL enabled. Normal operation.
L = PLL disabled. No clock delay compensation.</td></tr>
<tr><td>PMC[4:0]</td><td>I/O</td><td>Process Monitor Controls. These pins are used for factory test. N.C. in system applications.</td></tr>
</table>

SIGNAL DESCRIPTIONS (CONTINUED)

Signal	Type	Description
RD	I/O	STP1021A drives RD to qualify addresses on the VBus as READ cycles. It is also asserted with WR for swap cycles and with DEMAP for demap cycles. An an input, used for internal SRAM test only. H = Not a read cycle. L = Read (or load/store with WR and LDST low) cycle.
RESET	I	Reset. This causes an external reset for the STP1021A. At power-on, RESET must be held low for at least 100 ms to all allow the PLL to stabilize. If the PLL is known to be stable, RESET may be asserted for as short as 8 cycles. See reset operation. H = Normal operation. L = The STP1021A is externally reset.
RETRY	I	This signal is encoded along with RRDY or WRDY and with MEXC to indicate the type of acknowledgment. See MEXC table for description.
RGRT	I	This signal indicates that the STP1021A has been given a grant to use the VBus for read operations. H = VBus not available for read operations. L = VBus available for read operations.
RRDY	I	This signal indicates that incoming read data is valid. RRDY may be connected to WRDY when only a single ready signal is required. This signal is encoded with MEXC and RETRY. See MEXC table for description.
SIZE1 SIZE0	O	These bits indicate the transfer size of the current transaction. 00 = Byte 01 = Half word 10 = Word 11 = Doubleword
SPARE5 SPARE4 SPARE3 SPARE2 SPARE0	I	Not used. Should be tied high or left floating during normal chip operations.
SRMTST [1]	I	Reserved: Factory test pin. It must be connected to V_{CC} for normal operation.
STOP	I	Stop Mode for chip debug only. H = Stop internal clock. L = Normal operation.
SU	O	This signal indicates that the current bus transaction is a supervisor transaction. H = User (unprivileged) transaction. L = Supervisor (privileged) transaction.
TCK [1]	I	JTAG test clock input.
TDI [1]	I	JTAG test data input.
TDIODE1 TDIODE0		Connected to a thermal diode which can be used for junction temperature measurements
TDO	O	JTAG test data output.
TEST [1]	I	This pin can be used for board level testing. H = Normal operation. L = All outputs except ESB and TDO are placed in a high-impedance state.

SIGNAL DESCRIPTIONS (CONTINUED)

Signal	Type	Description
TMS [1]	I	JTAG test mode select input.
TRST [1]	I	JTAG reset input.
VCLK	I	Primary clock source.
VPLLRC	I	Phase locked loop filter capacitor. This pin should be connected to an external 0.1µF capacitor to ground.
WE[0:7]	O	These signals directly control the write enable signals of synchronous SRAM used for external cache. These signals are driven only when asserted; otherwise, they are tri-state. WE bit ordering corresponds to the big-endian convention (i.e. WE0 is the write enable for byte 0) (DATA63-DATA56). H = SRAM read. L = SRAM write.
WEE	I	This pin is used to control the assertion of WE7-WE0 signals. H = May not drive WE7-WE0. L = May drive WE7-WE0.
WR	I/O	STP1021A drives WR to qualify addresses on the bus as write cycle. It is asserted with RD for swaps as well as demap cycles. An an input, this signal is used to qualify invalidation requests. H = Not a write cycle. L = Write (or load/store with RD and LDST low) cycle.
WRDY	I	This signal indicates that incoming read data is valid. WRDY may be connected to RRDY when only a single ready signal is required. The signal is encoded with MEXC and RETRY. See MEXC table for description.
WGRT	I	This signal grants the STP1021A bus access for write operations. WGRT may be connected to RGRT when only a single grant line is required. H = VBus not available for write operations. L = VBus available for write operations.

1. These pins are pulled inactive with weak internal pull-ups.

TABLE 1: PIPESEL[1:0] = 00: Performance Group

PIPE Number	Description
PIPE0	No instruction available
PIPE1	D-Cache load miss
PIPE2	I-Cache TLB busy, DM_WALK
PIPE3	D-Cache TLB busy, DM_WALK
PIPE[5:4]	FPBusy_FREG_FSR_FQ 00 = No FP Event 01 = FP store FREG, FSR, or FQ busy 10 = FP LD FREG or FSR busy 11 = FP IMULDIV, FPX, or unimplemented busy
PIPE6	FQ full and F_Busy
PIPE7	User/Kernel

TABLE 1: PIPESEL[1:0] = 00: Performance Group (Continued)

PIPE Number	Description
PIPE[9:8]	Store buffer state 00 = None 01 = SB full 10 = SB flush 11 = Synchronous store
PIPE10	ASI in progress
PIPE11	Stall I-pipe during exception

TABLE 2: PIPESEL[1:0] = 01: Bus Monitor Group

PIPE Number	Description
PIPE[3:0]	These are 15 mutually exclusive signals encoded in four bits, valid for one cycle after $\overline{\text{CMDS}}$. 0000 = I-cache TLB level 0 0001 = I-cache TLB level 1 0010 = I-cache TLB level 2 0011 = I-cache TLB level 3 0100 = I-cache sequential, non-demand 0101 = I-cache sequential, demand 0110 = I-cache branch, non-demand 0111 = I-cache branch, demand 1000 = D-cache TLB level 0 1001 = D-cache TLB level 1 1010 = D-cache TLB level 2 1011 = D-cache TLB level 3 1100 = D-cache store buffer flush (forced drain or caused by events that require empty SB) 1101 = D-cache store buffer drain (nobody else is using bus) 1110 = D-cache load
PIPE[5:4]	Number of instructions in execute
PIPE6	Issue a fetch to the last instruction in a cache line
PIPE7	Exception has been detected in the group
PIPE8	User/Kernel
PIPE9	D-Unit stalls I-Pipe (waiting on bus access)
PIPE10	F-Unit stalls I-Pipe
PIPE11	Stall I-Pipe during exceptions

TABLE 3: PIPESEL[1:0] = 10: Test Debug Group

PIPE Number	Description
PIPE0	Stall I-Pipe during exceptions
PIPE[2:1]	Number of instructions in E-State
PIPE3	Control transfer instruction taken
PIPE4	Branch_In_Group
PIPE5	D_unit stalls I-Pipe (waiting on bus access)
PIPE[7:6]	Number of instruction candidates in D0 00 = Nothing in dispatch queue 01 = One instruction in dispatch queue 01 = Two instructions in dispatch queue 11 = Three instructions in dispatch queue
PIPE8	FPOP_IN_GROUP
PIPE9	Any LD MEM, LD ASI or ATOMIC REF in Group
PIPE10	Any ST MEM, ST ASI or Atomic REF in Group
PIPE11	F_unit stalls I-Pipe (fqueue full or dependencies or fcc not ready)

TABLE 4: PIPESEL[1:0] = 11: Miscellaneous Group

PIPE Number	Description
PIPE0	ESB strobe
PIPE1	At least one valid instruction fetched
PIPE2	New PC
PIPE3	FPU queue empty
PIPE[5:4]	FPOP DISPATCHED 00 = None dispatched 01 = FADD dispatched 10 = FMUL dispatched 11 = FDS dispatched
PIPE[8:6]	FPOP COMPLETED 000 = None completed & FPIPE not stalled 001 = FADD completed & FPIPE not stalled 010 = FMDS completed & FPIPE not stalled 011 = FEMODE & FPIPE not stalled 100 = SUBN_SRC & FPIPE stalled 101 = SUBN_RST & FPIPE stalled 110 = FDS_IN_FX & FPIPE stalled 111 = FPOP pending or IMULDIV & FPIPE stalled
PIPE[11:9]	FPOP_IN_GRP 000 = No FPOP, FP_LD, or FP_ST 001 = FPOP_ONLY_IN_GRP 010 = FP_LD_ONLY_IN_GRP 011 = FP_ST_ONLY_IN_GRP 100 = LD_B4_FPOP 101 = ST_BEFORE_FPOP 110 = FPOP_BEFORE_LD 111 = FPOP_BEFORE_ST

TIMING CONSIDERATIONS

The VBus read, write and invalidate operations are explained in the following section.

Cache Disabled/Non-Cacheable Single Read

Figure 3 shows a single read with the cache disabled. The external cache controller (STP1091) goes to the system bus to accomplish this operation. It deasserts $\overline{\text{RGRT}}$ to allow the STP1021A to complete pending write operations. When the data is available, the STP1091 negates grant, drives the data, and asserts $\overline{\text{RRDY}}$.

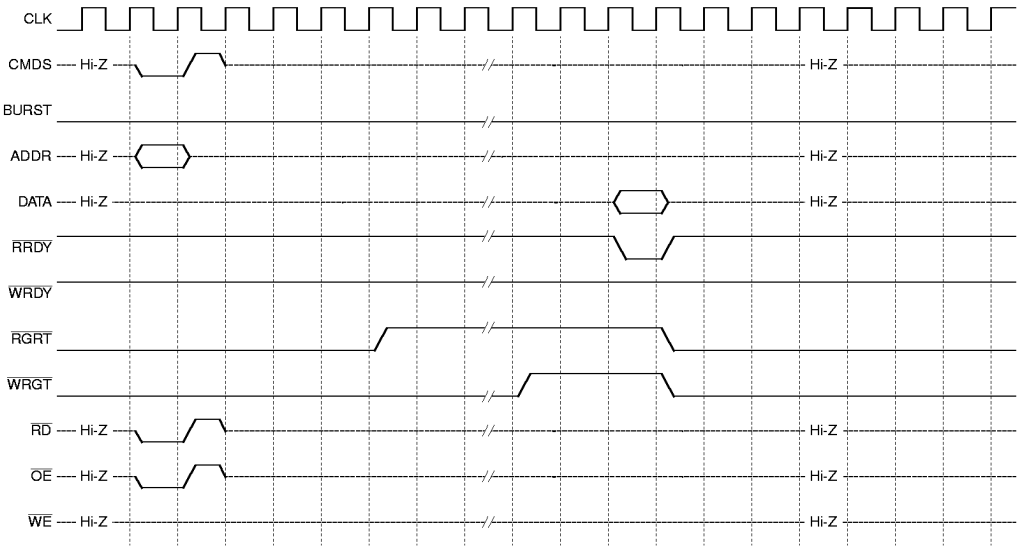


Figure 3. VBus Cache Disabled/Non-Cacheable Single Read

Cache Disabled Write (or Non-Cacheable) Write

Figure 4 shows a cache disabled write. The external cache controller (STP1091) terminates the VBus cycle by issuing a WRDY without asserting WEE. A non-cacheable write would be identical.

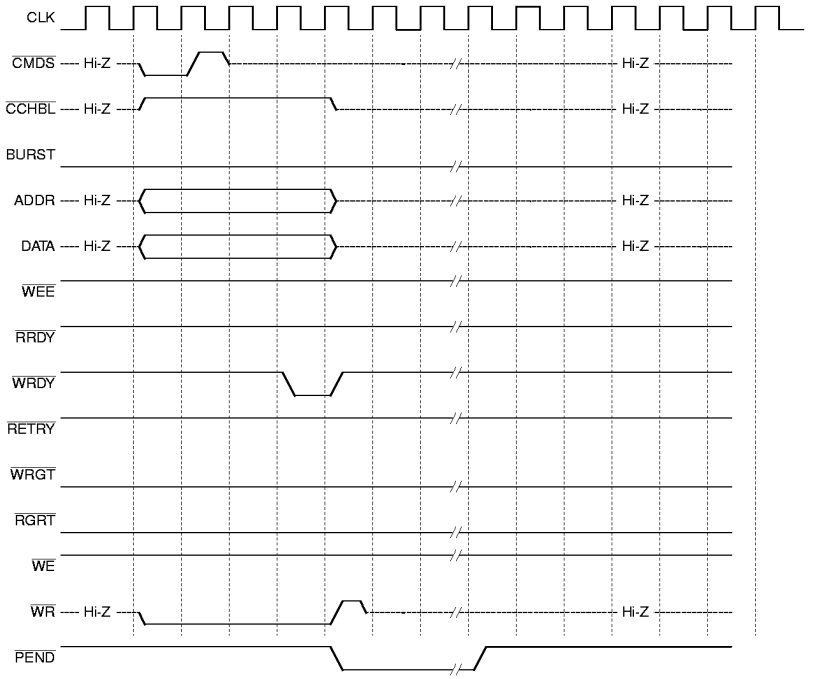


Figure 4. VBus Cache Disabled/Non-Cacheable Single Write

Cacheable Single Read Hit

Figure 5 shows a read by the STP1021A of a single cacheable word with an external cache hit. STP1021A asserts the address, cycle qualifiers, and the $\overline{OE}$ to SRAM. The STP1091 detects a tag match and issues a $\overline{RRDY}$ at the same time that the SRAMs drive data to STP1021A. The $\overline{OE}$ from STP1021A is delayed in the registers internal to the synchronous SRAMs, and the data is enabled two cycles after the $\overline{OE}$ is issued to the chip. Note that the partially bussed (not driven by the STP1021A for the entire cycle) VBus control signals are actively deasserted for 1/2 cycle before being released to the bus keepers.

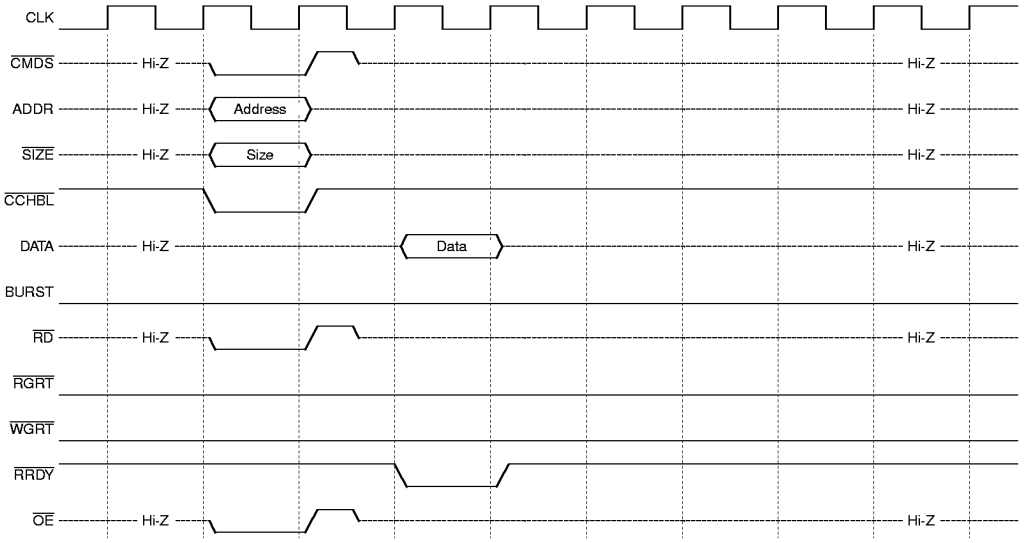


Figure 5. VBus Cacheable Single Read Hit

Cacheable Single Read Miss

Figure 6 shows a cacheable single-read miss. The STP1091 detects that a tag mismatch occurs and issues a cycle to the system bus to obtain data to fill the external cache. It removes $\overline{\text{RGRT}}$ to allow STP1021A to proceed with any write operation it may have had pending. When the system bus returns the requested data block, the STP1091 removes the bus grant to STP1021A (negates $\overline{\text{WGRT}}$) to obtain access to the SRAMs. The STP1091 writes the data into the SRAMs. The STP1091 issues a $\overline{\text{RRDY}}$ to STP1021A, as the data word requested (by STP1021A read) is driven on the DATA lines (while the data is being written into SRAMs).

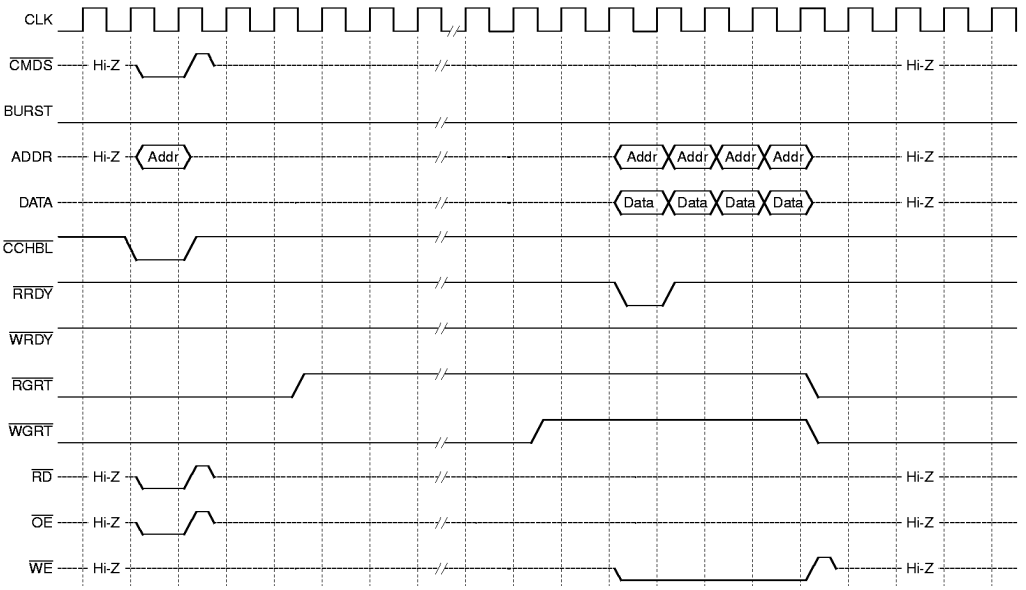


Figure 6. VBus Cacheable Single Read Miss

Burst Read Hit

Figure 7 shows a burst-read hit. As with a cacheable single-read hit, the STP1091 functions mainly to time the cycle by asserting $\overline{\text{RRDY}}$ as the SRAM provides the data.

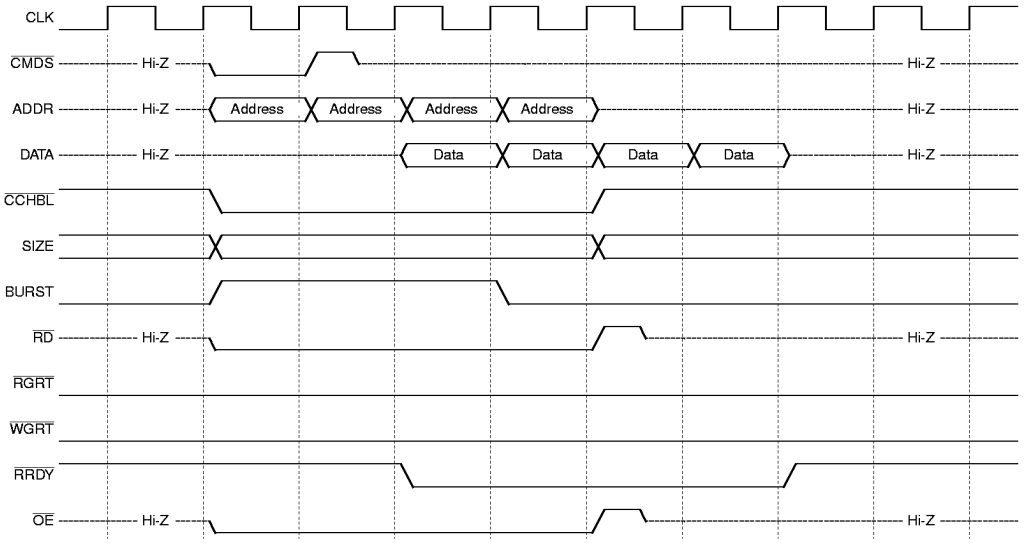


Figure 7. VBus Burst Read Hit

Burst Read Miss

Figure 8 shows a burst read miss. The external cache controller (STP1091) removes $\overline{\text{RRGT}}$ to indicate that the cycle is in progress and that STP1021A can proceed with an outstanding write if one is pending. When the data returns from the system bus, the STP1021A writes it into the SRAM and asserts $\overline{\text{RRDY}}$ when the requested data is on the VBus. Note that, in *Figure 8*, the STP1091 is in XBus configuration, and consequently the block size is 64 bytes. Only 32 bytes are sent to STP1021A, while all 64 bytes are stored in SRAM. Also note that with critical word first ordering, the data returned starts from the index into the block for the requested doubleword, continues to the last index, and then wraps from index 0 to the starting index minus 1.

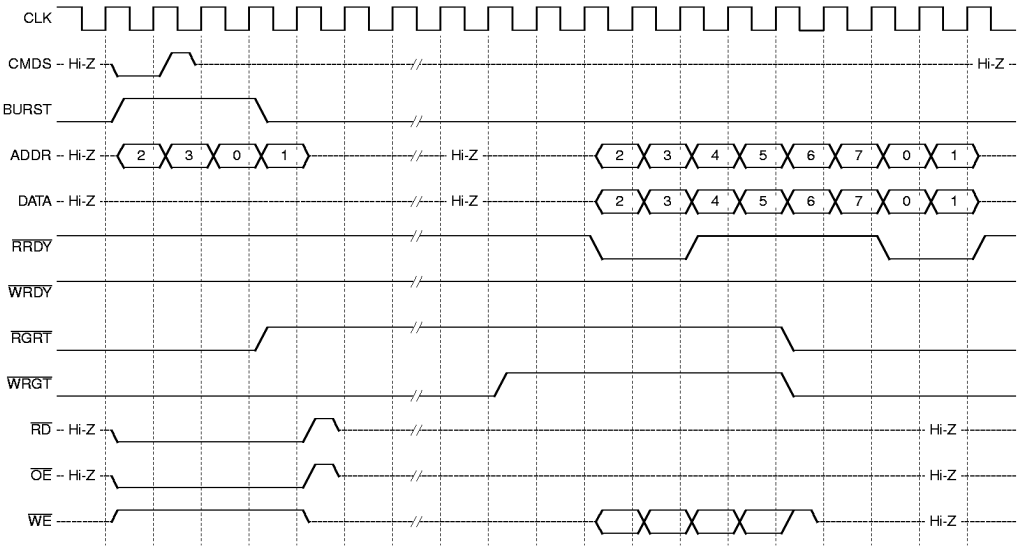


Figure 8. VBus Burst Read Miss

Cacheable Single Write Hit

Figure 9 shows a cacheable single-write hit. The STP1091 asserts $\overline{\text{WEE}}$ at the CMD + 2 cycle (i.e., two cycles after $\overline{\text{CMDS}}$) to allow the assertion of the write data (DATA, DPAR) and the write strobes ($\overline{\text{WE7}}$-$\overline{\text{WE0}}$). The STP1091 asserts the $\overline{\text{WRDY}}$ in the following cycle ($\overline{\text{CMDS}}$ + 3).

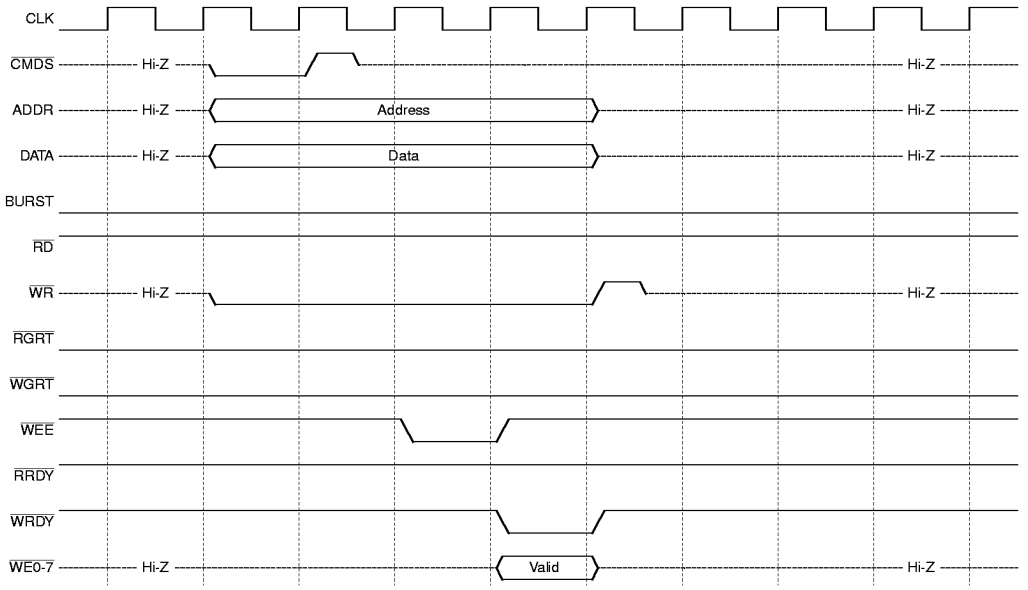


Figure 9. VBus Cacheable Single Write Hit

Cacheable Burst Write Hit

Figure 10 shows a burst write hit. It is basically the same except that $\overline{\text{WRDY}}$ is asserted for each data double-word written in the burst. The STP1021A deasserts BURST one cycle before the last write. Each of the individual writes in the burst from the STP1021A may be from one to eight bytes and may be at any address within the cache block. The number of consecutive writes may be of arbitrary length. If the external cache controller (STP1091) needs the VBus while a burst write cycle is occurring, it can deassert the $\overline{\text{WRGT}}$ signal to terminate the burst cycle prematurely. When the STP1021A reacquires the VBus, it continues the burst write from where it was interrupted.

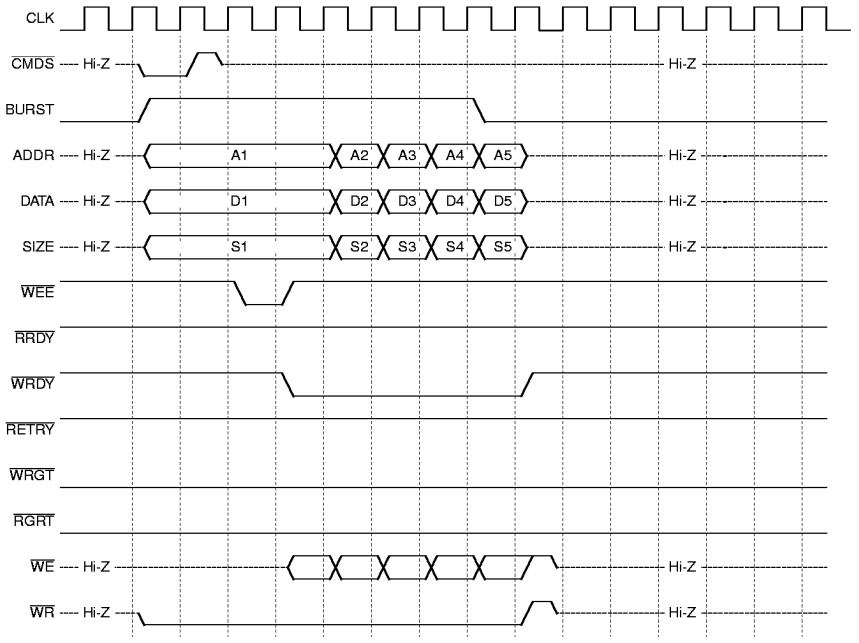


Figure 10. VBus Cacheable Burst Write Hit

Cache Invalidate

Figure 11 shows an invalidate. The external cache controller (STP1091) first removes the STP1021A from the VBus by revoking the $\overline{\text{RGRT}}$ and $\overline{\text{WGRT}}$ bus grants; it then asserts the address, $\overline{\text{WR}}$ and $\overline{\text{CMDS}}$. Multiple invalidates may occur consecutively. Invalidates may also occur when the STP1091 has obtained the VBus for SRAM reads or writes.

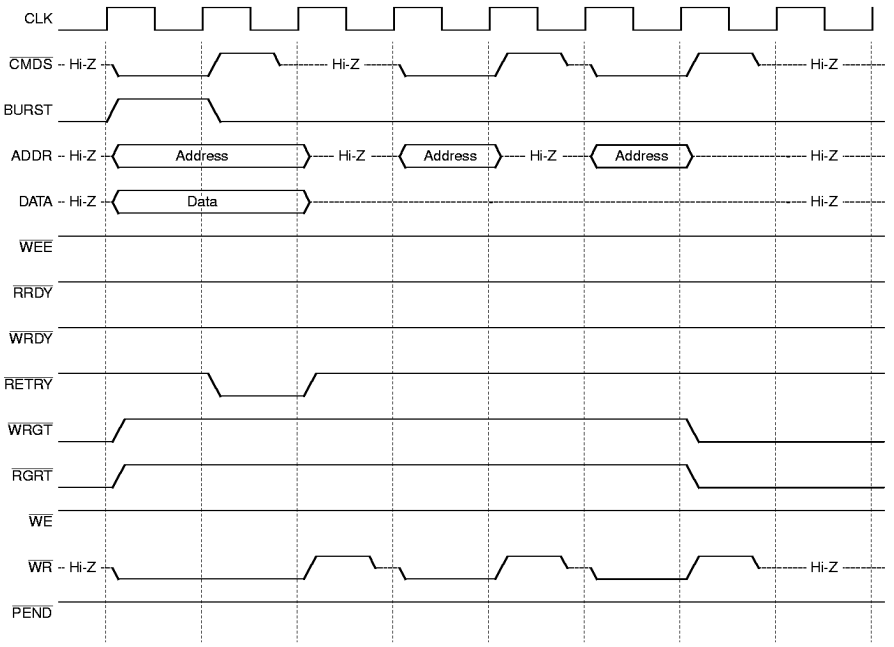


Figure 11. VBus Invalidation

Clock Operation

Proper clocking is essential at high operating frequencies. In order to reduce system clock skew, a phase lock loop (PLL) is implemented on-chip. For testing and other purposes, a PLL bypass mechanism is provided. When the $\overline{\text{PLLBYP}}$ signal is active (low), the PLL circuitry will be completely bypassed.

Phase Lock Loop Operation

The PLL operates by constantly measuring internal clock routing and gate delays and internally generating a clock that is effectively ahead of the external clock by an amount equal to the internal delay. This reduces clock skew to the internal logic. Prior to normal operation, the PLL must be allowed time to stabilize. To assure stabilization, $\overline{\text{RESET}}$ should be active for 100 ms (milliseconds).

The input clock to the STP1021A must never be stopped or changed from its normal periodic operation while the PLL is enabled. Doing so will cause PLL instability and unpredictable operation. To ensure proper operation of the PLL clock, V_{CCCK} and V_{SSCK} should be filtered of system noise. *Figure 12* shows a recommended filter circuit.

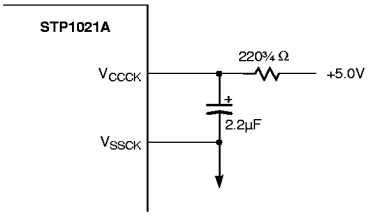


Figure 12. Typical Phase Lock Loop (PLL) Filter Circuit

Important Note: It is essential that the JTAG TAP controller be reset prior to or at the same time as $\overline{\text{RESET}}$ in order for the PLL to begin initialization. The TAP controller may be initialized either by asserting the $\overline{\text{TRST}}$ pin, or by asserting the TMS pin for five consecutive cycles of TCK (test clock). If this reset does not occur, the PLL clock feedback loop may not be established, and unpredictable operation may result. Whenever the JTAG interface is not in use by a particular system, asserting the $\overline{\text{TRST}}$ signal statically is strongly recommended.

Input Clock Requirements

The STP1021A can tolerate most clean stable clock sources when the PLL is enabled. With the PLL enabled, the STP1021A uses only the rising edge of the incoming clock. Internally, the STP1021A multiplies, then divides the clock to provide a stable 50% duty cycle clock. Input duty cycle must be at least 25% (either high or low). When the PLL is bypassed, care must be taken to provide a 50% duty cycle clock. Pin timings for operation with PLL bypassed are not fully defined.

Note: *Operation in a system with the PLL bypassed is not recommended or fully specified.*

Reset Operation

The STP1021A is reset from one of three sources: hardware reset, BIST reset, and watchdog reset. Reset from any source enables boot mode in the MMU, takes a reset trap, and starts executing from 0xFF000000.

In order for the STP1021A to properly reset care must be taken in the system implementation. In particular, JTAG operation may effect the STP1021A's ability to reset. The JTAG test access port (TAP) controller should be in the reset state when hardware reset is asserted.

Hardware Reset

Hardware reset is initiated external to the processor by asserting the $\overline{\text{RESET}}$ signal. Several actions are taken following a hardware reset. The STP1021A spends several hundred cycles initializing internal logic. In particular, during this time the cache column redundancy repair circuits are configured. As soon as $\overline{\text{RESET}}$ is asserted, the STP1021A will tri-state all signals immediately (except for TDO and ESB). All external logic should monitor $\overline{\text{RESET}}$ to ensure the validity of control signals. Appendix B shows what actions are taken by hardware reset.

At power-on, $\overline{\text{RESET}}$ must be held low for at least 100 ms to allow the PLL to stabilize. Once the PLL has stabilized, $\overline{\text{RESET}}$ must be asserted for an additional 16 cycles. If further reset operations are required beyond the initial power-on reset, $\overline{\text{RESET}}$ need only be asserted for a total of eight cycles.

The STP1021A implements internal RAM redundancy to increase component yield. A portion of this redundancy must be initialized each time the component is reset (hardware reset only). This initialization takes approximately 520 cycles, and is internally timed. These cycles begin once the $\overline{\text{RESET}}$ signal is deasserted and before the processor tries to fetch its first instruction. During this time the bus will be inactive, and the STP1021A will tri-state all I/O signals. All bus requests will be inactive, and the STP1021A will execute its first bus cycle approximately 525 cycles after $\overline{\text{RESET}}$ is deasserted.

Immediately after hardware reset and redundancy repair are complete, the STP1021A will execute a reset trap. This trap will cause the processor to enter boot mode (MCNTL.BT is set) and begin execution at virtual address 0xFF000000. This will force a READ-SINGLE bus operation at physical address 0xFF000000. The upper eight bits are set as a result of boot mode. In response to the read single operation, system logic should supply two valid SPARC instructions on the 64-bit data bus. Once these instructions have entered the pipeline, another read single request for the next two instructions will appear on the bus. The physical addresses requested by these reads will be contiguous until a control transfer instruction is executed (normally within two or three instructions).

At power-on reset, the STP1021A will execute in single instruction execution mode. Multiple instruction per cycle execution is enabled by setting the MIX bit in the action register (ASI 0x4C).

BIST Reset

The built-in self test (BIST) logic generates a second type of reset, which is nearly identical to the hardware reset. The BIST operations can be requested either by software (with a STA), or via the JTAG interface. When BIST is complete, an internal reset is automatically generated. A JTAG reset must be generated for the JTAG logic to be reset. This can be done by entering the TAP test logic reset state either by asserting TMS for five consecutive TCK cycles or asserting $\overline{\text{TRST}}$.

Watchdog Reset

In addition to the hardware reset, there is an internally generated reset referred to as a watchdog reset. This reset is caused by entry into error mode (trapping with ET bit of PSR set to 0).

To allow recovery from many error mode conditions, the only MMU control bit affected by a watchdog reset is the boot mode (BT) bit of the MCNTL register. The error mode (EM) bit of the MFSR is set to indicate that this is a watchdog reset, as opposed to a hardware reset. Breakpoints are cleared at watchdog reset.

When using the VBus interface, the STP1021A issues an error mode bus cycle, causing the cache controller (or external system logic) to record the occurrence of error mode. The completion of this bus cycle causes watchdog reset. Once the above actions have been completed, a reset trap will be generated.

The table in Appendix B gives the state of the internal registers after a hardware, BIST, or a Watchdog reset.

DEBUG SUPPORT

Built-in Self Test (BIST)

The STP1021A has Built-In Self Test (BIST) logic on-chip. BIST is a quick check for device integrity and not an exhaustive proof of the device function. Many types of device faults will be detected by an incorrect signature value after a BIST. There are two types of BIST: normal BIST and debug BIST. The normal BIST operation is a more exhaustive check of the logic than the debug BIST. To initiate BIST an STA instruction to ASI 0x39 is issued. Stores to virtual addresses 0x0, and 0x100 select normal BIST and debug BIST respectively. Once initiated, the internal logic controls the BIST operation. An external reset aborts the BIST operation. When the sequence completes, an internal reset is generated [1]. Then the BIST status and the signature can be read with loads from virtual addresses 0x100, and 0x0 with ASI 0x39.

External Monitors (Pipepins)

The STP1021A also provides several device pins to monitor processor operation, and control processor signals. These pins are the PIPE11-0 pins, and the $\overline{\text{TEST}}$ pin. With PIPESEL[1:0]=11, PIPE0 is the External Strobe (ESB) pin, which allows an external device to be triggered when an internal breakpoint is detected. This pin operates under software control to provide a programmable external synchronization pulse. It may be triggered by code, data, or cycle count breakpoint detection. The PIPE11-0 pins are provided to monitor the internal state of the processor and can be used to aid in system hardware and software debug. The $\overline{\text{TEST}}$ pin, when asserted, will tri-state the outputs of all the output buffers, except the TDO and ESB. This allows external test equipment to control the device's signals. Processor state is not assured after assertion of $\overline{\text{TEST}}$.

JTAG (with Enhancement)

The STP1021A provides five-signals for supporting the IEEE 1149.1 standard JTAG serial scan interface. This interface is used for manufacturing fault coverage testing, periphery and interconnect testing, Built-In Self Test (BIST), and remote debugging environment.

JTAG is implemented on STP1021A in full compliance with the IEEE1149.1 standard. All mandatory public instructions for the TAP controller are supported. In addition, a number of private instructions are also implemented for various functions.

1. After BIST completes, the STP1021A generates an internal reset. This internal reset behaves similar to the hardware reset. One of the consequences of this reset is that MCNTL gets initialized; in particular, the parity enable bit of the MCNTL register gets reset so that the STP1021A starts generating odd parity on the pins. This internally generated reset is not seen by a cache controller such as the STP1091.

Boundary Scan

Boundary scan is used in testing printed circuit boards and the chips mounted on those boards. It is crucial in testing the SuperSPARC II-MXCC module. For STP1021A, boundary scan is also used in the enhanced boundary scan mode for testing the STP1021A chip at-speed on low-cost test stations.

Boundary scan cells in full compliance with the IEEE 1149.1 standard are used in all functional I/O pads. All boundary scan cells are connected into a shift register chain. All boundary scan operations are controlled through JTAG.

Self Monitoring Features

STP1021A provides performance monitoring capabilities. It provides the ability to count user or supervisor instructions/cycles, using two 32 bits counters. Breakpoints and counters are setup through ASI instructions.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating	Units
V_{CC}	Supply voltage range	0 to 5.5	V
V_I	Input voltage range	-0.5 to V_{CC} + 0.5	V
V_O	Output voltage range	-0.5 to V_{CC} + 0.5	V
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{CC})	±50	mA
	Current into any output in the low state	96	mA
T_{STG}	Storage temperature	-65 to 150	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC} [1]	Supply voltage		4.95	5.0	5.05	V
V_{SS} [2]	Ground		–	0	–	V
V_{IH}	Input high voltage [3]	All except CLK/VCLK	2.0	–	V_{CC} + 0.3	V
		CLK/VCLK	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input low voltage [3]		-0.3	–	0.8	V
I_{OH}	Output high current		–	–	-500.0	uA
I_{OL}	Output low current		–	–	500	uA
T_C	Operating case temperature		–	–	85	°C
T_A	Operating ambient temperature		0	–	[4]	°C

1. V_{CC} includes V_{CCC}, V_{CCCK}, V_{CCI}, V_{CCP}.
2. V_{SS} includes V_{SSC}, V_{SSCK}, V_{SSI}, V_{SSP}.
3. V_{IH} (max) and V_{IL} (min) are characterized but not tested during manufacturing test.
4. Maximum ambient temperature is limited by air flow such that the maximum case temperature does not exceed T_C.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	I_{OH} = Max, V_{CC} = Min	2.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = Max, V_{CC} = Max	–	–	0.4	V
I_{CC}	Supply current	V_{CC} = Max, f=75 MHz $t_{w(VCLK)}$ or $t_{W(CLK)}$ = Min	–	2.9	3.2	A
		V_{CC} = Max, f=85 MHz $t_{w(VCLK)}$ or $t_{W(CLK)}$ = Min	-	3.3	3.7	
I_{CCQ}	Quiescent power supply current	V_{CC} = Max, V_I = V_{SS} or V_{CC}	–	425	–	mA
I_{OZ}	High-impedance output current	V_{CC} = Max, V_O = VCC [1]	–	–	20	uA
		V_{CC} = Max, V_O = VSS [2]	–	–	-20	uA
I_I	Input current	V_I = V_{SS} to V_{CC}, Inputs with pullups	–	–	250	uA
		V_I = V_{SS} to V_{CC}, All other inputs	–	–	50	uA
W_D	Power dissipation	V_{CC} = max, f = 75 MHz	–	14.5	17.0	W
		V_{CC} = max, f = 85 MHz	-	16.5	19.0	W
C_I	Input capacitance [3]		–	5	–	pF
C_O	Output capacitance [4]		–	10	–	pF

1. Measured at VCC
2. Measured at VSS
3. This specification is provided as an aid to board design. This specification is not assured during manufacturing testing.
4. This specification is provided as an aid to board design. This specification is not assured during manufacturing testing.

AC Characteristics: VBus Timing - Setup and Hold [1]

Symbol	Parameter	Signals	75 MHz Min	85 MHz Min	Max	Unit
t_{su}(VA)	VBus setup to VCLK	ADDR35-ADDR0, $\overline{\text{ADDR20}}$	4.5	4.0	–	ns
t_{su}(VD)	VBus setup to VCLK	DATA63-DATA0, DPAR0-DPAR7	4.5	4.0	–	ns
t_{su}(VC1)	VBus setup to VCLK	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CMDS}}$, $\overline{\text{DEMAP}}$	4.5	4.0	–	ns
t_{su}(VC2)	VBus setup to VCLK	$\overline{\text{WEE}}$, $\overline{\text{WRDY}}$, $\overline{\text{RRDY}}$, $\overline{\text{WGRT}}$, $\overline{\text{RGRT}}$, $\overline{\text{MEXC}}$, $\overline{\text{RETRY}}$	4.5	4.0	–	ns
t_{su}(IRL)	VBus setup to VCLK	IRL (synchronous) [2]	4.5	4.0	–	ns
t_{su}(OE)	VBus setup to VCLK	$\overline{\text{OE}}$	4.5	4.0	–	ns
t_{su}(PEND)	VBus setup to VCLK	$\overline{\text{PEND}}$ setup to VCLK	4.5	4.0	–	ns
t_h(VA)	VBus hold from VCLK	ADDR35-ADDR0, $\overline{\text{ADDR20}}$	1.0	1.0	–	ns
t_h(VD)	VBus hold from VCLK	DATA63-DATA0, DPAR0-DPAP7	1.0	1.0	–	ns
t_h(VC1)	VBus hold from VCLK	$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CMDS}}$, $\overline{\text{DEMAP}}$	1.0	1.0	–	ns
t_h(VC2)	VBus hold from VCLK	$\overline{\text{WEE}}$, $\overline{\text{WRDY}}$, $\overline{\text{RRDY}}$, $\overline{\text{WGRT}}$, $\overline{\text{RGRT}}$, $\overline{\text{MEXC}}$, $\overline{\text{RETRY}}$	1.0	1.0	–	ns
t_h(IRL)	VBus hold from VCLK	IRL (synchronous) [2]	1.0	1.0	–	ns
t_h(OE)	VBus hold from VCLK	$\overline{\text{OE}}$	1.0	1.0	–	ns
t_h(PEND)	VBus hold from VCLK	$\overline{\text{PEND}}$	1.0	1.0	–	ns

1. VBus Timings are preliminary based on initial characterization, and are subject to change.
2. IRL are asynchronous inputs. Times given are minimum to assure synchronous operation.

Note: All timing numbers include tester guardband approximately 600ps

AC Characteristics: VBus Timing - Switching Characteristics [1] [2]

Symbol	Parameter	Test Conditions	Min	75 MHz Max	85 MHz Max	Unit
t_p(VA)	Propagation delay, VCLK to ADDR35-ADDR0, $\overline{ADDR20}$	I_{OH} = Max I_{OL} = Max C_L = 35pF V_{load} = 2.25V	–	6.5	6.0	ns
t_p(VD)	Propagation delay, VCLK to DATA63-DATA0, DPAR0-DPAR7		–	6.5	6.0	ns
t_p(VC1)	Propagation delay, VCLK to $\overline{RD}$, $\overline{WR}$, $\overline{CMDS}$, $\overline{DEMAP}$		–	6.5	6.0	ns
t_p(VC3)	Propagation delay, VCLK to BURST, $\overline{CCHBL}$, $\overline{CSA}$, $\overline{LDST}$, $\overline{SU}$		–	6.5	6.0	ns
t_p(SIZE)	Propagation delay, VCLK to SIZE1-SIZE0		–	6.5	6.0	ns
t_p(OE)	Propagation delay, VCLK to $\overline{OE}$		–	6.5	6.0	ns
t_p(WE)	Propagation delay, VCLK to $\overline{WE7}$-$\overline{WE0}$		–	6.5	6.0	ns
t_p(ERR)	Propagation delay, VCLK to $\overline{ERROR}$		–	6.5	6.0	ns
t_{oh}(VA)	Output hold time, VCLK to ADDR35-ADDR0, $\overline{ADDR20}$		1.5	–	–	ns
t_{oh}(VD)	Output hold time, VCLK to DATA63-DATA0, DPAR0-DPAR7		1.5	–	–	ns
t_{oh}(VC1)	Output hold time, VCLK to $\overline{RD}$, $\overline{WR}$, $\overline{CMDS}$		1.5	–	–	ns
t_{oh}(DEMAP)	Output hold time, VCLK to $\overline{DEMAP}$		1.5	–	–	ns
t_{oh}(VC3)	Output hold time, VCLK to BURST, $\overline{CCHBL}$, $\overline{CSA}$, $\overline{LDST}$, $\overline{SU}$		15	–	–	ns
t_{oh}(SIZE)	Output hold time, VCLK to SIZE1-SIZE0		1.5	–	–	ns
t_{oh}(OE)	Output hold time, VCLK to $\overline{OE}$		1.5	–	–	ns
t_{oh}(WE)	Output hold time, VCLK to $\overline{WE7}$-$\overline{WE0}$		1.5	–	–	ns
t_{oh}(ERR)	Output hold time, VCLK to $\overline{ERROR}$		1.5	–	–	ns

1. Switching characteristics are given with maximum number of outputs simultaneously switching.
2. VBus Timings are preliminary based on initial characterization, and are subject to change.

Note: All timing numbers include tester guardband approximately 600ps

Clock Timing [1]

Symbol	Parameter	75/85 MHz			Unit
		Min	Typ	Max	
t_w(VCLK)	VCLK pulse duration [2] at 75 MHz	13.3	–	13.4	ns
	VCLK pulse duration [3] at 85 MHz	11.7	-	13.4	ns
	VCLK duty cycle	25	50	75	%
t_w(TCK)	TCK pulse duration	100	–	–	ns
	TCK duty cycle	–	50	–	%

1. This is for the PLL enabled. If the PLL is disabled, the part supports a fully static design. The timing parameters are not assured, since this is not tested.
2. 75 MHz - Switching characteristics are given with maximum number of outputs simultaneously switching.
3. 85 MHz - Switching characteristics are given with maximum number of outputs simultaneously switching.

JTAG and Miscellaneous Timing - Setup and Hold

Symbol	Parameter	Signal	75/85 MHz		Unit
			Min	Max	
t_{su}(RESET)	Setup to VCLK	RESET (synchronous) [1]	10	–	ns
t_{su}(TDI)	JTAG setup to TCK	TDI	10	–	ns
t_{su}(TMS)	JTAG setup to TCK	TMS	10	–	ns
t_h(RESET)	Hold from VCLK	RESET (synchronous) [1]	6	–	ns
t_h(TDI)	JTAG hold from TCK	TDI	20	–	ns
t_h(TMS)	JTAG hold from TCK	TMS	20	–	ns

1. RESET can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.

JTAG and Miscellaneous Timing - Switching Characteristics [1]

Symbol	Parameter	Condition	75/85 MHz		Unit
			Min	Max	
t_p(TDO)	TCK (falling edge) to TDO	I_{OL} = Max I_{OH} = Max V_{LOAD} = 2.25V C_L = 35 pF	–	25	ns
t_{oh}(TDO)	TCK (falling edge) to TDO		5	–	ns
t_p(PIPE)	VCLK to PIPE9-PIPE0		–	14.5	ns
t_p(ESB)	VCLK to ESB		–	14.5	ns
t_{oh}(PIPE)	VCLK to PIPE9-PIPE0		0.5	–	ns
t_{oh}(ESB)	VCLK to ESB		0.5	–	ns

1. Switching characteristics are given with maximum number of outputs switching simultaneously.

PARAMETER MEASUREMENT

Load Circuit Parameters

Timing Parameters		C_{LOAD} [1] (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	35	0.5	-0.5	2.25
	t_{PZL}				
t_{dis}	t_{PHZ}	35	0.5	-0.5	2.25
	t_{PLZ}				
t_{PD}		35	0.5	-0.5	2.25

1. C_{LOAD} includes probes and test fixture capacitance.

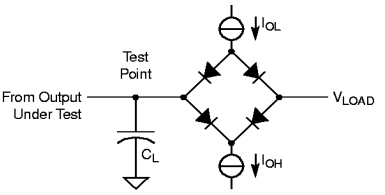
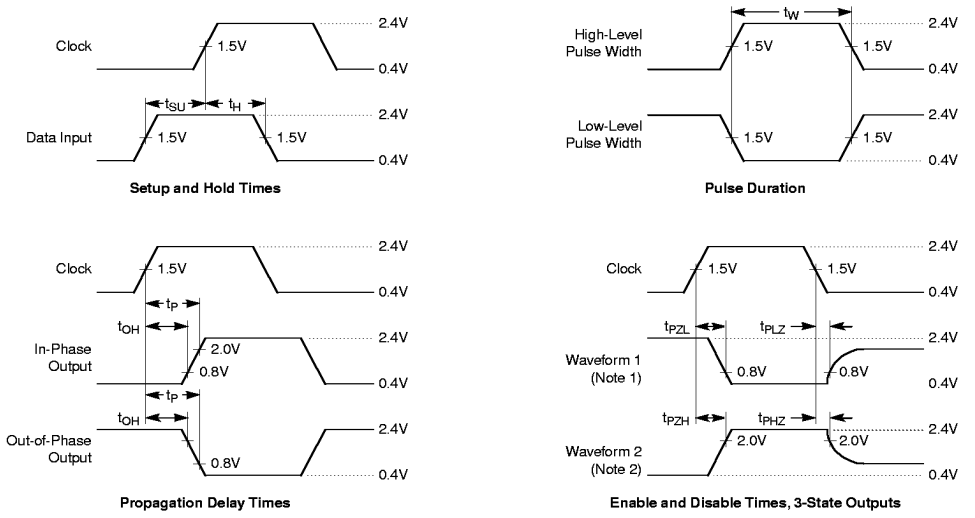


Figure 13. Load Circuit and Parameters



1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are specified values.

Figure 14. Voltage Waveforms

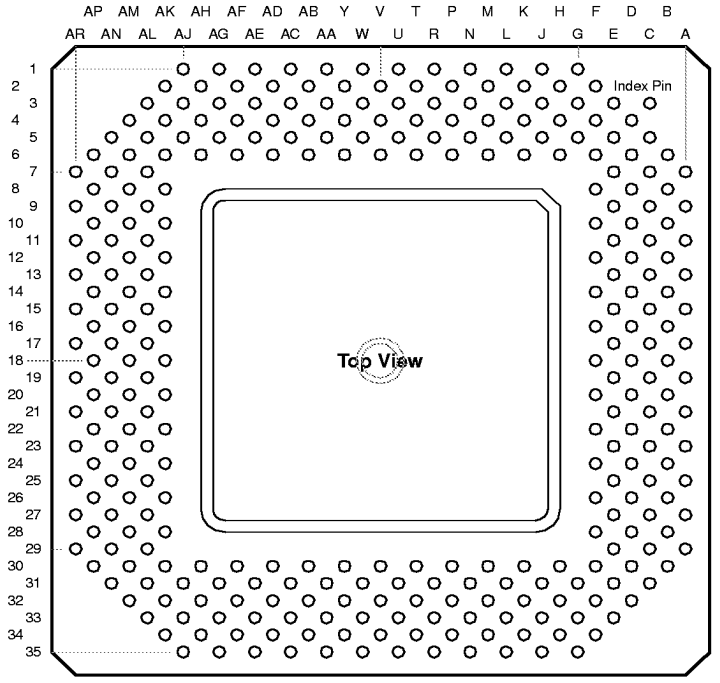
PIN ASSIGNMENTS

313-Pin Ceramic PGA Package Pin Assignment

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A7	n/c	D22	DATA37	H32	DATA49	T34	DATA62	AE1	VSSP	AL7	VSSP	AP18	VCCC
A9	DATA20	D24	DATA41	H34	DATA51	U1	PLLBYP	AE3	VCCI	AL9	VCCP	AP20	RETRY
A11	VSSP	D26	DPAR2	J1	DATA10	U3	VSSC	AE5	VSSC	AL11	VSSC	AP22	WR
A13	DATA25	D28	DATA47	J3	VSSP	U5	VSSP	AE31	VSSC	AL13	VSSC	AP24	SIZE0
A15	VSSI	D30	TDIODE1	J5	VCCP	U31	VSSP	AE33	VCCP	AL15	VCCC	AP26	SIZE1
A17	DATA31	D32	VCCI	J31	VCCC	U33	VSSC	AE35	VSSP	AL17	VSSC	AP28	spare5
A19	DATA33	E3	IRL1	J33	VSSP	U35	DATA63	AF2	ADDR0	AL19	VSSC	AP30	ADDR20B
A21	VCCI	E5	VSSI	J35	DATA52	V2	VSSP	AF4	ADDR1	AL21	VCCC	AR7	ADDR17
A23	DATA38	E7	VSSC	K2	DATA9	V4	VCCP	AF6	ADDR3	AL23	VSSC	AR9	WE7
A25	VSSP	E9	VCCC	K4	DATA11	V6	VCCCK	AF30	ADDR31	AL25	VSSC	AR11	VSSP
A27	DATA44	E11	VSSC	K6	DATA12	V30	PIPE11	AF32	ADDR34	AL27	VCCC	AR13	WE2
A29	n/c	E13	VSSC	K30	DATA50	V32	VCCC	AF34	PIPE0	AL29	VSSC	AR15	VCCI
B6	DATA16	E15	VCCC	K32	DPAR1	V34	VSSP	AG1	ADDR2	AL31	VSSI	AR17	RRDY
B8	DATA18	E17	VSSC	K34	DATA53	W1	DATA1	AG3	VSSP	AL33	ADDR25	AR19	MEXC
B10	DATA21	E19	VSSC	L1	VSSP	W3	VSSC	AG5	VCCC	AM4	VSSP	AR21	VSSI
B12	DATA24	E21	VCCC	L3	VCCP	W5	VSSC	AG31	VCCC	AM6	ADDR13	AR23	OE
B14	DPAR4	E23	VSSC	L5	VSSC	W31	VSSC	AG33	VSSP	AM8	ADDR16	AR25	VSSP
B16	DATA30	E25	VSSC	L31	VSSC	W33	VSSP	AG35	ADDR33	AM10	WE6	AR27	DEMAP
B18	VCCC	E27	VCCC	L33	VCCP	W35	PIPE10	AH2	ADDR4	AM12	WEE	AR29	PEND
B20	DATA34	E29	VSSC	L35	VSSP	Y2	RESET	AH4	ADDR6	AM14	WE0		
B22	DATA36	E31	VSSI	M2	DATA6	Y4	DATA0	AH6	ADDR7	AM16	RGRT		
B24	DATA40	E33	PMC3	M4	DATA7	Y6	VCK	AH30	ADDR27	AM18	VSSP		
B26	DATA42	F2	DATA15	M6	DATA8	Y30	PIPE7	AH32	ADDR29	AM20	BURST		
B28	DATA46	F4	IRL2	M30	DATA54	Y32	PIPE8	AH34	ADDR32	AM22	spare4		
B30	PIPESEL0	F6	IRL0	M32	DATA55	Y34	PIPE9	AJ1	ADDR5	AM24	CCHBL		
C3	n/c	F8	TEST	M34	DATA56	AA1	VSSI	AJ3	VCCP	AM26	CSA		
C5	spare0	F10	DATA19	N1	DATA5	AA3	VCCC	AJ5	VSSP	AM28	ADDR20		
C7	VCCP	F12	DATA22	N3	VSSP	AA5	VCCC	AJ31	VSSC	AM30	ADDR22		
C9	VSSP	F14	DATA26	N5	VSSC	AA31	VCCC	AJ33	VCCP	AM32	VCCI		
C11	VCCP	F16	DATA28	N31	VSSC	AA33	VCCP	AJ35	ADDR30	AN5	ADDR12		
C13	VSSP	F18	DATA32	N33	VSSP	AA35	VCCI	AK2	ADDR8	AN7	VSSP		
C15	VCCP	F20	DPAR3	N35	DATA57	AB2	ERROR	AK4	ADDR9	AN9	VSSI		
C17	VSSP	F22	DATA39	P2	DPAR7	AB4	STOP	AK6	ADDR11	AN11	VCCP		
C19	VSSP	F24	DATA43	P4	DATA4	AB6	TCK	AK8	ADDR14	AN13	VSSP		
C21	VCCP	F26	DATA45	P6	VSSCK	AB30	PIPE4	AK10	ADDR18	AN15	VCCC		
C23	VSSP	F28	PIPESEL1	P30	DATA58	AB32	PIPE5	AK12	WE5	AN17	VSSC		
C25	VCCP	F30	PMC4	P32	DATA59	AB34	PIPE6	AK14	WE1	AN19	VCCP		
C27	VSSP	F32	PMC2	P34	DPAR0	AC1	TDI	AK16	CMDS	AN21	VSSP		
C29	VCCP	F34	PMC1	R1	VCCI	AC3	VCCP	AK18	WRDY	AN23	VCCP		
C31	TDIODE0	G1	DATA13	R3	VCCP	AC5	VSSC	AK20	RD	AN25	VSSP		
D4	VCCI	G3	VCCP	R5	VCCC	AC31	VSSC	AK22	SU	AN27	VCCP		
D6	SRMTST	G5	VSSC	R31	VCCC	AC33	VSSP	AK24	LDST	AN29	VSSP		
D8	DATA17	G31	VSSC	R33	VCCP	AC35	PIPE3	AK26	ADDR19	AN31	ADDR23		
D10	DPAR5	G33	VCCP	R35	VSSI	AD2	TMS	AK28	ADDR21	AP6	ADDR15		
D12	DATA23	G35	DATA48	T2	DATA3	AD4	TDO	AK30	ADDR24	AP8	spare2		
D14	DATA27	H2	DPAR6	T4	DATA2	AD6	TRST	AK32	ADDR26	AP10	WE4		
D16	DATA29	H4	DATA14	T6	VPLLRC	AD30	ADDR35	AK34	ADDR28	AP12	WE3		
D18	VSSP	H6	IRL3	T30	DATA60	AD32	PIPE1	AL3	ADDR10	AP14	spare3		
D20	DATA35	H30	PMC0	T32	DATA61	AD34	PIPE2	AL5	VCCP	AP16	WGRT		

PIN LAYOUT

313-Pin Ceramic PGA Package

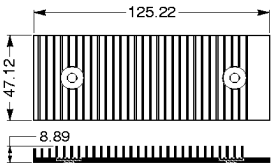


THERMAL CHARACTERISTICS

Thermal Resistance vs. Air Flow [1] [2] [3]

Symbol	Air Flow (ft./min)				
	100	200	300	400	500
Θ_{CA} (°C/W)	4.8	3.5	2.8	2.3	2.0

1. Specified Θ_{CA} values are for straight-fin type heatsink.
2. T_C can be calculated by: $T_C = T_A + P_D \times \Theta_{CA}$.
3. @85 MHz maximum power = 16.5 Watts.

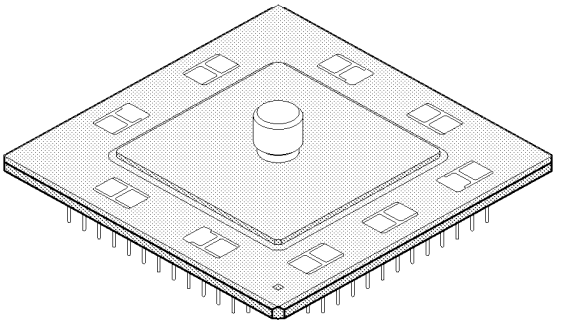


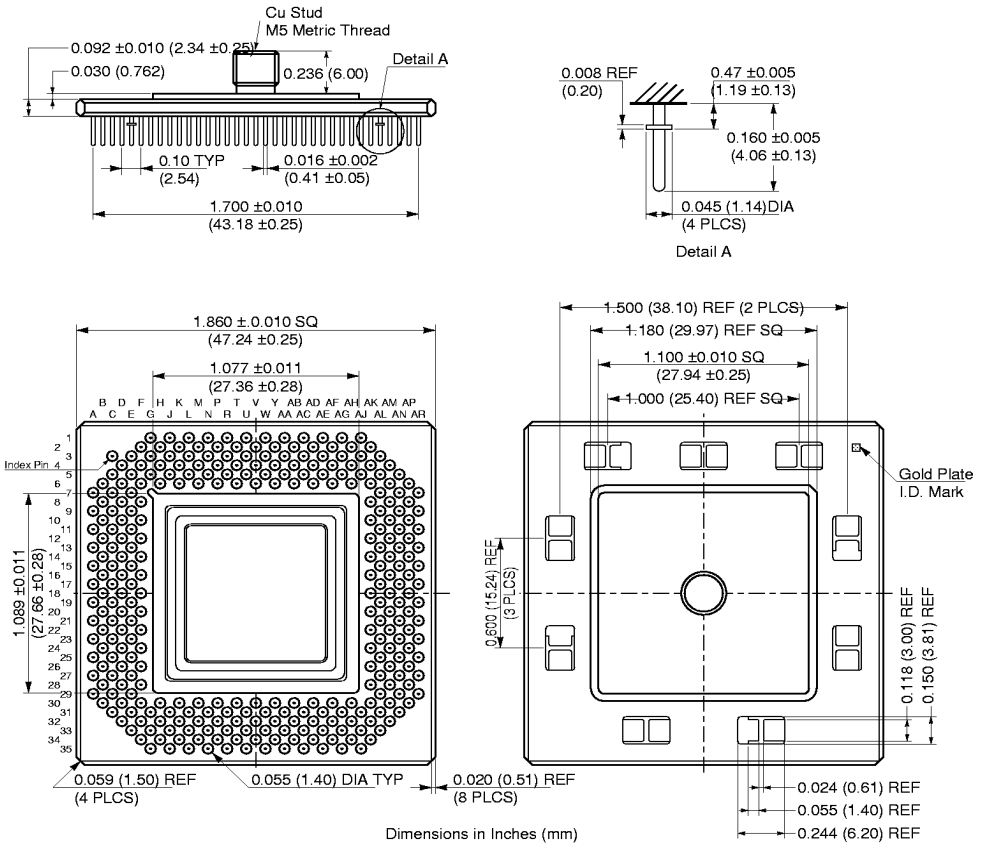
Dimensions in MM.

Heatsink shown for reference only. The STP1021A is not shipped with a heatsink. Contact your SPARC Technology Business sales representative for details.

PACKAGE DIMENSIONS

313-Pin Ceramic PGA Package





APPENDIX A — ADDRESS SPACE IDENTIFIER (ASI) SUPPORT

For each instruction access and each normal data access, the processor appends to the 32-bit memory address an 8-bit address space identifier, or ASI. The ASI encodes whether the processor is in supervisor or user mode, and whether the access is an instruction or data access. Supervisor programs can also make access to program-controlled address spaces by using the privileged Load/Store Alternate instructions. These privileged Load/Store instructions, contain implementation dependent ASI codes that specify the address space to be accessed. These address spaces can be the MMU registers, cache controller registers, processor state registers, and other processor or system-dependent values.The following table provides an assignment list of all the STP1021A ASIs.

TABLE 5: Assignments of STP1021A ASIs

ASI	Function	Access	Size
0x00 to 0x01	Reserved	–	–
0x02	Control space access	LD/ST	All
0x03	Reference MMU flush/probe	LD/ST	Single
0x04	Reference MMU registers	LD/ST	Single
0x05	MMU C-TLB diagnostics	LD/ST	Single
0x06	MMU D-TLB diagnostics	LD/ST	Single
0x07	Reserved	–	–
0x08	User instruction	LD/ST	All
0x09	Supervisor instruction	LD/ST	All
0x0A	User data	LD/ST	All
0x0B	Supervisor data	LD/ST	All
0x0C	Instruction cache tags	LD/ST	Double
0x0D	Instruction cache data	LD/ST	Double
0x0E	Data cache tags	LD/ST	Double
0x0F	Data cache data	LD/ST	Double
0x10 to 0x1F	Reserved	–	–
0x20 to 0x2F	MMU bypass	LD/ST	All
0x30	Store buffer tags	LD/ST	Double
0x31	Store buffer data	LD/ST	Double
0x32	Store buffer control	LD/ST	Single
0x33 to 0x35	Reserved	–	–
0x36	Instruction cache flash clear	ST	Single
0x37	Data cache flash clear	ST	Single
0x38	MMU breakpoint diagnostics	LD/ST	Double
0x3A to 0x3F	Reserved	–	–
0x40	Kernel	LD/ST	Single
0x41 to 0x47	Reserved	–	–
0x48	Performance counter A	LD/ST	Single

TABLE 5: Assignments of STP1021A ASIs (Continued)

ASI	Function	Access	Size
0x49	Performance counter B	LD/ST	Single
0x4A	Counter breakpoint control register	LD/ST	Single
0x4B	Counter breakpoint status register	LD/ST	Single
0x4C	Action register	LD/ST	Single
0x4D to 0xFF	Unassigned	–	–

APPENDIX B — REGISTER STATE AFTER RESET

The following table shows the state of the internal registers after a reset.

TABLE 6: Register State After Reset

Register	State After Rest		
	Hardware	BIST	Watchdog
Floating-Point Queue	Invalidated	Invalidated	Unchanged
Boot Mode (MCNTL.BT)	1 (Boot mode)	1 (Boot mode)	1 (Boot mode)
MMU Enable (MCNTL.EN)	0 (MMU disabled)	0 (MMU disabled)	Unchanged
No Fault (MCNTL.NF)	0 (Faults enabled)	0 (Faults enabled)	Unchanged
Data Cache Enable (MCNTL.DE)	0 (Data Cache disabled)	0 (Data Cache disabled)	Unchanged
Instruction Cache Enable (MCNTL.IE)	0 (Instruction Cache disabled)	0 (Instruction Cache disabled)	Unchanged
Store Buffer enable (MCNTL.SB)	0 (Store Buffer disabled)	0 (Store Buffer disabled)	Unchanged
MBus Mode (MCNTL.MB)	0 (Read Only)	0 (Read Only)	0 (Read Only)
Parity Enable (MCNTL.PE)	0 (Parity disabled)	0 (Parity disabled)	Unchanged
Snoop Enable (MCNTL.SE)	0 (Snooping disabled)	0 (Snooping disabled)	Unchanged
Partial Store Ordering (MCNTL.PSO)	0 (TSO/Strong Ordering)	0 (TSO/Strong Ordering)	Unchanged
Alternate Cacheable (MCNTL.AC)	0 (Noncacheable)	0 (Noncacheable)	Unchanged
Table Walk Cacheable (MCNTL.TC)	0 (Noncacheable)	0 (Noncacheable)	Unchanged
Error Mode (MFSR.EM)	0 (Not an error mode, or watchdog reset)	0 (Not an error mode, or watchdog reset)	1 (A watchdog reset)
TLB Lock Bits	0 (All TLB lock bits cleared)	0 (All TLB lock bits cleared)	0 (All TLB lock bits cleared)
Multiple Instruction Mode (ACTION.MIX)	0 (Single Instruction Execution)	0 (Single Instruction Execution)	0 (Single Instruction Execution)
Breakpoints (MDIAG)	0 (All breakpoints disabled)	0 (All breakpoints disabled)	0 (All breakpoints disabled)
Program Counter	0 (PC=0x0, nPC=0x4)	0 (PC=0x0, nPC=0x4)	0 (PC=0x0, nPC=0x4)
BIST Status	00 (No BIST since reset)	01 or 10 (BIST run since reset)	Not Affected
Store Buffer Tags	Valid bits cleared	Valid bits cleared	Valid bits cleared
Store Buffer Contents	Contents Uninitialized	Contents Uninitialized	Contents Unchanged
Data Cache	Contents Uninitialized	Contents Uninitialized	Contents Unchanged
Instruction Cache	Contents Uninitialized	Contents Uninitialized	Contents Unchanged
Register File	Contents Uninitialized	Contents Uninitialized	Contents Unchanged
Processor Status Register (PSR)	S=1, ET=0, EC=0, Ver=0, Impl=4, PSR current window pointer Uninitialized	S=1, ET=0, EC=0, Ver=0, Impl=4, PSR current window pointer Uninitialized	S=1, ET=0, EC=0, Ver=0, Impl=4, PSR current window pointer Unchanged

TABLE 6: Register State After Reset (Continued)

Register	State After Rest		
	Hardware	BIST	Watchdog
Window Invalid Mask (WIM)	Uninitialized	Uninitialized	Unchanged
Fault Status Register (MFSR)	Uninitialized (except for MFSR error mode bit)	Uninitialized (except for MFSR error mode bit)	Unchanged (except for MFSR error mode bit)
Emulation Facilities	Disabled	Disabled	Unchanged

APPENDIX C — BOUNDARY SCAN DESCRIPTION

The following table shows the ordering of the STP1021A boundary scan chain. Pin 0 is connected to TDO, while pin 301 is connected to TDI.

TABLE 7: The STP1021A Boundary Scan Bit Definition

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
0	breset_in	44	spare2_in	88	spare5_out	132	pipe5_out	176	data48_out	220	data30_out	264	data15_out
1	error_out	45	we7_out	89	spare5_in	133	allboe	177	data48_in	221	data30_in	265	data15_in
2	erboe	46	we6_out	90	addr19_out	134	pipe6_out	178	pipesel1_in	222	data29_out	266	data14_out
3	addr0_out	47	we5_out	91	addr19_in	135	pipe7_out	179	pipesel0_in	223	data29_in	267	data14_in
4	addr0_in	48	we4_out	92	addr20_out	136	pipe8_out	180	data47_out	224	data28_out	268	data13_out
5	addr1_out	49	wee_in	93	addr20_in	137	pipe9_out	181	data47_in	225	data28_in	269	data13_in
6	addr1_in	50	srboe	94	addr20b_out	138	pipe10_out	182	data46_out	226	l971	270	data12_out
7	addr2_out	51	we3_out	95	addr21_out	139	pipe11_out	183	data46_in	227	dpar4_out	271	data12_in
8	addr2_in	52	we2_out	96	addr21_in	140	data63_out	184	data45_out	228	dpar4_in	272	l1014
9	addr3_out	53	we1_out	97	addr22_out	141	data63_in	185	data45_in	229	data27_out	273	dpar6_out
10	addr3_in	54	we0_out	98	addr22_in	142	data62_out	186	data44_out	230	data27_in	274	dpar6_in
11	l435	55	spare3_out	99	adboe3	143	data62_in	187	data44_in	231	data26_out	275	data11_out
12	addr4_out	56	spare3_in	100	addr23_out	144	data61_out	188	l1017	232	data26_in	276	data11_in
13	addr4_in	57	cmds_out	101	addr23_in	145	data61_in	189	dpar2_out	233	data25_out	277	data10_out
14	addr5_out	58	cmds_in	102	addr24_out	146	data60_out	190	dpar2_in	234	data25_in	278	data10_in
15	addr5_in	59	stboe1	103	addr24_in	147	data60_in	191	data43_out	235	data24_out	279	data9_out
16	addr6_out	60	rgrt_in	104	addr25_out	148	daboe0	192	data43_in	236	data24_in	280	data9_in
17	addr6_in	61	wgrt_in	105	addr25_in	149	dpar0_out	193	data42_out	237	data23_out	281	data8_out
18	addr7_out	62	rrdy_in	106	addr26_out	150	dpar0_in	194	data42_in	238	data23_in	282	data8_in
19	addr7_in	63	wrdy_in	107	addr26_in	151	data59_out	195	data41_out	239	data22_out	283	data7_out
20	addr8_out	64	mexc_in	108	addr27_out	152	data59_in	196	data41_in	240	data22_in	284	data7_in
21	addr8_in	65	retry_in	109	addr27_in	153	data58_out	197	data40_out	241	data21_out	285	data6_out
22	addr9_out	66	burst_out	110	addr28_out	154	data58_in	198	data40_in	242	data21_in	286	data6_in
23	addr9_in	67	stboe2	111	addr28_in	155	data57_out	199	data39_out	243	data20_out	287	data5_out
24	addr10_out	68	rd_out	112	addr29_out	156	data57_in	200	data39_in	244	data20_in	288	data5_in
25	addr10_in	69	rd_in	113	addr29_in	157	data56_out	201	data38_out	245	l965	289	data4_out
26	addr11_out	70	wr_out	114	addr30_out	158	data56_in	202	data38_in	246	dpar5_out	290	data4_in
27	addr11_in	71	wr_in	115	addr30_in	159	data55_out	203	data37_out	247	dpar5_in	291	daboe7
28	addr12_out	72	spare4_out	116	adboe4	160	data55_in	204	data37_in	248	data19_out	292	dpar7_out
29	addr12_in	73	spare4_in	117	addr31_out	161	data54_out	205	data36_out	249	data19_in	293	dpar7_in
30	addr13_out	74	oe_out	118	addr31_in	162	data54_in	206	data36_in	250	data18_out	294	data3_out
31	addr13_in	75	oe_in	119	addr32_out	163	data53_out	207	l1044	251	data18_in	295	data3_in
32	adboe1	76	oeboe	120	addr32_in	164	data53_in	208	dpar3_out	252	data17_out	296	data2_out
33	addr14_out	77	su_out	121	addr33_out	165	data52_out	209	dpar3_in	253	data17_in	297	data2_in
34	addr14_in	78	cchbl_out	122	addr33_in	166	data52_in	210	data35_out	254	data16_out	298	data1_out
35	addr15_out	79	adboe2	123	addr34_out	167	daboe1	211	data35_in	255	data16_in	299	data1_in
36	addr15_in	80	size0_out	124	addr34_in	168	dpar1_out	212	data34_out	256	test_in	300	data0_out
37	addr16_out	81	size1_out	125	addr35_out	169	dpar1_in	213	data34_in	257	srmtst_in	301	data0_in
38	addr16_in	82	ldst_out	126	addr35_in	170	data51_out	214	data33_out	258	spare0_out		
39	addr17_out	83	stboe3	127	pipe0_out	171	data51_in	215	data33_in	259	spare0_in		
40	addr17_in	84	demap_out	128	pipe1_out	172	data50_out	216	data32_out	260	lirl0_in		
41	addr18_out	85	demap_in	129	pipe2_out	173	data50_in	217	data32_in	261	lirl1_in		
42	addr18_in	86	csa_out	130	pipe3_out	174	data49_out	218	data31_out	262	lirl2_in		
43	spare2_out	87	pend_in	131	pipe4_out	175	data49_in	219	data31_in	263	lirl3_in		

ORDERING INFORMATION

Part Number	Speed	Description
STP1021APGA-85	85 MHz	85 MHz SuperSPARC-II Microprocessor
STP1021APGA-75	75 MHz	75 MHz SuperSPARC-II Microprocessor

Document Part Number: STP1021A