Sun

STP1010

July 1994

microSPARC™

DATA SHEET — Highly Integrated 32-Bit RISC Microprocessor

DESCRIPTION

The microSPARC 32-bit microprocessor is a highly integrated RISC CPU Implementing the SPARC Architecture ver.8. Due to its relative high performance and low cost, it is ideally suited for low-cost single processor applications.

The microSPARC includes: A pipelined Integer Unit (IU), a Floating Point Unit (FPU), separate Instruction and Data Caches and a fully implemented Reference MMU.

It interfaces efficiently with the rest of the system, by incorporating complete DRAM and SBus interface and controllers. Testability at the system level is provided by supporting a complete JTAG interface.

Operating at the nominal internal frequency of 50 MHz, the throughput achieved is 26 SPECint92 and 21 SPECfp92.

Features

- SPARC High Performance RISC architecture
- Operating Frequency at 50 MHz
- 7 window, 120-word register file
- 4 Kbyte Instruction cache, 2 Kbyte Data cache
- On-chip Memory Management Unit
- Integrated Floating Point Processor
- Interface to S-Bus at 1/2 system clock
- Integrated DRAM controller
- IEEE1149.1 (JTAG) boundary scan test bus
- TAB Packaging

Benefits

- Compatible with 7500 SPARC applications and development tools
- 50 MIPs peak performance
- Fast interrupt response, procedure calls and program execution
- Decouples processor operation from slow external memory
- Support for sophisticated operating systems with memory protection and virtual addressing
- 12 MFlops peak performance
- Connection to industry standard expansion bus
- Simple, low part count system design
- Ease of manufacturing test
- Low cost, high density board assembly

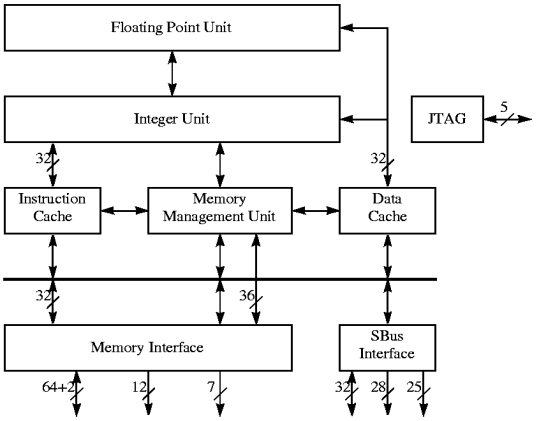


Figure 1. microSPARC Block Diagram

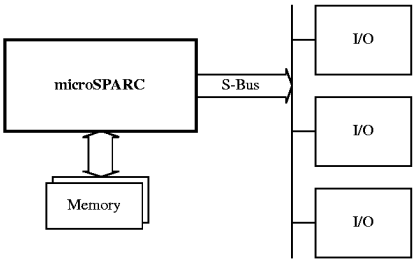


Figure 2. Typical microSPARC System Block Diagram

TECHNICAL OVERVIEW

Integer Unit (IU)

The STP1010 Integer Unit executes SPARC integer instructions as defined in the SPARC Architecture Manual (Version 8). The IU contains 120 *r* registers (7-window registers and 8-global registers) and operates on instructions using a five-stage pipeline.

Floating Point Unit (FPU)

The FPU fully executes all single and double precision FP instructions as defined in the SPARC Architecture Manual (Version 8). Quad-precision instructions and *fsmuld* instruction are not implemented. They are trapped to *unimplemented_FPop*. Since all implemented instructions are executed within hardware, this FPU never generates *unfinished_FPop* exception. The FPU contains 32x32 *f* registers.

Memory Management Unit (MMU)

The MMU is compatible with the SPARC Reference MMU, as defined by the SPARC Architecture Manual Version 8 appendix H "SPARC Reference MMU Architecture". The STP1010 MMU also serves as an I/ O MMU. This MMU translates 32-bit virtual addresses of each running process to 31-bit physical addresses in memory. The 3-high order bits of Physical address are maintained to support memory mapping into 8 different address spaces. The MMU supports 64 contexts.

The MMU also protects memory so that a process can be prohibited from reading or writing to the address space of another process.

The MMU controls arbitration between I/ O, Data Cache, Instruction Cache, and TLB references to memory.

The MMU contains a 32-entry fully associative TLB and uses a pseudo random algorithm for the replacement of TLB entries.

Instruction Cache

The Instruction Cache is a 4-KByte, virtually addressed physically tagged cache. The Instruction Cache data is organized as 128 lines of 32 bytes.

Data Cache

The Data Cache is 2-KByte, direct mapped, physically tagged, write through cache with no write allocate. The data store is organized as 128 lines of 16 bytes.

Data cache read and write hits take no extra pipe cycle except double-word operations. *LDD* takes 2 cycles to complete (1 extra cycle) and *STD* takes 3 cycles to complete (2 extra cycles).

There are two Store Buffers to hold data being stored from the IU or FPU to memory or other physical devices. The Store Buffers are 32-bit register.

Memory Interface

The STP1010 provides a complete DRAM controller which generates all the signals necessary to support up to 128 MBytes of system memory.

The DRAM bus is 64 bits wide with two parity bits, one covering each 32 bits of data.

The system DRAM is organized as four banks, each of which may be 2 MBytes, 8 MBytes, or 32 MBytes depending upon the size of DRAM used.

The STP1010 RAM Refresh Control logic provides complete DRAM Refresh Control. This Refresh Controller performs $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh. Refresh interval is programmable.

SBus Interface

The SBus Interface performs all functions necessary to interface the STP1010 to the SBus, including dynamic bus sizing, cycle re-run control, burst cycle re-ordering, arbitration, and general SBus control.

SBus Controller (SBC)

The STP1010 SBC (SBus Controller) controls SBus devices connected to the bus. The SBC Control logic operates as the system SBus Controller. It supports:

- Programmed Input/ Output (PIO) transactions between the CPU and SBus devices.
- Direct Virtual Memory Access (DVMA) transactions between SBus masters and local resources. (referred to as Local DVMA)
- Direct Virtual Memory Access (DVMA) transactions between SBus masters and other SBus slave devices. (referred to as Bypass DVMA)

The SBC works with the MMU to arbitrate the system and memory resources and for I/ O address translations.

For further details on SBus specification, please refer to the SBus Specification Rev A.2. available from Sun Microsystems. The STP1010 does not comply with SBus Rev B.0.

JTAG Test Bus Interface

The STP1010 has a five-wire Test Access Port (TAP) interface to support internal scan, boundary scan and clock control. This interface is compatible with IEEE 1149.1 specification, “IEEE Standard Test Access Port and Boundary Scan Architecture”. The TAP supports a BYPASS instruction which places a minimum shift path (1 bit) between the chip’s TDI and TDO pins. This allow efficient access to any single chip in the daisy-chain without board-level multiplexing.

TAP Controller

The TAP controller is a synchronous Finite State Machine (FSM) which controls the sequence of operations of the JTAG test circuitry, in response to changes at the JTAG bus. The TAP controller is asynchronous with respect to the system clock(s), and can therefore be used to control the clock control logic.

The TAP FSM implements the state (16 states) diagram as detailed in the 1149.1 protocol.

TABLE 1: Pin Descriptions

Signal	Description
MEMDATA[63:0]	64-bit bidirectional memory data bus for accessing main memory.
MEMPAR[1:0]	Bidirectional memory data parity pins. Parity is provided on a word basis (for DRAM only).[1]
MEMADDR[11:0]	DRAM address output pins. These memory address pins require external buffering to provide the necessary drive for the DRAMs.
RAS_L[3:0]	DRAM Row Address Strobe. Four separate RAS signals, buffered externally to provide sufficient drive to connect directly to the DRAMs. 4 DRAM banks are supported.[1]
CAS_L[1:0]	DRAM Column Address Strobes. Two separate CAS signals are provided for word access, and are buffered externally to provide sufficient drive to connect directly to the DRAMs.[1]
MWE_L	DRAM Write Enable output pin. MWE is buffered externally to provide sufficient drive to connect directly to the DRAMs and VRAMs.
SBADDR[27:0]	SBus Address output pins, to provide the Physical Address to SBus slave devices.
SBDATA[31:0]	Bidirectional SBus data pins. The 32-bit SBus data pins provide SBus support for the CPU, and support DBMA cycle access via the CPU SBus controller.
SLVSEL_L[4:0]	Output Slave Select pins. A separate slave select is driven to each SBus slot and the I/O chip. This is used in conjunction with the physical address for accessing each slot/device.
SB_SIZE[2:0]	Bidirectional SBus transfer Size description pins. These three pins describe (encoded) the size of the data transfer of the current SBus operation (See SBus controller section).
SB_READ	Bidirectional SBus Read/Write pin. This pin indicates whether the current transfer is a read or a write operation.
SBCLK	SBus clock (1/2 internal system clock) output pin.
SB_AS_L	SBus Address Strobe Output pin.
SB_ACK_L[2:0]	Transfer Acknowledgment bidirectional pins. The ACK[2:0] pins return the status (encoded) of the current SBus transfer, from the slave.
SB_LERR_L	SBus Late data Error input pin. This pin is driven by the current SBUs slave, and aborts the current SBus transfer.
SB_BR_L[4:0]	Bus Request input pins (1/SBus slot).
SB_BG_L[4:0]	Bus Grant output pins 1/SBus slot).
IRL[3:0]	Interrupt Request Lines input pins. These 4 pins represent the encoded highest priority, pending interrupt. These pins are driven by the I/O chip, directly to the CPU.
CP_STAT_L[1:0]	Active low CP Status output pins. Used to indicate CP interrupt/trap status as follows: 11 - Normal 10 - Level 15 interrupt 01 - Trap occurred, when trap disabled 00 - Reserved
JTAG_CK	Test (JTAG) input clock for boundary scan registers.
JTAG_MS	Test Mode Select input pin.

TABLE 1: Pin Descriptions (Continued)

Signal	Description
JTAG_TDI	Test Data Input pin (JTAG standard).
JTAG_TRST	JTAG Reset pin (JTAG standard).
JTAG_TDO	Test Data Output pin (JTAG standard).
EXT_CLK	CPU input clock pin.
INPUT_RESET_L	Power-up reset input pin.
EXT_EVENT_L	This input pin can be used to stop clocks during debug on an externally triggered event.
INT_EVENT_L	This output is for use during debug. It is an internal counter overflow bit.
REF_CLOCK	Clock output at 2x INPUT_CLOCK frequency.
RI_REQ	This output signal indicates that the MMU is doing either an operation to memory, to an ASI, control space, or an SBus device. This signal can be used to validate the physical address observation on the SBus address pins using view mode during debug.
VDDC, VSSC	5.0V core power/ground.
VDDP, VSSP	Periphery power/ground.

1. MEMPAR1 and CAS_L0 are associated with MEMDATA[63:32].
   MEMPAR0 and CAS_L1 are associated with MEMDATA[31:00].
   RAS_L0 selects 1st 32 MByte Bank.
   RAS_L1 selects 2nd 32 MByte Bank.
   RAS_L2 selects 3rd 32 MByte Bank.
   RAS_L3 selects 4th 32 MByte Bank.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Symbol	Parameter	Min	Max	Units
V_{DDC}	Core supply voltage	-0.5	7	V
V_{DDP}	Periphery supply voltage	-0.5	7	V
V_{IN}	Input voltage (any pin)	-0.5	7	V
I_{IK}	Input clamp current (any pin)	-20	20	mA
I_{OK}	Output clamp current	-50	50	mA
P_D	Continuous power dissipation	–	6	W
T_J	Operating junction temperature	0	125	°C
T_S	Storage temperature	-65	150	°C
V_{SD}	Static discharge voltage	2000	–	V

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DDC}	Core supply voltage	4.75	5.0	5.25	V
V_{DDP}	Peripheral supply voltage	4.75	5.0	5.25	V
V_{SSC} , V_{SSP}	Ground	-0.2	0	0.2	V
V_{IODC}	DC I/O voltage	0	–	V_{DDP}	V
V_{IH}	Input high voltage	2.0	–	–	V
V_{IHC}	Input high voltage (IN_CLK)	2.4	–	–	V
V_{IL}	Input low voltage	–	–	0.8	V
I_{OH}	High-level output current	–	–	1.0	mA
I_{OL}	Low-level output current	–	–	2.0	mA
T_A	Operating temperature (free-air)	0	–	70	°C
T_J	Junction temperature [1]	15	–	95	°C

1. The maximum allowed operating temperature depends on system heat sinking and air flow velocity. This is not a guaranteed specification and should be determined for each system configuration.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	V_{CC} = 5V ±5%	2.4	–	–	V
V_{OL}	Output low voltage		–	–	0.4	V
I_{IL}	Low-level input current	Input signals except JTAG	–	–	-20	µA
		JTAG signals	–	–	-2	µA
I_{IH}	High-level input current	Input signals except JTAG	–	–	20	µA
		JTAG signals	–	–	50	µA
I_{OZ}	High-impedance output current [1]		-10	–	10	µA
I_{CC}	Dynamic supply current		–	700	1000	mA
I_{CCQ}	Quiescent power supply current		–	–	2	mA
C_I	Input capacitance [2]		–	10	–	pF
C_O	Output capacitance [2]		–	10	–	pF

1. Except pins which cannot be hi-impedance: CP_STAT, INT_EVENT, JTDO, MADDR[11:0], MRAS, MCAS, MWE, REF_CLK, SBADDR[27:0], SBAS, SBCLK, SBGR[4:0], and SBSEL[4:0].
2. This specification is provided as an aid to board design and is not guaranteed during manufacturing testing.

AC Characteristics (Memory Interface)

Symbol	Description	Conditions	Min	Max	Unit
t_{SU}	Setup time to REF_CLK ↑	MDATA[63:0], MPAR[1:0]	8.0	–	ns
t_H	Hold time from $\overline{MCAS}$ ↑	MDATA[63:0], MPAR[1:0]	2.0	–	ns
$t_{SU(MDATA)}$	MEMDATA[63:0] to $\overline{MCAS}$ ↓	I_{OL} = Max, I_{OH} = Max V_{LOAD} = 2.1V, C_L = 35 pF (See *Figure 4*)	5	–	ns
$t_{SU(MPAR)}$	MEMPAR[1:0] to $\overline{MCAS}$ ↓		5	–	ns
$t_{SU(MADDR)}$	MEMADDR[11:0] to $\overline{MCAS}$ ↓		12	–	ns
$t_{P(MRAS)}$	REF_CLK ↑ to MRAS[3:0] ↓		–	16	ns
	REF_CLK ↑ to MRAS[3:0] ↑		–	4	ns
$t_{P(MCAS)}$	REF_CLK ↑ to $\overline{MCAS}$[1:0]		–	10	ns
$t_{P(MWE)}$	REF_CLK ↑ to $\overline{MWE}$		–	10	ns
$t_{OH(MDATA)}$	REF_CLK ↑ to MEMDATA[63:0]		0	–	ns
$t_{OH(MPAR)}$	REF_CLK ↑ to MEMPAR[1:0]		0	–	ns
$t_{OH(MADDR)}$	$\overline{MCAS}$ ↓ to MEMADDR[11:0]		16	–	ns
$t_{OH(MRAS)}$	REF_CLK ↑ to MRAS[3:0] ↓		0	–	ns
	REF_CLK ↑ to MRAS[3:0] ↑		0	–	ns
$t_{OH(MCAS)}$	REF_CLK ↑ to $\overline{MCAS}$[1:0]		0	–	ns
$t_{OH(MWE)}$	REF_CLK ↑ to $\overline{MWE}$		0	–	ns

AC Characteristics (JTAG Interface)

Symbol	Description	Conditions	Min	Max	Unit
t_{SU}	Setup time to JTCK ↑	JTMS, JTDI	20.0	–	ns
t_H	Hold time from JTCK ↑	JTMS, JTDI	0	–	ns
f_{JTCK}	JTCK clock frequency	JTCK	1.0	20.0	MHz
$t_{P(JTDO)}$	JTCK ↑ to JTDO	I_{OL} = Max, I_{OH} = Max V_{LOAD} = 2.1V, C_L = 35 pF (See *Figure 4*)	–	20.0	ns
$t_{OH(JTDO)}$	JTCK ↑ to JTDO		0	–	ns

AC Characteristics (SBus Interface) [1]

Symbol	Description	Conditions	Min	Max	Unit
t_{SU}	Setup time to SBCLK↑	$\overline{SBLERR}$, $\overline{SBRQ}$[4:0], SBDATA[31:0], SBSIZE[2:0], SBREAD, $\overline{SBACK}$[2:0]	10.5	–	ns
t_H	Hold time from SBCLK↑	$\overline{SBLERR}$, $\overline{SBRQ}$[4:0], SBDATA[31:0], SBSIZE[2:0], SBREAD, $\overline{SBACK}$[2:0]	2.0	–	ns
$t_{SO(SBDATA)}$	SBCLK↑ to SBDATA[31:0]	I_{OL} = Max, I_{OH} = Max V_{LOAD} = 2.1V, C_L = 35 pF (See *Figure 4*)	18.0	–	ns
$t_{SO(SBSIZE)}$	SBCLK↑ to SBSIZE[2:0]		18.0	–	ns
$t_{SO(SBREAD)}$	SBCLK↑ to SBREAD		16.0	–	ns
$t_{SO(SBACK)}$	SBCLK↑ to $\overline{SBACK}$[2:0]		18.0	–	ns
$t_{SO(SBSEL)}$	SBCLK↑ to $\overline{SBSEL}$[4:0]		16.0	–	ns
$t_{SO(SBADDR)}$	SBCLK↑ to SBADDR[27:0]		16.0	–	ns
$t_{SO(SBAS)}$	SBCLK↑ to $\overline{SBAS}$		18.0	–	ns
$t_{SO(SBGR)}$	SBCLK↑ to $\overline{SBGR}$[4:0]		16.0	–	ns
$t_{P(SBCLK↑)}$	REF_CLK↑ to SBCLK↑		0	1.0	ns
$t_{P(SBCLK↓)}$	REF_CLK↑ to SBCLK↑		0	1.0	ns
$t_{OH(SBDATA)}$	SBCLK↑ to SBDATA[31:0] [2]		2.0	–	ns
$t_{OH(SBSIZE)}$	SBCLK↑ to SBSIZE[2:0] [2]		0.5	–	ns
$t_{OH(SBREAD)}$	SBCLK↑ to SBREAD [2]		0.5	–	ns
$t_{OH(SBACK)}$	SBCLK↑ to $\overline{SBACK}$[2:0]		3.5	–	ns
$t_{OH(SBSEL)}$	SBCLK↑ to $\overline{SBSEL}$[4:0]		5.0	–	ns
$t_{OH(SBADDR)}$	SBCLK↑ to SBADDR[27:0]		5.0	–	ns
$t_{OH(SBAS)}$	SBCLK↑ to $\overline{SBAS}$		3.5	–	ns
$t_{OH(SBGR)}$	SBCLK↑ to $\overline{SBGR}$[4:0]		5.0	–	ns

1. These test values are designed to guarantee operation to SBus specification under SBus loading conditions.
2. The SBus specification calls for minimum hold time of 2.5 ns for these parameters. Test equipment constraints result in a guaranteed minimum hold time which is less than 2.5 ns.

AC Characteristics (Input Clock)

Symbol	Description	Signals	Min	Typ	Max	Unit
$t_{W(ICH)}$	Clock input high pulse width	IN_CLK	4.5	5.0	5.5	ns
$t_{W(ICL)}$	Clock input low pulse width	IN_CLK	4.5	5.0	5.5	ns
$t_{W(ICP)}$	Input clock period	IN_CLK	10.0	–	–	ns
t_{rC}	Clock rise time	IN_CLK	–	–	1.5	ns
t_{fC}	Clock fall time	IN_CLK	–	–	1.5	ns

AC Characteristics (Misc. Signals)

Symbol	Description	Conditions	Min	Max	Unit
$t_{P(CP\_STAT)}$	REF_CLK ↑ to CP_STAT ↑		–	[1]	
$t_{OH(CP\_STAT)}$	REF_CLK ↑ to CP_STAT ↑		5	–	cycle
$t_{SU(IRQ)}$	Setup to REF_CLK ↑	IRQ[3:0]	2	–	cycle
$t_{H(IRQ)}$	Hold from REF_CLK ↑	IRQ[3:0]	[1]	–	
$t_{SU(EXT\_EVENT)}$	Setup to REF_CLK ↑	EXT_EVENT	9.0	–	ns
$t_{H(EXT\_EVENT}$	Hold from REF_CLK ↑	EXT_EVENT	0.0	–	ns

1. Functionality is only tested for these signals

Load Circuit Parameters

Timing Parameters		C_{LOAD} [1] (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{ON}	t_{PZH} t_{PZL}	35	2.0	-0.37	2.1
t_{DLS}	t_{PHZ} t_{PLZ}	35	2.0	-0.37	2.1
t_{PD}		35	2.0	-0.37	2.1
$t_{PD(MSH)}$		35	6.0	-0.37	2.1

1. C_{LOAD} includes probes and test fixture capacitance.

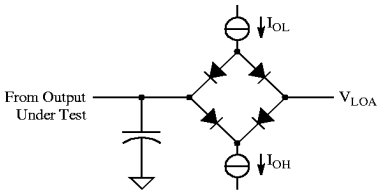
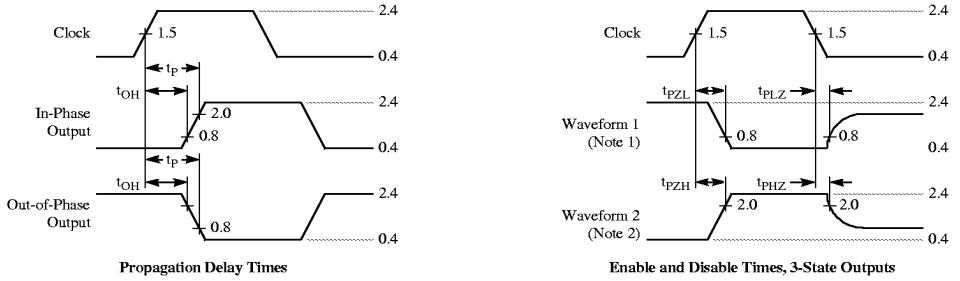


Figure 3. Load Circuit



1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. Fo r t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are specified values.

Figure 4. Voltage Waveforms

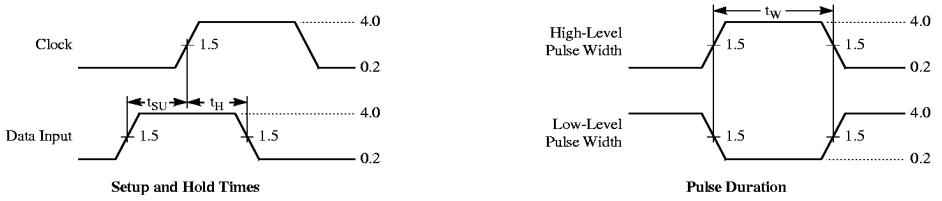


Figure 5. Voltage Waveforms

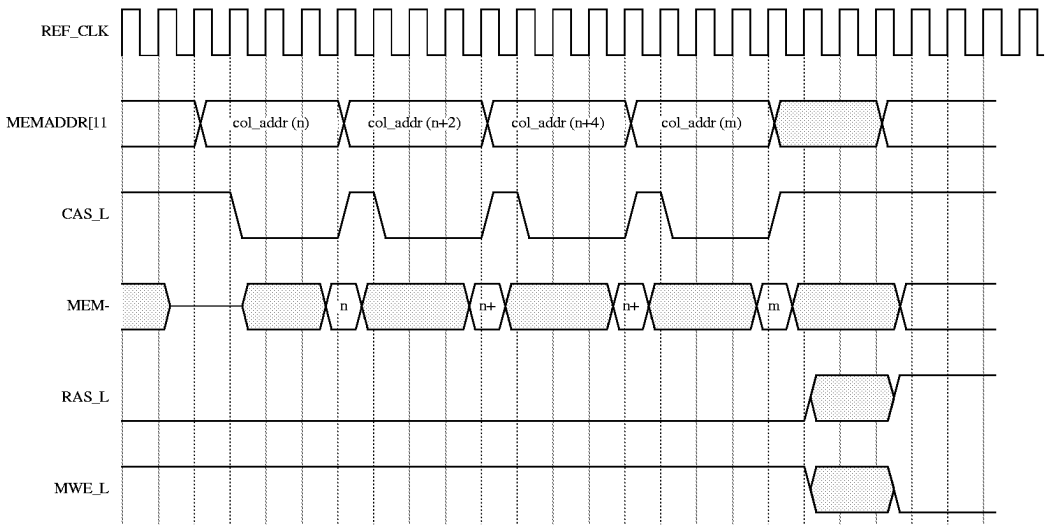


Figure 6. Page Mode Read Following a Read

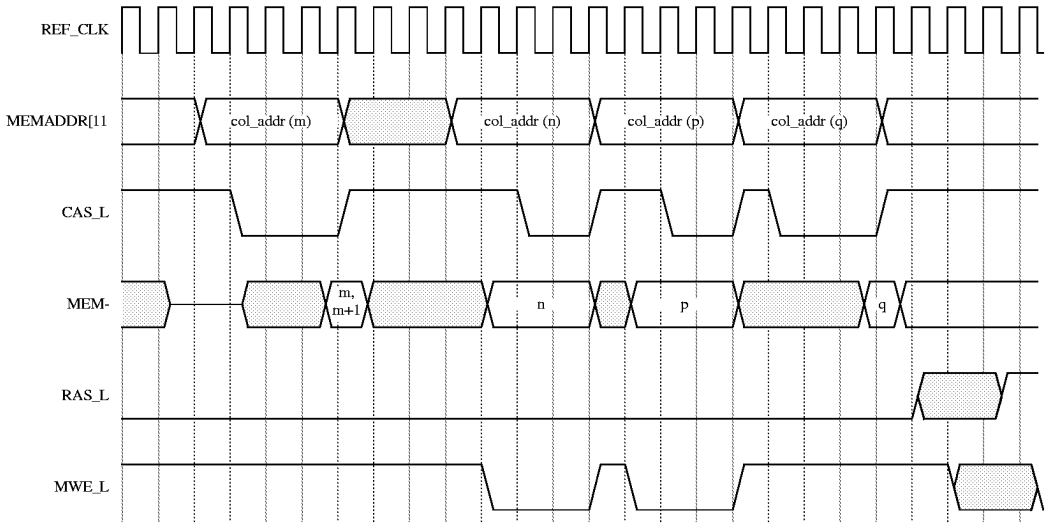


Figure 7. Page Mode Write Following a Read

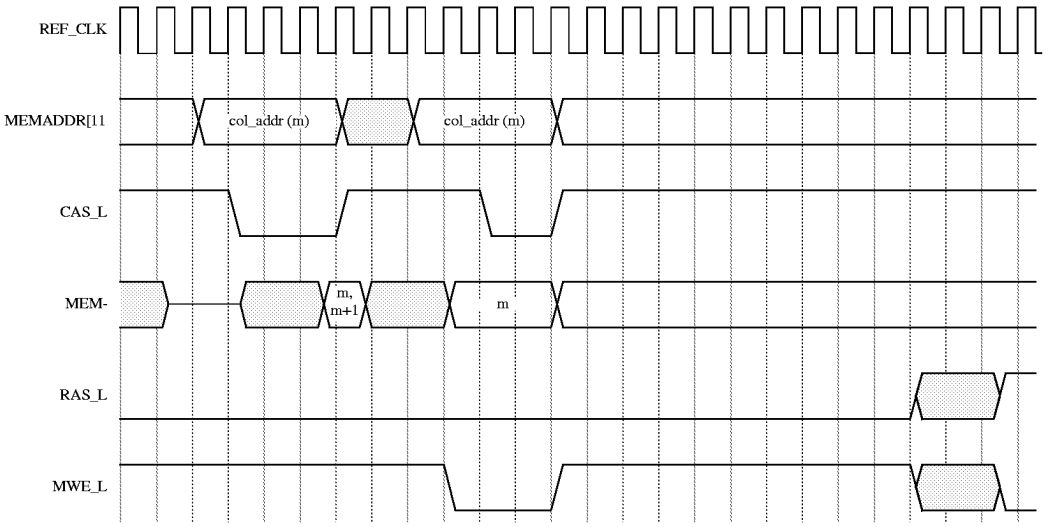


Figure 8. Page Mode Read-Modify-Write Sequence

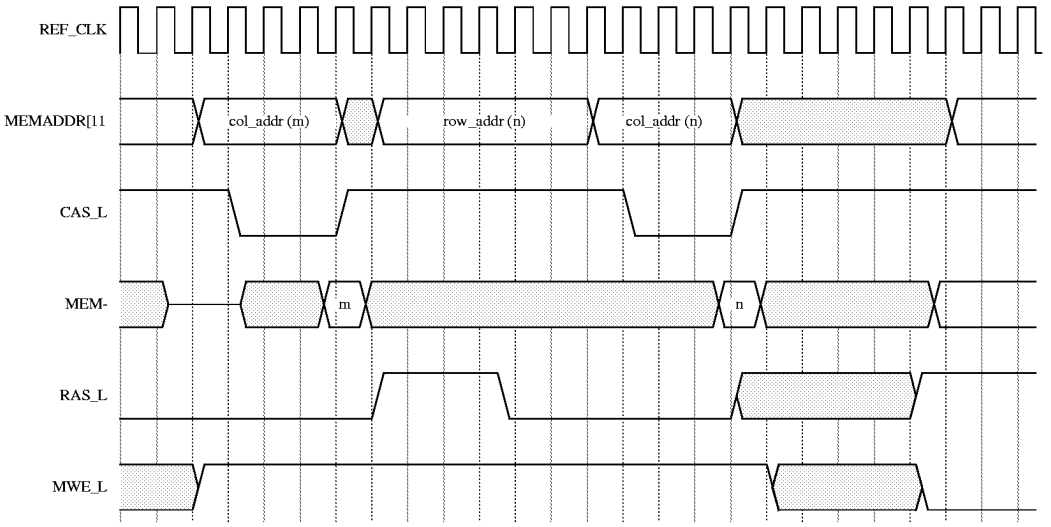


Figure 9. Non Page Read Following a Read

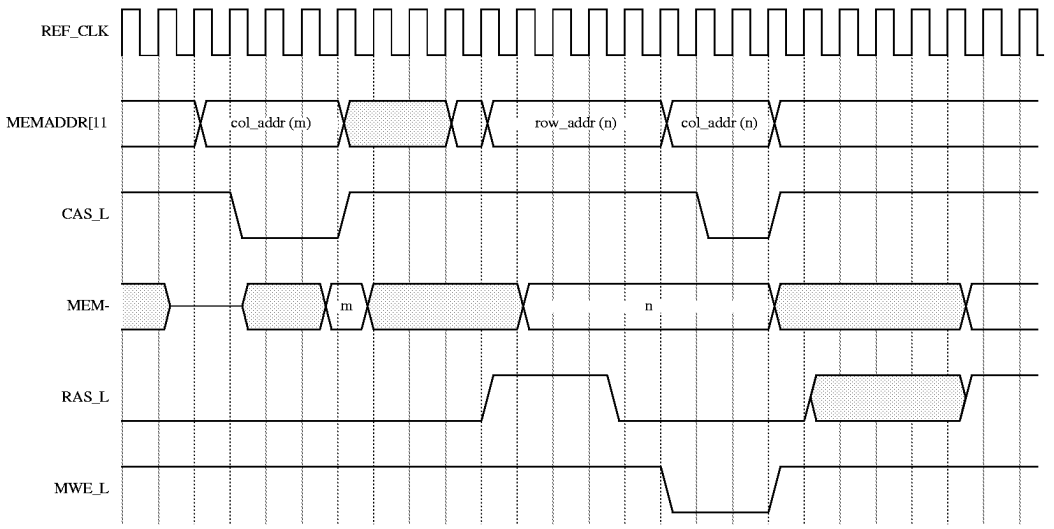
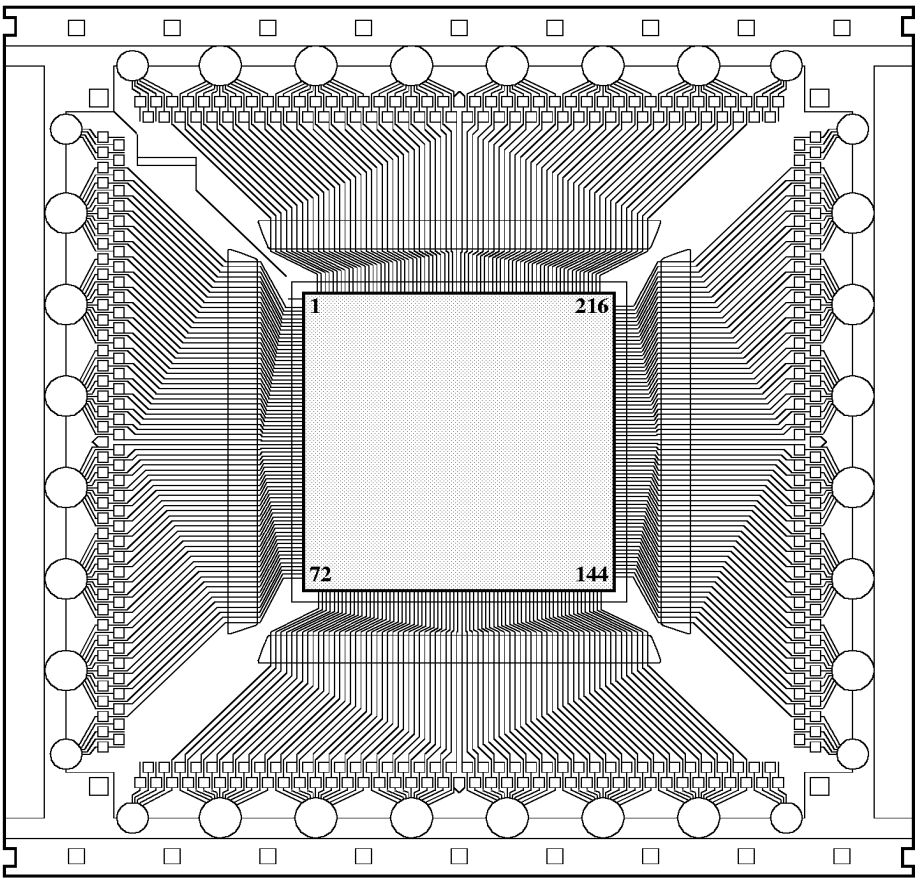


Figure 10. Non Page Write Following a Read

288TAB PACKAGE PIN ASSIGNMENT

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	VCCC	49	MEMDATA [33]	97	MEMDATA [5]	145	GNDC	193	GNDP	241	JTDI
2	MEMPAR[1]	50	GNDP	98	MEMDATA [4]	146	SBDATA [16]	194	SBACK[1]	242	GNDP
3	MEMDATA [63]	51	MEMDATA [32]	99	MEMDATA [3]	147	SBADDR [16]	195	SBACK[0]	243	JTDO
4	MEMDATA [62]	52	VCCP	100	VCCP	148	SBDATA [15]	196	SBRQ[4]	244	MEMADDR[11]
5	VCCP	53	VCCC	101	MEMDATA [2]	149	SBADDR [15]	197	SBRQ[3]	245	Reserved
6	MEMDATA [61]	54	MEMPAR[0]	102	GNDP	150	SBDATA [14]	198	GNDC	246	JTMS
7	GNDP	55	GNDC	103	MEMDATA [1]	151	SBADDR [14]	199	SBRQ[2]	247	JTRST
8	MEMDATA [60]	56	MEMDATA [31]	104	MEMDATA [0]	152	GNDP	200	VCCC	248	RESET
9	MEMDATA [59]	57	MEMDATA [30]	105	SBDATA [31]	153	SBDATA [13]	201	SBRQ[1]	249	JTCK
10	MEMDATA [58]	58	GNDP	106	VCCC	154	SBADDR [13]	202	SBRQ[0]	250	VCCC
11	MEMDATA [57]	59	MEMDATA [29]	107	SBDATA [30]	155	SBDATA [12]	203	SBLERR	251	IN_CLK
12	GNDP	60	MEMDATA [28]	108	GNDC	156	SBADDR [12]	204	SBSEL[4]	252	GNDC
13	MEMDATA [56]	61	MEMDATA [27]	109	GNDP	157	SBDATA [11]	205	SBSEL[3]	253	GNDP
14	VCCP	62	VCCP	110	SBDATA [29]	158	SBADDR [11]	206	GNDP	254	SBCLK
15	MEMDATA [55]	63	MEMDATA [26]	111	VCCP	159	VCCP	207	SBSEL[2]	255	VCCP
16	MEMDATA [54]	64	GNDP	112	SBDATA [28]	160	SBDATA [10]	208	VCCP	256	IRQ[3]
17	VCCC	65	MEMDATA [25]	113	SBDATA [27]	161	VCCC	209	SBSEL[1]	257	IRQ[2]
18	MEMDATA [53]	66	MEMDATA [24]	114	VCCC	162	SBADDR [10]	210	SBSEL[0]	258	IRQ[1]
19	GNDC	67	MEMDATA [23]	115	SBADDR [27]	163	GNDC	211	SBSIZE[2]	259	IRQ[0]
20	GNDP	68	MEMDATA [22]	116	GNDC	164	GNDP	212	GNDP	260	MEMADDR[10]
21	MEMDATA [52]	69	GNDP	117	SBDATA [26]	165	SBDATA [9]	213	SBSIZE[1]	261	MEMADDR[9]
22	MEMDATA [51]	70	MEMDATA [21]	118	SBADDR [26]	166	SBADDR [9]	214	SBSIZE[0]	262	GNDP
23	MEMDATA [50]	71	VCCP	119	GNDP	167	SBDATA [8]	215	SBREAD	263	MEMADDR[8]
24	VCCP	72	VCCC	120	SBDATA [25]	168	SBADDR [8]	216	GNDC	264	VCCP
25	MEMDATA [49]	73	GNDC	121	SBADDR [25]	169	SBDATA [7]	217	VCCC	265	MEMADDR[7]
26	GNDP	74	MEMDATA [20]	122	VCCC	170	SBADDR [7]	218	VCCP	266	MEMADDR[6]
27	MEMDATA [48]	75	MEMDATA [19]	123	SBDATA [24]	171	SBDATA [6]	219	SBGR[4]	267	MEMADDR[5]
28	MEMDATA [47]	76	MEMDATA [18]	124	GNDC	172	SBADDR [6]	220	GNDP	268	GNDP
29	MEMDATA [46]	77	GNDP	125	SBADDR [24]	173	GNDP	221	SBGR[3]	269	MEMADDR[4]
30	VCCC	78	MEMDATA [17]	126	SBDATA [23]	174	GNDC	222	SBGR[2]	270	MEMADDR[3]
31	MEMDATA [45]	79	MEMDATA [16]	127	SBADDR [23]	175	SBDATA [5]	223	SBGR[1]	271	MEMADDR[2]
32	GNDC	80	MEMDATA [15]	128	VCCP	176	VCCC	224	SBGR[0]	272	VCCP
33	GNDP	81	VCCP	129	SBDATA [22]	177	SBADDR [5]	225	GNDP	273	VCCC
34	MEMDATA [44]	82	MEMDATA [14]	130	SBADDR [22]	178	VCCP	226	EXT_EVENT	274	MEMADDR[1]
35	VCCP	83	GNDP	131	GNDP	179	SBDATA [4]	227	N.C.	275	GNDC
36	MEMDATA [43]	84	MEMDATA [13]	132	SBDATA [21]	180	SBADDR [4]	228	VCCP	276	GNDP
37	MEMDATA [42]	85	MEMDATA [12]	133	SBADDR [21]	181	SBDATA [3]	229	N.C.	277	MEMADDR[0]
38	MEMDATA [41]	86	GNDC	134	SBDATA [20]	182	SBADDR [3]	230	N.C.	278	MRAS[3]
39	GNDP	87	MEMDATA [11]	135	SBADDR [20]	183	SBDATA [2]	231	N.C.	279	MRAS[2]
40	MEMDATA [40]	88	VCCC	136	SBDATA [19]	184	SBADDR [2]	232	CP_STAT[1]	280	MRAS[1]
41	MEMDATA [39]	89	MEMDATA [10]	137	SBADDR [19]	185	GNDP	233	GNDP	281	GNDP
42	MEMDATA [38]	90	GNDP	138	SBDATA [18]	186	SBDATA [1]	234	CP_STAT[0]	282	MRAS[0]
43	VCCP	91	MEMDATA [9]	139	SBADDR [18]	187	SBADDR [1]	235	INT_EVENT	283	VCCP
44	MEMDATA [37]	92	VCCP	140	GNDP	188	SBDATA [0]	236	REF_CLK	284	MCAS[1]
45	GNDP	93	MEMDATA [8]	141	SBDATA [17]	189	SBADDR [0]	237	GNDC	285	MCAS[0]
46	MEMDATA [36]	94	MEMDATA [7]	142	SBADDR [17]	190	SBAS	238	N.C.	286	MWE
47	MEMDATA [35]	95	MEMDATA [6]	143	VCCP	191	VCCP	239	VCCC	287	GNDP
48	MEMDATA [34]	96	GNDP	144	VCCC	192	SBACK[2]	240	VCCP	288	GNDC

MECHANICAL DATA: STP1010TAB-50



Tape Film Thickness:	0.125 mm (5 mil)
Tape Format:	JEDEC Metric, BD-24
Outer Lead Pitch:	0.25 mm (9.8 Mil)
Body Size:	20 mm square
Test PAD Pitch:	0.40 mm
Carrier Type:	JEDEC “Metric TAB Tape Carrier”, Super 48 mm
Shipping Method:	JEDEC “Metric TAB Magazine” 48 mm
Die Metallization:	UP