TSV632, TSV632A, TSV633, TSV633A TSV634, TSV634A, TSV635, TSV635A

Dual and quad rail-to-rail input/output 60 µA 880 kHz operational amplifiers

Features

- Rail-to-rail input and output
- Low power consumption: 60 µA typ at 5 V
- Low supply voltage: 1.5 V - 5.5 V
- Gain bandwidth product: 880 kHz typ
- Unity gain stability
- Low power shutdown mode: 5 nA typ
- Low offset voltage: 800 µV max (A version)
- Low input bias current: 1 pA typ
- EMI hardened op-amps
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40° C to +125° C

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

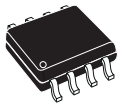
Description

The TSV63x series of dual and quad operational amplifiers offers low voltage operation and rail-to-rail input and output.

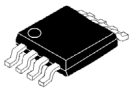
This family features an excellent speed/power consumption ratio, offering a 880 kHz gain-bandwidth product while consuming only 60 µA at 5 V supply voltage. The devices also feature an ultra-low input bias current and have a shutdown mode (TSV633, TSV635).

These features make the TSV63x family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.


SOT23-8


SO-8


DFN8 2x2


MiniSO-8


TSSOP-14


TSSOP-16

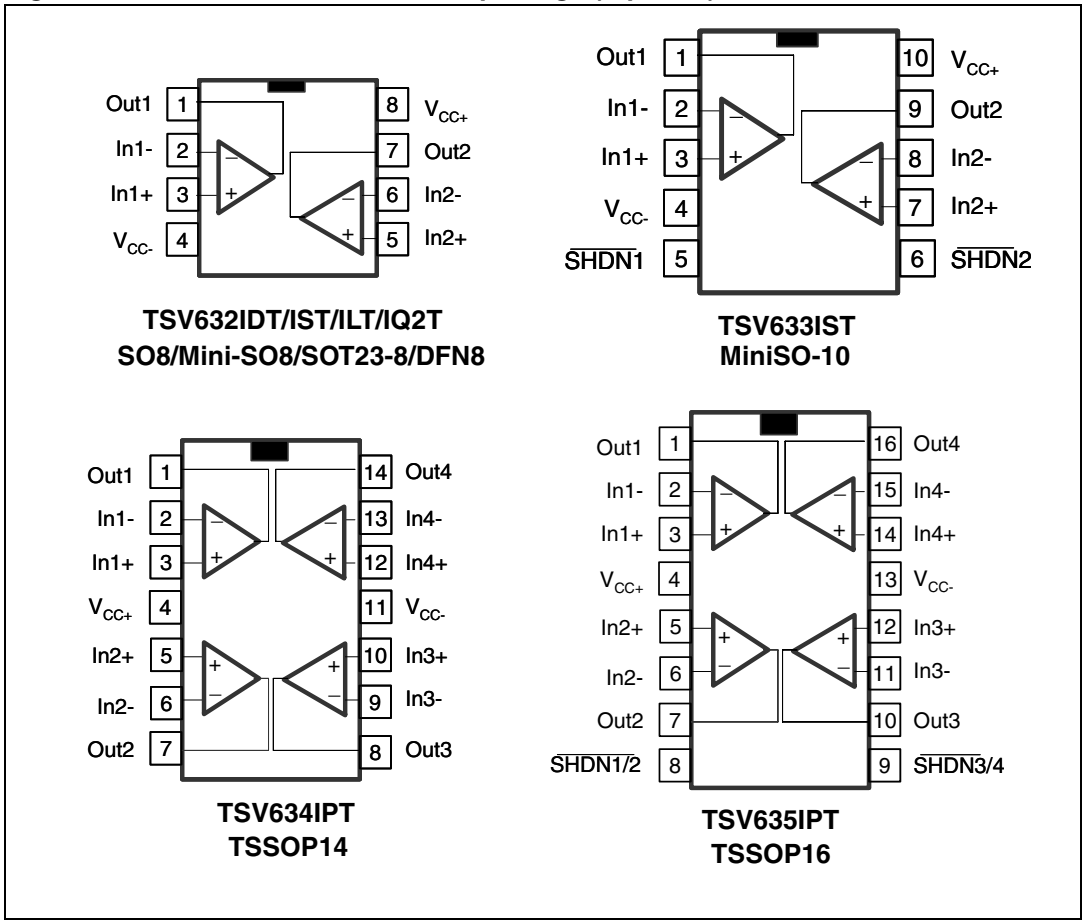
Table 1. Device summary

Reference	Dual version		Quad version	
	Without standby	With standby	Without standby	With standby
TSV63x	TSV632	TSV633	TSV634	TSV635
TSV63xA	TSV632A	TSV633A	TSV634A	TSV635A

Contents

1 Package pin connections

Figure 1. Pin connections for each package (top view)



2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	6	V
V_{id}	Differential input voltage (2)	$\pm V_{CC}$	V
V_{in}	Input voltage (3)	V_{CC-} - 0.2 to V_{CC+} + 0.2	V
I_{in}	Input current (4)	10	mA
$\overline{SHDN}$	Shutdown voltage(3)	V_{CC-} - 0.2 to V_{CC+} + 0.2	V
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(5)(6) DFN8 2x2 SOT23-8 MiniSO-8 SO-8 MiniSO-10 TSSOP14 TSSOP16	 57 105 190 125 113 100 95	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(7)	4	kV
	MM: machine model(8)	300	V
	CDM: charged device model(9)	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC}-V_{in} must not exceed 6 V, V_{in} must not exceed 6V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common mode input voltage range	V_{CC-} - 0.1 to V_{CC+} + 0.1	V
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 4. Electrical characteristics at V_{CC+} = +1.8 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25° C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV63x TSV63xA TSV633AIST - MiniSO10			3 0.8 1	mV
		$T_{min} < T_{op} < T_{max}$ - TSV63x $T_{min} < T_{op} < T_{max}$ - TSV63xA $T_{min} < T_{op} < T_{max}$ - TSV633AIST			4.5 2 2.2	mV
DV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	(V_{out} = V_{CC}/2)		1	10(1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
I_{ib}	Input bias current	(V_{out} = V_{CC}/2)		1	10(1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 1.8 V, V_{out} = 0.9 V	53	74		dB
		$T_{min} < T_{op} < T_{max}$	51			dB
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 0.5 V to 1.3 V	85	95		dB
		$T_{min} < T_{op} < T_{max}$	80			dB
V_{OH}	High level output voltage	R_L = 10 kΩ $T_{min} < T_{op} < T_{max}$	35 50	5		mV
V_{OL}	Low level output voltage	R_L = 10 kΩ $T_{min} < T_{op} < T_{max}$		4	35 50	mV
I_{out}	I_{sink}	V_o = 1.8 V	6	12		mA
		$T_{min} < T_{op} < T_{max}$	4			
	I_{source}	V_o = 0 V	6	10		mA
		$T_{min} < T_{op} < T_{max}$	4			
I_{CC}	Supply current (per operator)	No load, V_{out} = V_{CC}/2	40	50	60	µA
		$T_{min} < T_{op} < T_{max}$			62	µA
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz	700	790		kHz
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		45		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		13		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, Av = 1	0.2	0.27		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz f = 10 kHz		60 33		$\frac{nV}{\sqrt{Hz}}$

1. Guaranteed by design.

Table 5. Shutdown characteristics V_{CC} = 1.8 V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
I_{CC}	Supply current in shutdown mode (all operators)	$\overline{SHDN}$ = V_{CC-}		2.5	50	nA
		$T_{min} < T_{op} < 85°$ C			200	nA
		$T_{min} < T_{op} < 125°$ C			1.5	µA
t_{on}	Amplifier turn-on time	R_L= 2 kΩ, V_{out} = V_{CC-} to V_{CC-}+0.2 V		200		ns
t_{off}	Amplifier turn-off time	R_L = 2 kΩ, V_{out} = V_{CC+} - 0.5 V to V_{CC+} - 0.7 V		20		ns
V_{IH}	$\overline{SHDN}$ logic high		1.35			V
V_{IL}	$\overline{SHDN}$ logic low				0.6	V
I_{IH}	$\overline{SHDN}$ current high	$\overline{SHDN}$ = V_{CC+}		10		pA
I_{IL}	$\overline{SHDN}$ current low	$\overline{SHDN}$ = V_{CC-}		10		pA
I_{OLeak}	Output leakage in shutdown mode	$\overline{SHDN}$ = V_{CC-}		50		pA
		$T_{min} < T_{op} < 125°$ C		1		nA

Table 6. V_{CC+} = +3.3 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25° C, R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV63x TSV63xA TSV633AIST - MiniSO10			3 0.8 1	mV
		$T_{min} < T_{op} < T_{max}$ - TSV63x $T_{min} < T_{op} < T_{max}$ - TSV63xA $T_{min} < T_{op} < T_{max}$ - TSV633AIST			4.5 2 2.2	mV
DV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	$V_{out} = V_{CC}/2$		1	10(1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
I_{ib}	Input bias current	$V_{out} = V_{CC}/2$		1	10(1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 3.3 V, V_{out} = 1.65 V	57	79		dB
		$T_{min} < T_{op} < T_{max}$	53			
A_{vd}	Large signal voltage gain	R_L = 10 kΩ, V_{out} = 0.5 V to 2.8 V	88	98		dB
		$T_{min} < T_{op} < T_{max}$	83			
V_{OH}	High level output voltage	R_L = 10 kΩ $T_{mi.} < T_{op} < T_{max}$	35 50	5		mV
V_{OL}	Low level output voltage	R_L = 10 kΩ $T_{min} < T_{op} < T_{max}$		4	35 50	mV
I_{out}	I_{sink}	V_o = 3.3 V	23	45		mA
		$T_{min} < T_{op} < T_{max}$	20			
	I_{source}	V_o = 0 V	23	38		mA
		$T_{min} < T_{op} < T_{max}$	20			
I_{CC}	Supply current (per operator)	No load, V_{out} = 1.75 V	43	55	64	µA
		$T_{min} < T_{op} < T_{max}$			66	µA
AC performance						
GBP	Gain bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz	710	860		kHz
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		46		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		13		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, A_V = 1	0.22	0.29		V/µs

1. Guaranteed by design.

Table 7. Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25° C, and R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltages	TSV63x TSV63xA TSV633AIST - MiniSO10			3 0.8 1	mV
		$T_{min} < T_{op} < T_{max}$ - TSV63x $T_{min} < T_{op} < T_{max}$ - TSV63xA $T_{min} < T_{op} < T_{max}$ - TSV633AIST			4.5 2 2.2	mV
DV_{io}	Input offset voltage drift			2		µV/°C
I_{io}	Input offset current	(V_{out} = V_{CC}/2)		1	10(1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
I_{ib}	Input bias current	(V_{out} = V_{CC}/2)		1	10(1)	pA
		$T_{min} < T_{op} < T_{max}$		1	100	pA
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	0 V to 5 V, V_{out} = 2.5 V	60	80		dB
		$T_{min} < T_{op} < T_{max}$	55			dB
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 1.8 to 5 V	75	102		dB
		$T_{min} < T_{op} < T_{max}$	73			
A_{vd}	Large signal voltage gain	R_L= 10 kΩ, V_{out} = 0.5 V to 4.5 V	89	98		dB
		$T_{min} < T_{op} < T_{max}$	84			dB
EMIRR	EMI rejection ratio EMIRR = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mV_{rms}, f = 400 MHz		61		dB
		V_{RF} = 100 mV_{rms}, f = 900 MHz		85		
		V_{RF} = 100 mV_{rms}, f =1800 MHz		92		
		V_{RF} = 100 mV_{rms}, f =2400 MHz		83		
V_{OH}	High level output voltage	R_L = 10 kΩ $T_{min} < T_{op} < T_{max}$	35 50	7		mV
V_{OL}	Low level output voltage	R_L = 10 kΩ $T_{min} < T_{op} < T_{max}$		6	35 50	mV
I_{out}	I_{sink}	V_o = 5 V	40	69		mA
		$T_{min} < T_{op} < T_{max}$	35			
	I_{source}	V_o = 0 V	40	74		mA
		$T_{min} < T_{op} < T_{max}$	35			
I_{CC}	Supply current (per operator)	No load, V_{out}=V_{CC}/2	50	60	69	µA
		$T_{min} < T_{op} < T_{max}$			72	µA
AC performance						
GBP	Gain bandwidth product	R_L= 2 kΩ, C_L = 100 pF, f = 100 kHz	730	880		kHz
F_u	Unity gain frequency	R_L = 2 kΩ, C_L = 100 pF,		830		kHz

Table 7. Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T_{amb} = 25° C, and R_L connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ϕm	Phase margin	R_L = 2 kΩ, C_L = 100 pF		48		Degrees
G_m	Gain margin	R_L = 2 kΩ, C_L = 100 pF		13		dB
SR	Slew rate	R_L = 2 kΩ, C_L = 100 pF, Av=1	0.25	0.34		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz f = 10 kHz		60 33		$\frac{nV}{\sqrt{Hz}}$
THD+e_n	Total harmonic distortion + noise	V_{CC} = 5V, f = 1kHz, A_V = 1, R_L = 100kΩ, V_{icm} = V_{CC}/2, V_{out} = $2V_{PP}$		0.002		%

1. Guaranteed by design.

Table 8. Shutdown characteristics at V_{CC} = 5 V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
I_{CC}	Supply current in shutdown mode (all operators)	$\overline{SHDN}$ = V_{CC-}		5	50	nA
		T_{min} < T_{op} < 85° C			200	nA
		T_{min} < T_{op} < 125° C			1.5	µA
t_{on}	Amplifier turn-on time	R_L = 2 kΩ, V_{out} = V_{CC-} V to V_{CC-}+0.2 V		200		ns
t_{off}	Amplifier turn-off time	R_L = 2 kΩ, V_{out} = V_{CC+} - 0.5 V to V_{CC+} - 0.7 V		20		ns
V_{IH}	$\overline{SHDN}$ logic high		2			V
V_{IL}	$\overline{SHDN}$ logic low				0.8	V
I_{IH}	$\overline{SHDN}$ current high	$\overline{SHDN}$ = V_{CC+}		10		pA
I_{IL}	$\overline{SHDN}$ current low	$\overline{SHDN}$ = V_{CC-}		10		pA
I_{OLeak}	Output leakage in shutdown mode	$\overline{SHDN}$ = V_{CC-}		50		pA
		T_{min} < T_{op} < 125° C		1		nA

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

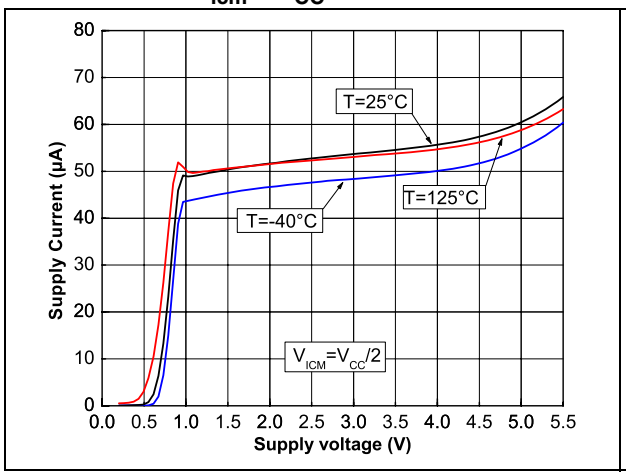


Figure 3. Output current vs. output voltage at V_{CC} = 1.5 V

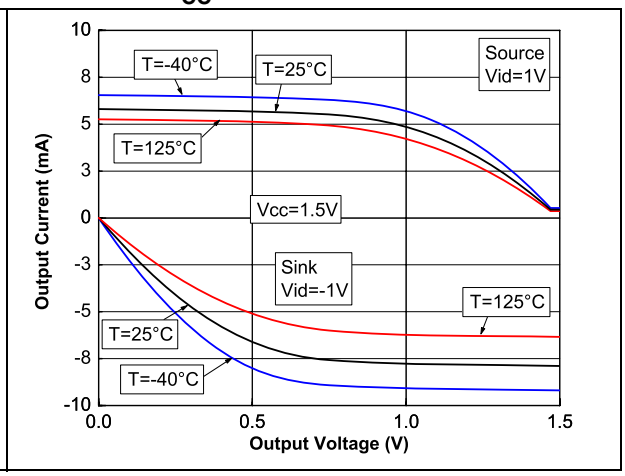


Figure 4. Output current vs. output voltage at V_{CC} = 5 V

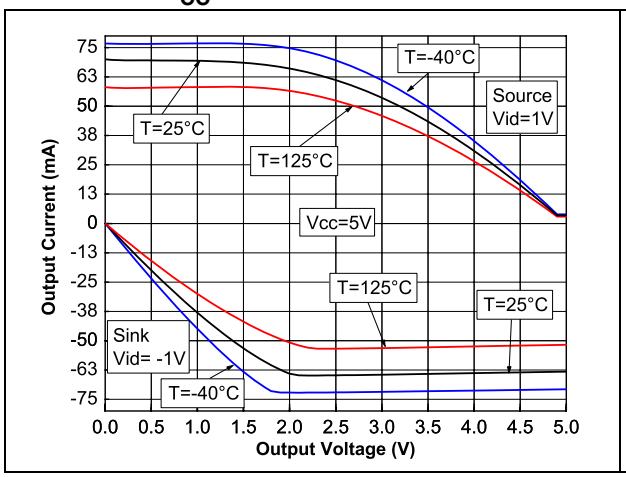


Figure 5. Voltage gain and phase vs. frequency at V_{CC} = 1.5 V

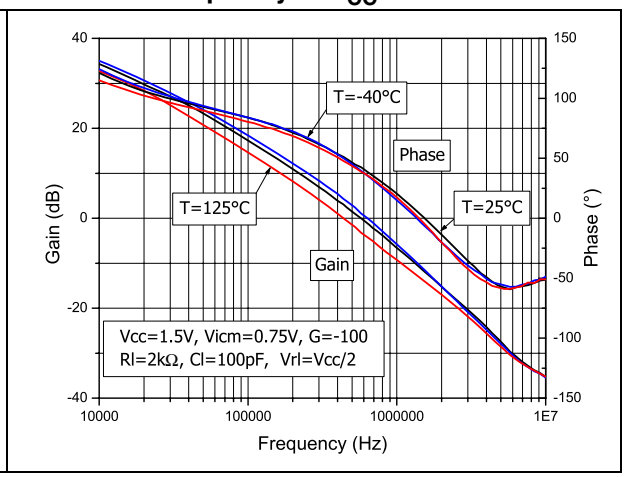


Figure 6. Voltage gain and phase vs. frequency at V_{CC} = 5 V

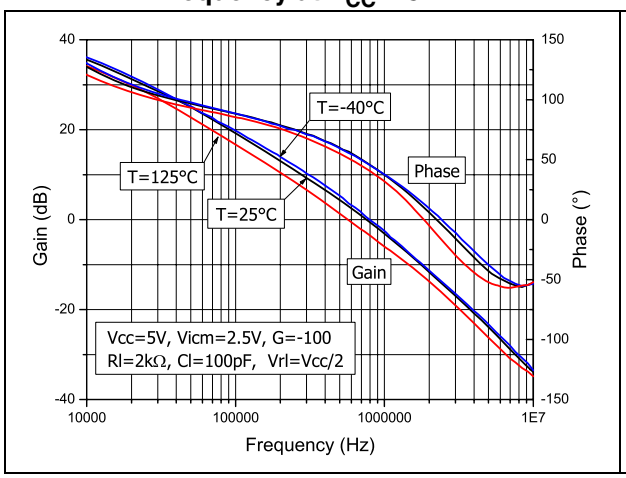


Figure 7. Phase margin vs. output current at V_{CC} = 5 V

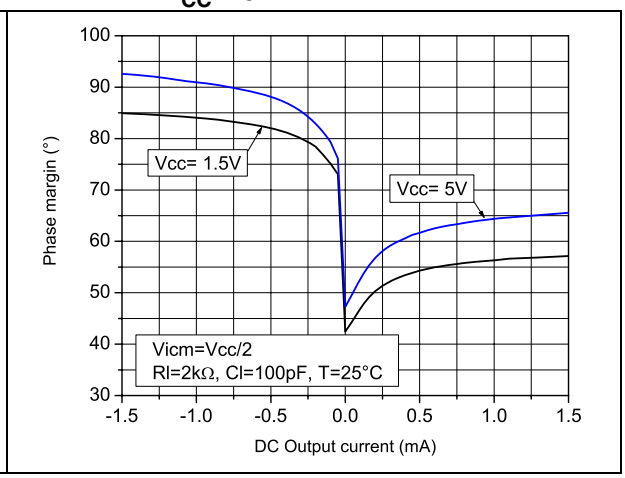


Figure 8. Positive slew rate vs. time

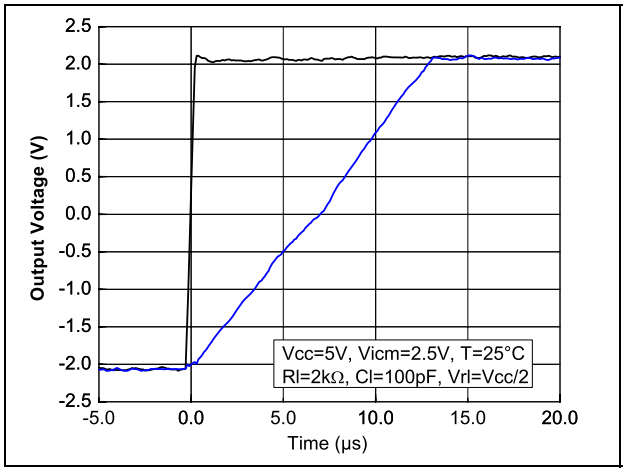


Figure 9. Negative slew rate vs. time

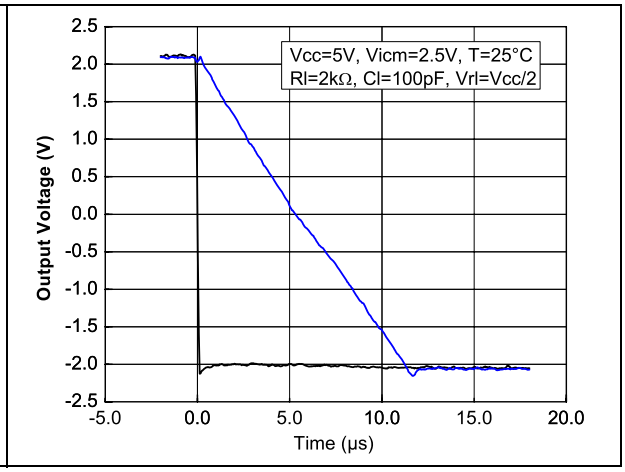


Figure 10. Positive slew rate vs. supply voltage

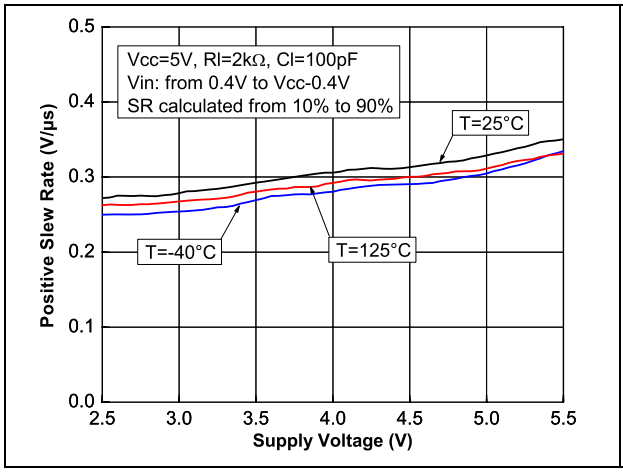


Figure 11. Negative slew rate vs. supply voltage

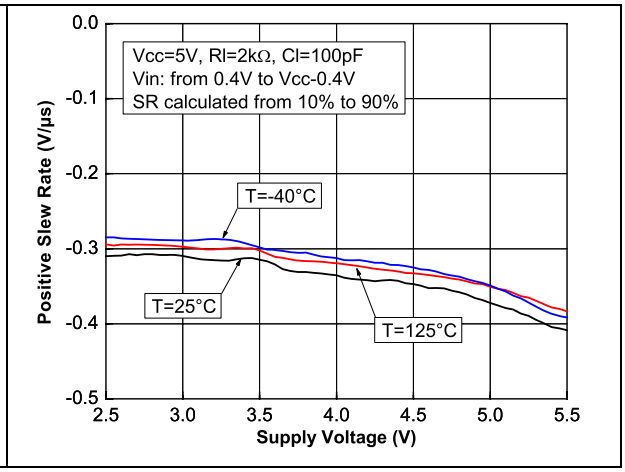


Figure 12. Distortion + noise vs. output voltage

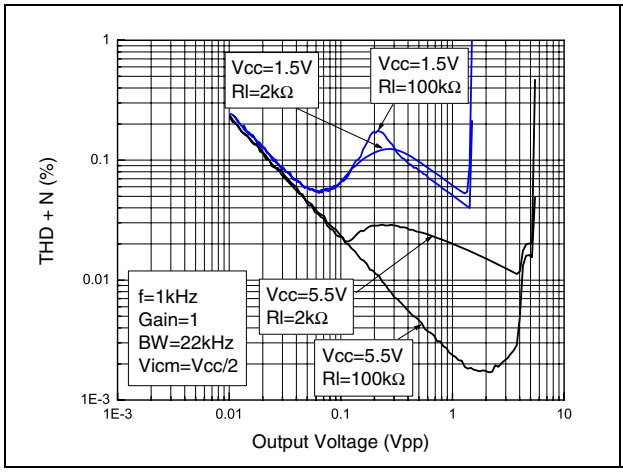


Figure 13. Distortion + noise vs. frequency

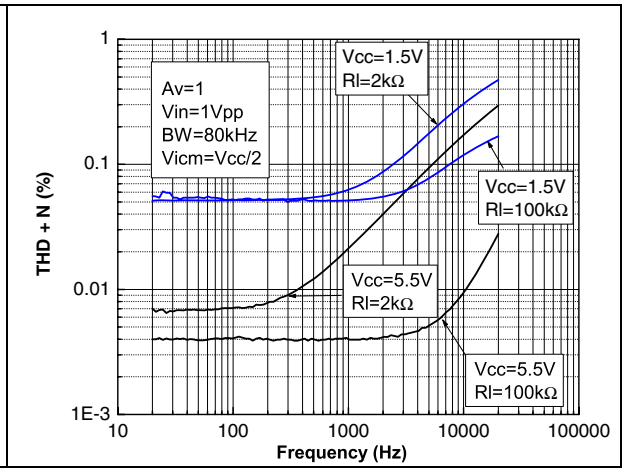


Figure 14. Noise vs. frequency

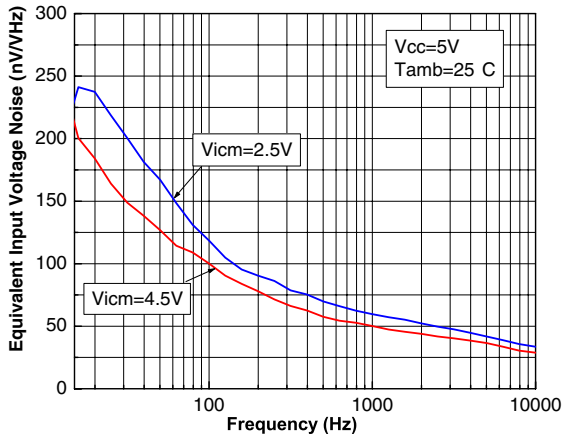
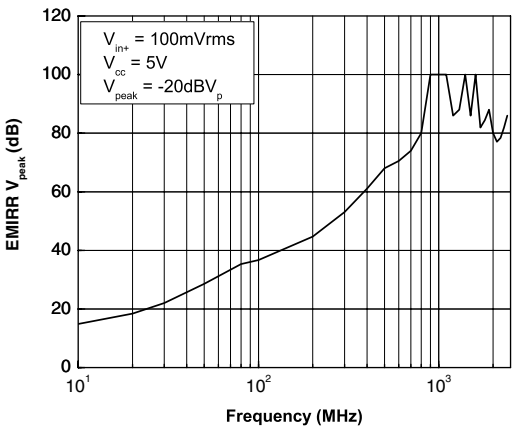


Figure 15. EMIRR vs. frequency at Vcc = 5 V, T = 25° C



4 Application information

4.1 Operating voltages

The TSV63x can operate from 1.5 to 5.5 V. Their parameters are fully specified for 1.8-, 3.3- and 5-V power supplies. However, the parameters are very stable in the full V_{CC} range and several characterization curves show the TSV63x characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40° C to +125° C.

4.2 Rail-to-rail input

The TSV63x are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common mode range is extended from V_{CC-} - 0.1 V to V_{CC+} + 0.1 V. The transition between the two pairs appears at V_{CC+} - 0.7 V. In the transition region, the performance of CMRR, PSRR, V_{io} (*Figure 16* and *Figure 17*) and THD is slightly degraded.

Figure 16. Input offset voltage vs input common mode at V_{CC} = 1.5 V

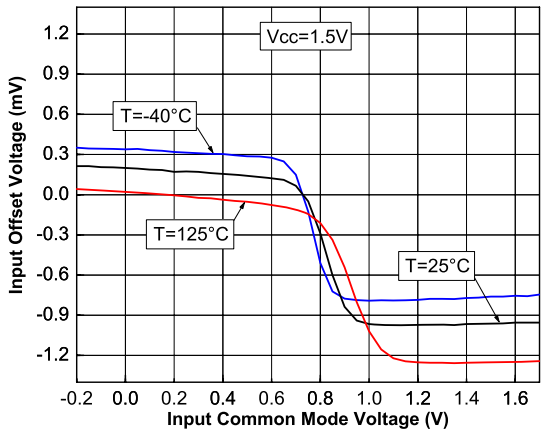
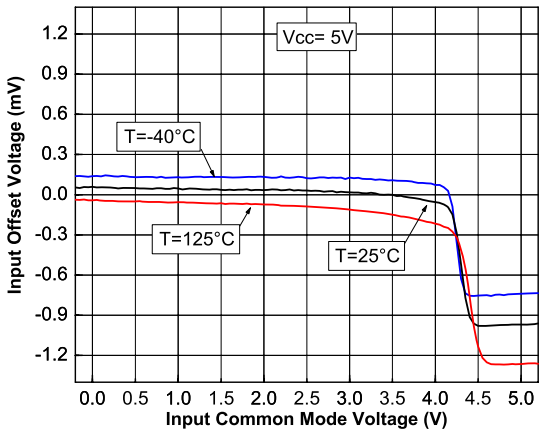


Figure 17. Input offset voltage vs input common mode at V_{CC} = 5 V



The devices are guaranteed without phase reversal.

4.3 Rail-to-rail output

The operational amplifiers' output levels can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

4.4 Shutdown function (TSV633 - TSV635)

The operational amplifiers are enabled when the $\overline{SHDN}$ pin is pulled high. To disable the amplifiers, the $\overline{SHDN}$ must be pulled down to V_{CC-}. When in shutdown mode, the amplifiers' output is in a high impedance state. The $\overline{SHDN}$ pin must never be left floating, but tied to V_{CC+} or V_{CC-}.

The turn-on and turn-off times are calculated for an output variation of ±200 mV (*Figure 18* and *Figure 19* show the test configurations).

Figure 18. Test configuration for turn-on time (Vout pulled down)

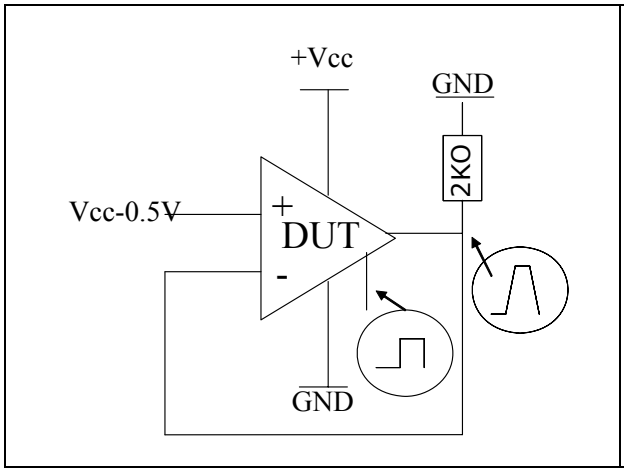


Figure 19. Test configuration for turn-off time (Vout pulled down)

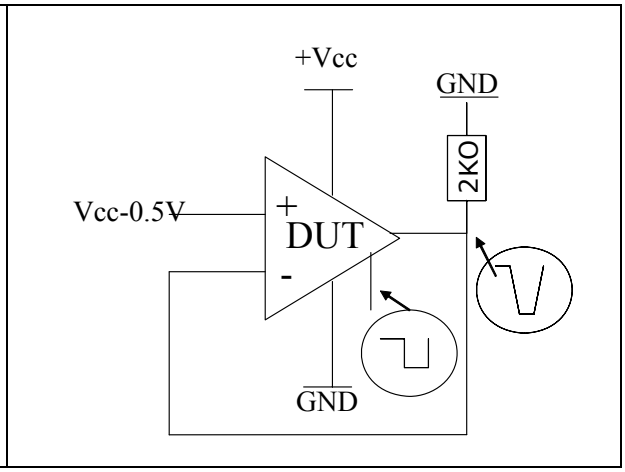


Figure 20. Turn-on time, V_{CC} = 5 V, Vout pulled down, T = 25° C

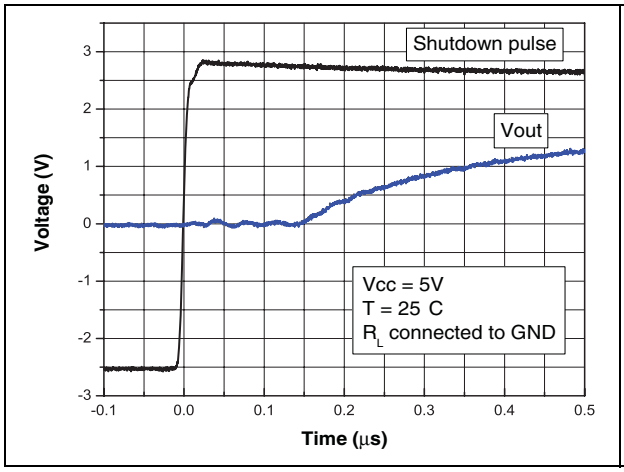
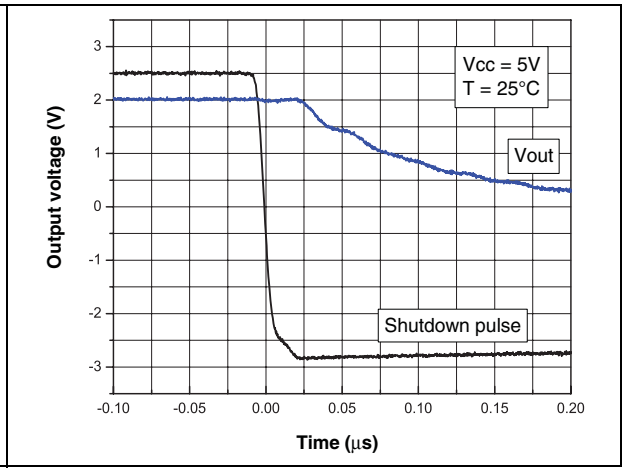


Figure 21. Turn-off time, V_{CC} = 5 V, Vout pulled down, T = 25° C



4.5 Optimization of DC and AC parameters

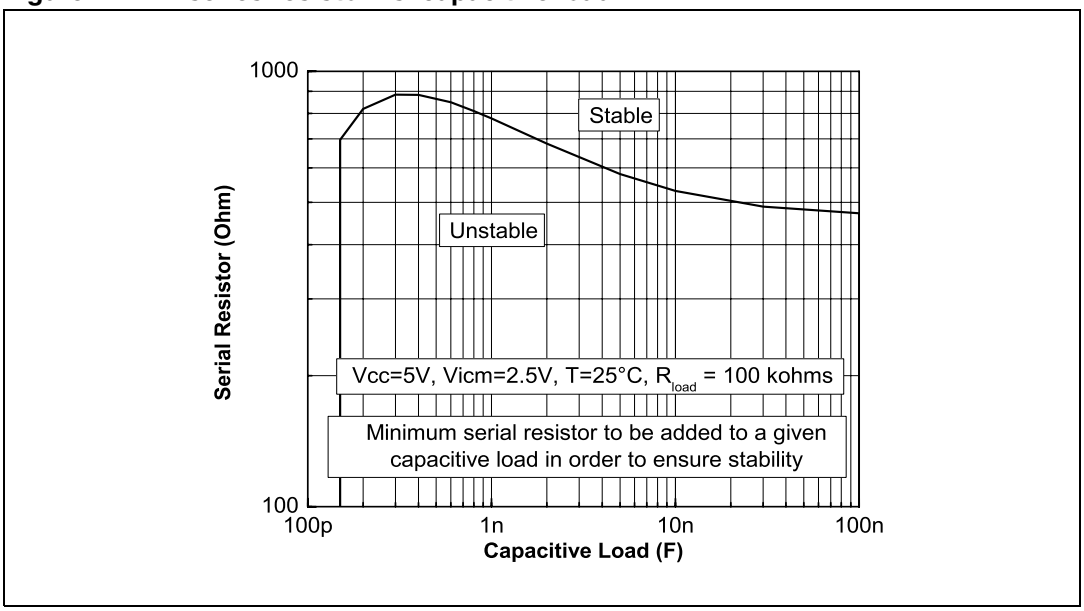
These devices use an innovative approach to reduce the spread of the main DC and AC parameters. An internal adjustment achieves a very narrow spread of the current consumption (60 µA typical, min/max at ±17 %). Parameters linked to the current consumption value, such as GBP, SR and AVd, benefit from this narrow dispersion. All parts present a similar speed and the same behavior in terms of stability. In addition, the minimum values of GBP and SR are guaranteed (GBP = 730 kHz minimum and SR = 0.25 V/µs minimum).

4.6 Driving resistive and capacitive loads

These products are micro-power, low-voltage operational amplifiers optimized to drive rather large resistive loads, above 2 kΩ For lower resistive loads, the THD level may significantly increase.

In a *follower* configuration, these operational amplifiers can drive capacitive loads up to 100 pF with no oscillations. When driving larger capacitive loads, adding an in-series resistor at the output can improve the stability of the devices (see *Figure 22* for recommended in-series resistor values). Once the in-series resistor value has been selected, the stability of the circuit should be tested on bench and simulated with the simulation model.

Figure 22. In-series resistor vs. capacitive load



4.7 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

4.8 Macromodel

Two accurate macromodels (with or without shutdown feature) of the TSV63x is available on STMicroelectronics' web site at www.st.com. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV63x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It also helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

5.1 DFN8 2x2 package information

Figure 23. DFN8 2x2 mm package mechanical drawing

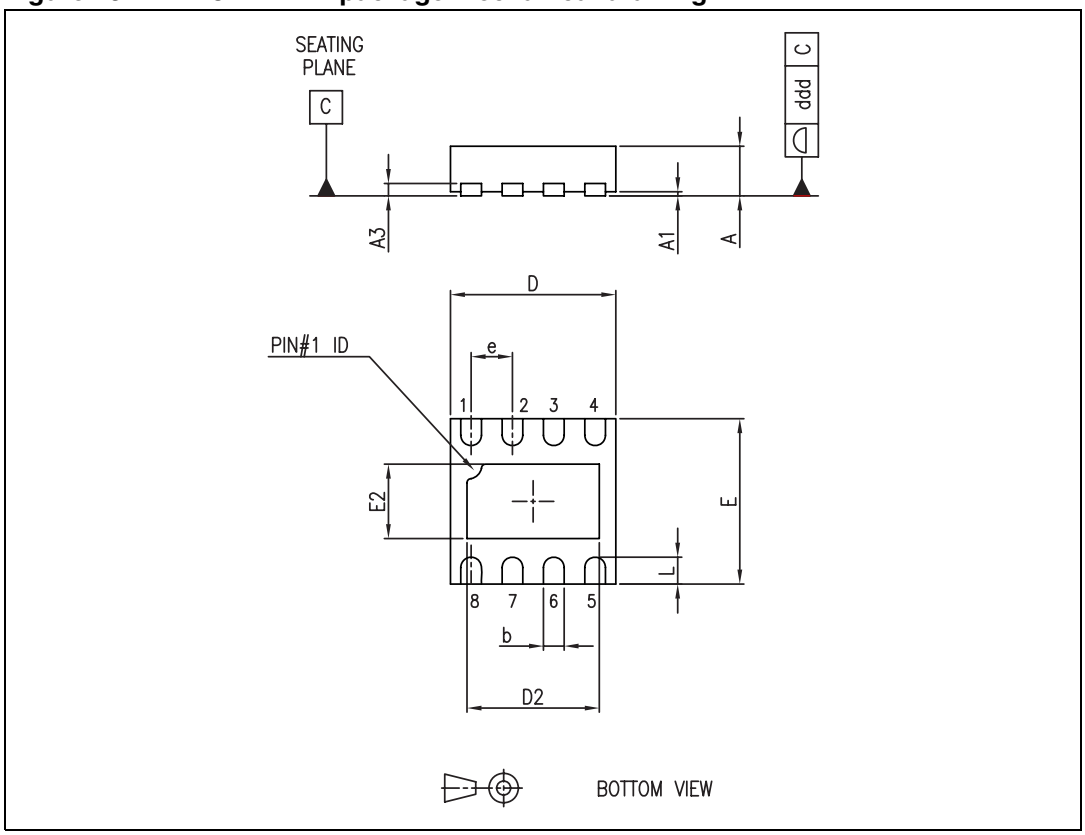
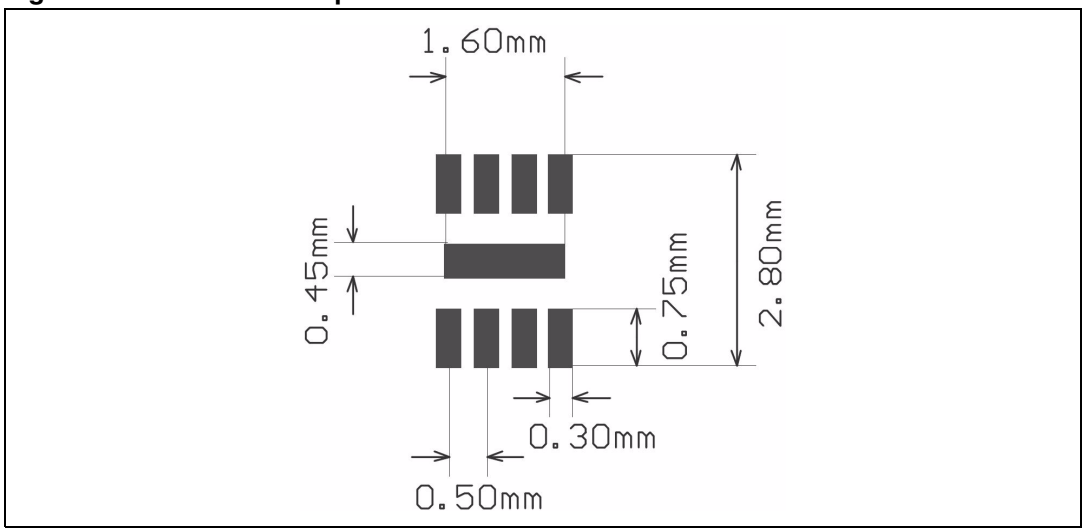


Table 9. DFN8 2 x 2 mm package mechanical data (pitch 0.5 mm)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.040
e		0.50			0.020	
L			0.50			0.020
ddd			0.08			0.003

Figure 24. DFN8 2x2 footprint recommendation



5.2 SOT23-8 package information

Figure 25. SOT23-8 package mechanical drawing

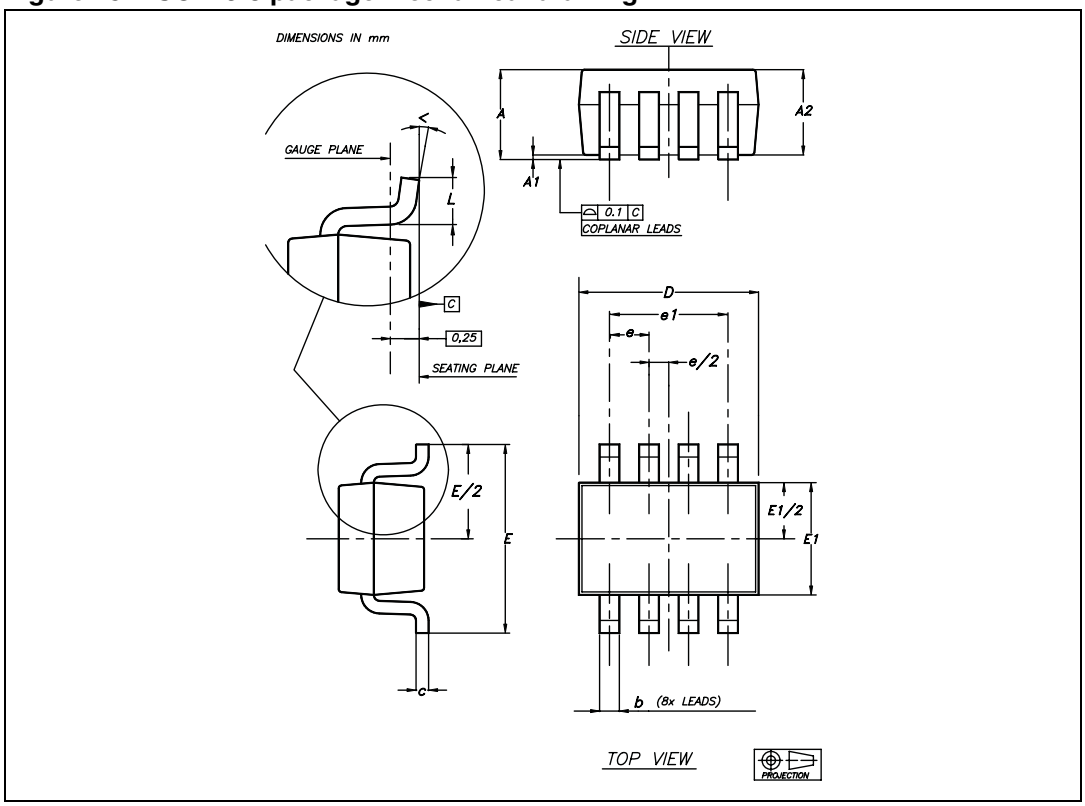


Table 10. SOT23-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1			0.15			0.006
A2	0.90		1.30	0.035		0.051
b	0.22		0.38	0.009		0.015
c	0.08		0.22	0.003		0.009
D	2.80		3	0.110		0.118
E	2.60		3	0.102		0.118
E1	1.50		1.75	0.059		0.069
e		0.65			0.026	
e1		1.95			0.077	
L	0.30		0.60	0.012		0.024
<	0°		8°			

5.3 SO-8 package information

Figure 26. SO-8 package mechanical drawing

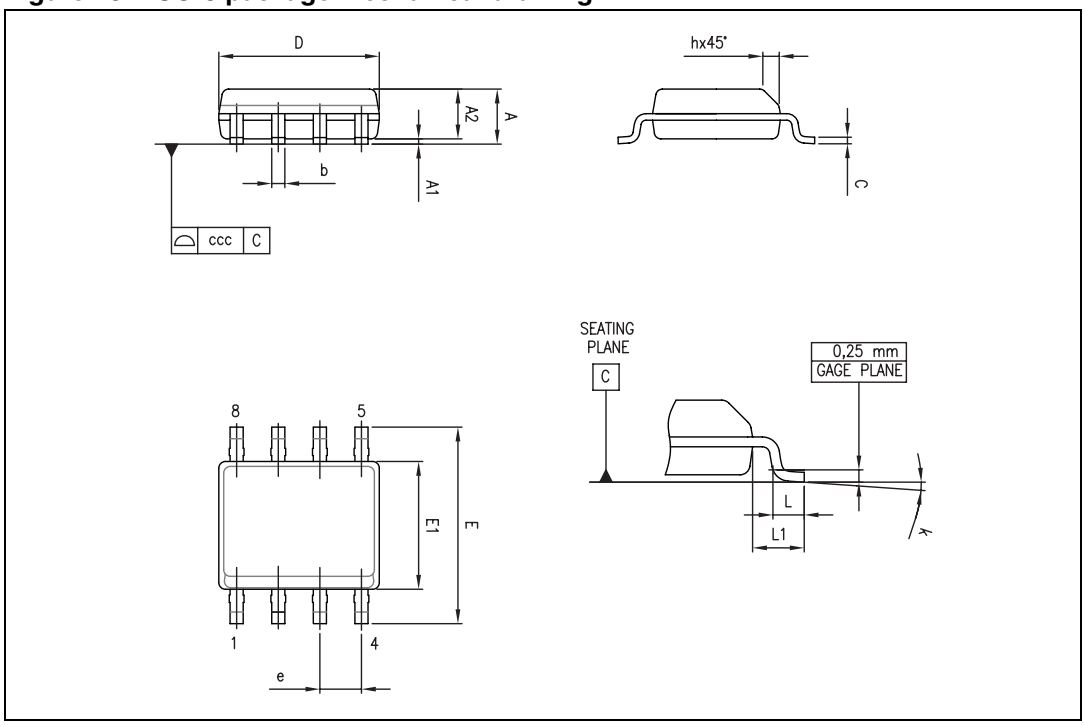


Table 11. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0		8°	1°		8°
ccc			0.10			0.004

5.4 MiniSO-8 package information

Figure 27. MiniSO-8 package mechanical drawing

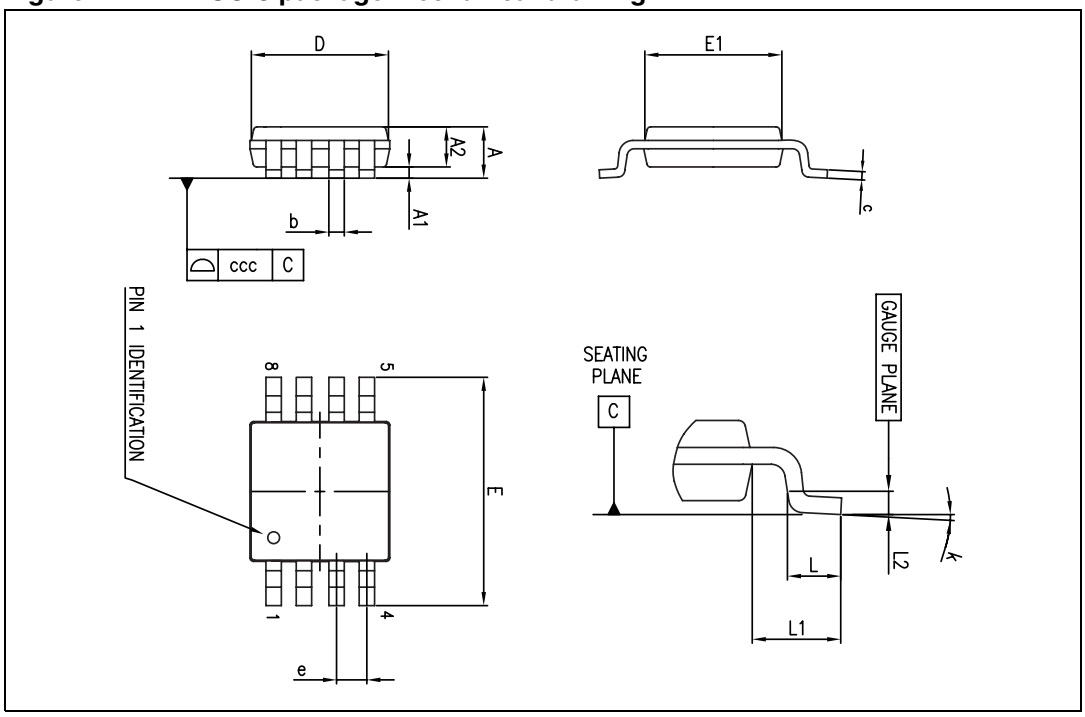


Table 12. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

5.5 MiniSO-10 package information

Figure 28. MiniSO-10 package mechanical drawing

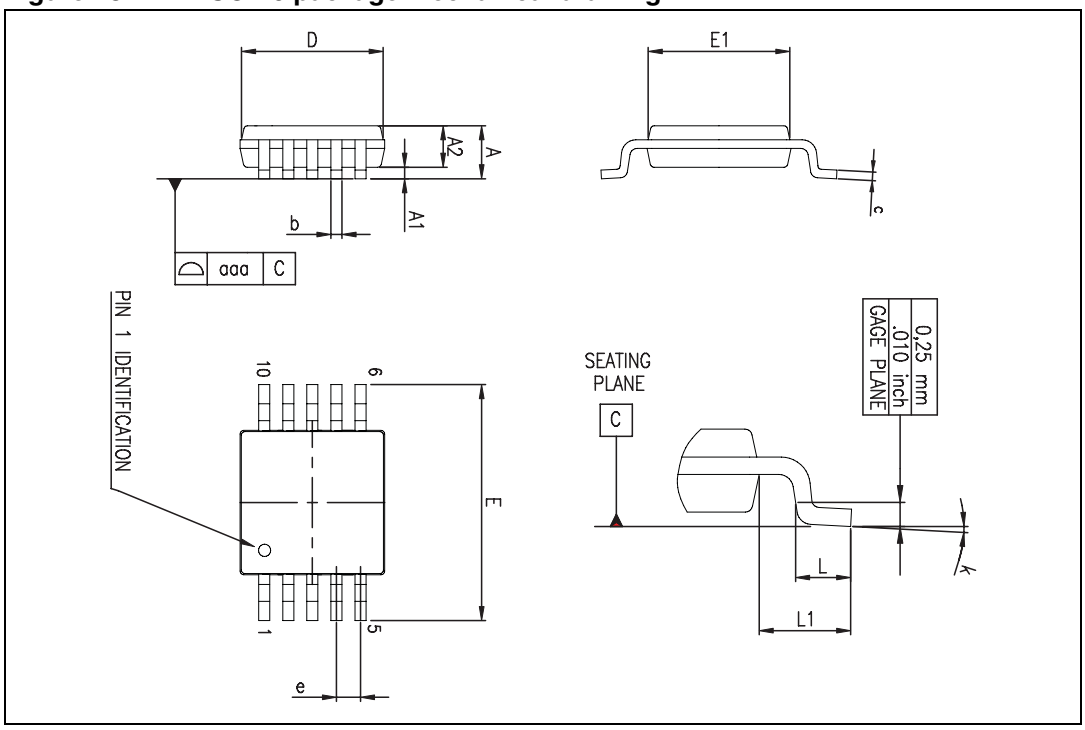


Table 13. MiniSO-10 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.10			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.15	0.23	0.30	0.006	0.009	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.50			0.020	
L	0.40	0.55	0.70	0.016	0.022	0.028
L1		0.95			0.037	
k	0°	3°	6°	0°	3°	6°
aaa			0.10			0.004

5.6 TSSOP14 package information

Figure 29. TSSOP14 package mechanical drawing

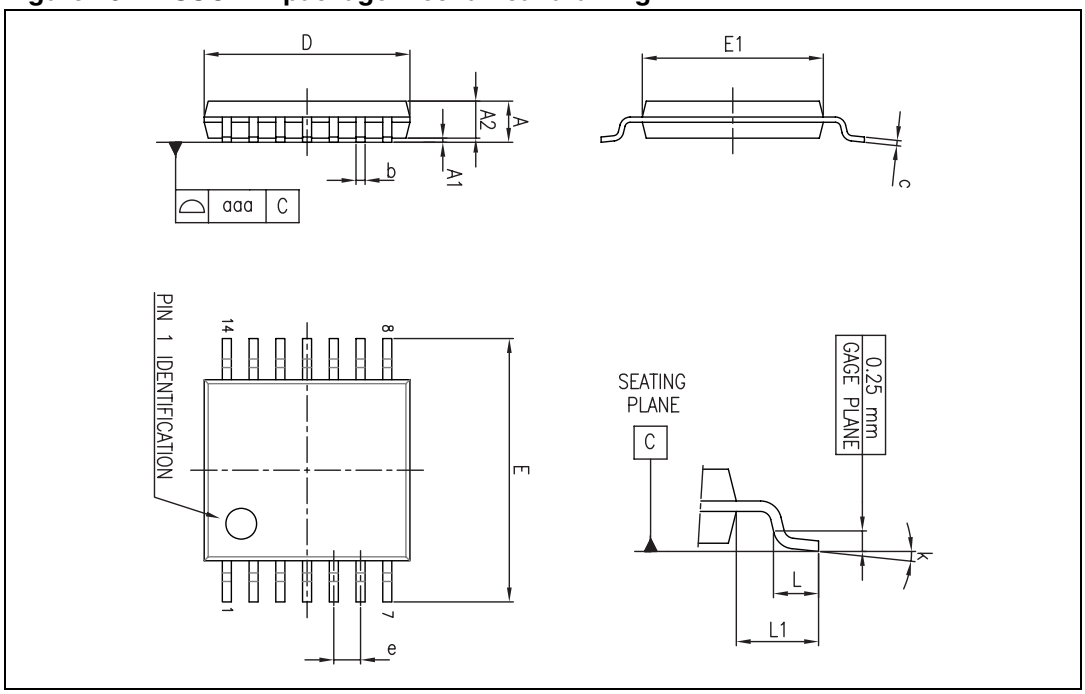


Table 14. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

5.7 TSSOP16 package information

Figure 30. TSSOP16 package mechanical drawing

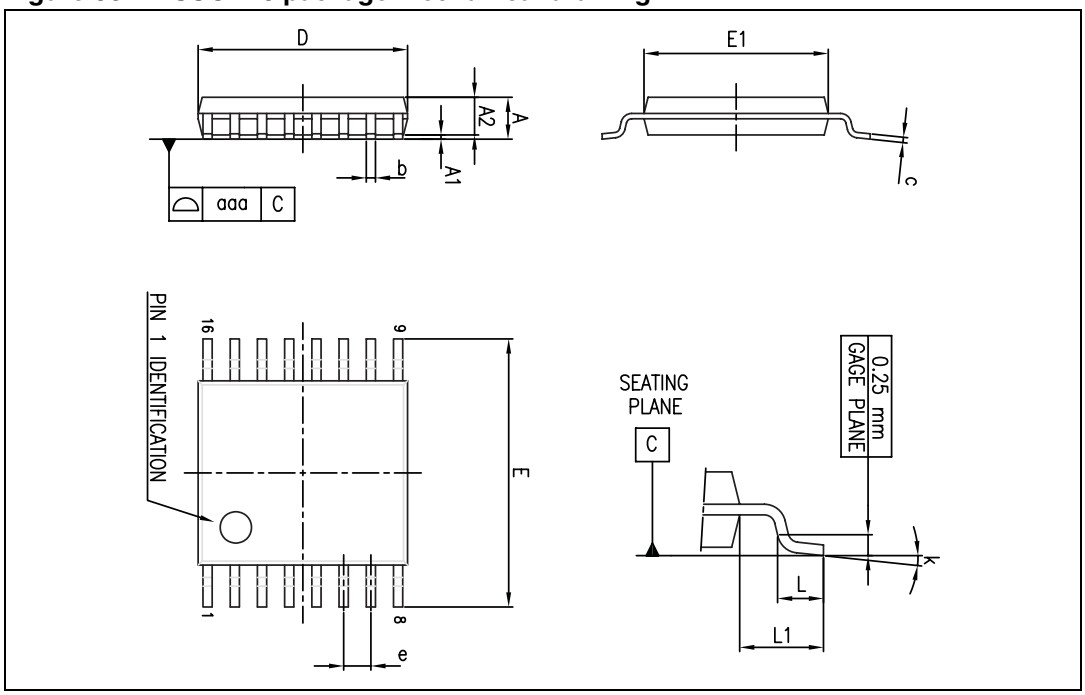


Table 15. TSSOP16 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
aaa			0.10			0.004

6 Ordering information

Table 16. Order codes

Order code	Temperature range	Package	Packing	Marking
TSV632IQ2T	-40° C to +125° C	DFN8 2x2	Tape & reel	K1N
TSV632ID/DT		SO-8	Tube and tape & reel	TSV632
TSV632AID/DT				TV632A
TSV632IST		MiniSO-8	Tape & reel	K110
TSV632AIST				K145
TSV632ILT		SOT23-8	Tape & reel	K110
TSV632AILT				K145
TSV633IST		MiniSO-10	Tape & reel	K111
TSV633AIST				K146
TSV634IPT		TSSOP-14	Tape & reel	TSV634
TSV634AIPT				TSV634A
TSV635IPT		TSSOP-16	Tape & reel	TSV635
TSV635AIPT				TSV635A

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
25-May-2009	1	Initial release.
15-Jun-2009	2	Corrected pin connection diagram in *Figure 1*.
03-Sep-2009	3	Added root part numbers (TSv63xA) and *Table 1: Device summary* on cover page. Added order code TSV632AILT in *Table 16: Order codes*.
07-Nov-2011	4	*Chapter 5*: added DFN8 2x2 package mechanical drawing. Added ordering information for DFN package to *Table 16: Order codes*. Corrected unit on Y axis of *Figure 16* and *Figure 17*.

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