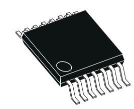
TS615

DUAL WIDE BAND OPERATIONAL AMPLIFIER WITH HIGH OUTPUT CURRENT

- **LOW NOISE :** 2.5nV/√Hz
- **HIGH OUTPUT CURRENT :** 420mA
- **VERY LOW HARMONIC AND INTERMODULATION DISTORTION**
- **HIGH SLEW RATE :** 410V/µs
- **-3dB BANDWIDTH :** 40MHz@gain=12dB on 25Ω load single ended.
- **21.2Vp-p DIFFERENTIAL OUTPUT SWING** on 50Ω load, 12V power supply
- **CURRENT FEEDBACK STRUCTURE**
- **5V to 12V POWER SUPPLY**
- **SPECIFIED FOR 20Ω and 50Ω DIFFERENTIAL LOAD**
- **POWER DOWN FUNCTION WITH A SHORT CIRCUITED OUTPUT** to keep the matching with the line in sleep mode



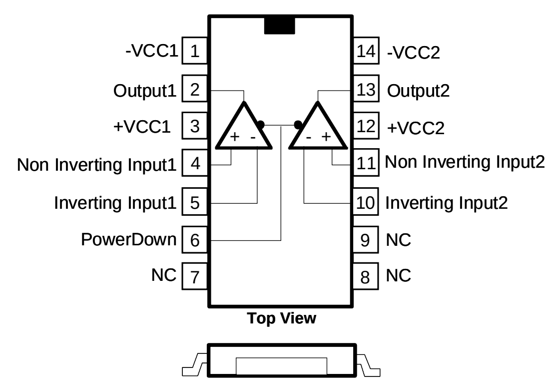
P
TSSOP14 Exposed-Pad
(Plastic Micro package)

ORDER CODE

Part Number	Temperature Range	Package
TS615IPWT	-40, +85°C	PW

PW= Thin Shrink Small Outline Package with Exposed-Pad (TSSOP Exposed-Pad) only available in Tape & Reel (PWT)

PIN CONNECTIONS (top view)



Cross Section View Showing Exposed-Pad
This pad can be connected to a (-Vcc) copper area on the PCB

DESCRIPTION

The TS615 is a dual operational amplifier featuring a high output current 410mA. These drivers can be configured differentially for driving signals in telecommunication systems using multiple carriers. The TS615 is ideally suited for xDSL (High Speed Asymmetrical Digital Subscriber Line) applications. This circuit is capable of driving a 10Ω or 25Ω load at ±2.5V, 5V, ±6V or +12V power supply. The TS615 will be able to reach a -3dB bandwidth of 40MHz on 25Ω load with a 12dB gain. This device is designed for the high slew rates to support low harmonic distortion and intermodulation. The TS615 is fitted out with Power Down function to decrease the consumption. During this sleep state the device displays a short circuit output in order to keep the impedance matching with the line. The TS615 is housed in TSSOP14 Exposed-Pad plastic package for a very low thermal resistance.

APPLICATION

- Line driver for xDSL
- Multiple Video Line Driver

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	±7	V
V_{id}	Differential Input Voltage [2]	±2	V
V_{in}	Input Voltage Range [3]	±6	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{std}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thjc}	Thermal Resistance Junction to Case	4	°C/W
R_{thja}	Thermal Resistance Junction to Ambient Area	40	°C/W
$P_{max.}$	Maximum Power Dissipation (@25°C)	3.1	W
ESD except pins 4, 5, 10, 11	CDM : Charged Device Model HBM : Human Body Model MM : Machine Model	1.5 2 200	kV kV V
ESD only pins 4, 5, 10, 11	CDM : Charged Device Model HBM : Human Body Model MM : Machine Model	1 1 100	kV kV V
	Output Short Circuit	[4]	

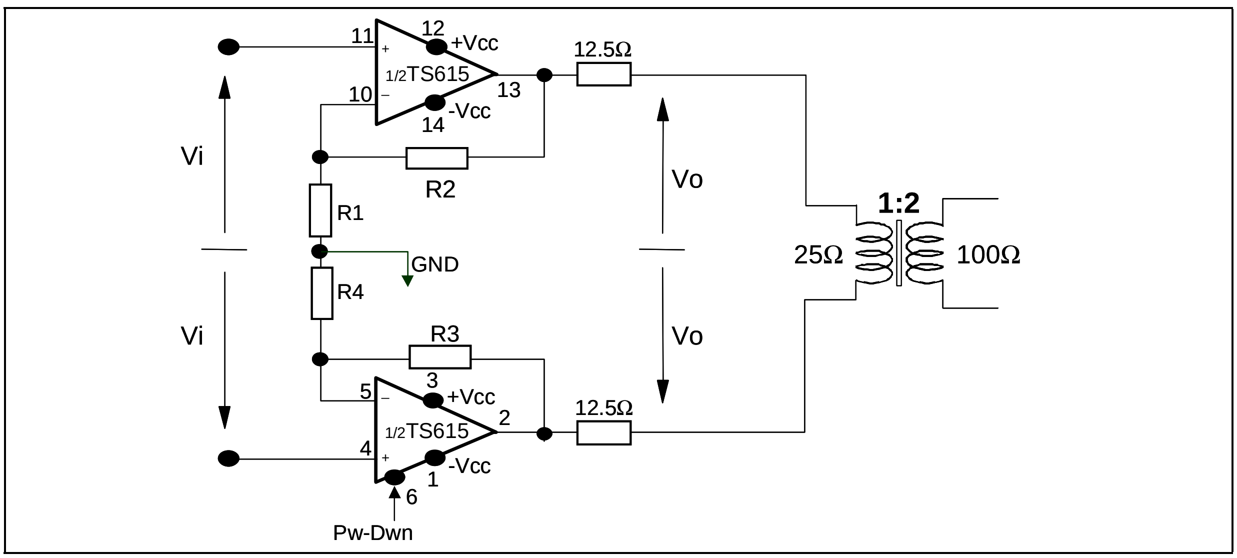
1. All voltage values, except differential voltage are with respect to network terminal.
2. Differential voltage are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltage must never exceed V_{CC} +0.3V.
4. An output current limitation protects the circuit from transient currents. Short-circuits can cause excessive heating. Destructive dissipation can result from short circuit on amplifiers.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	±2.5 to ±6	V
V_{icm}	Common Mode Input Voltage	$-V_{CC}$+1.5V to $+V_{CC}$-1.5V	V

TYPICAL APPLICATION:

Differential Line Driver for xDSL Applications



ELECTRICAL CHARACTERISTICS

V_{CC} = ±6Volts, R_{fb}=910Ω,T_{amb} = 25°C (unless otherwise specified)

Note: as described on page 24 (table 71), the TS615 requires a 620Ω feedback resistor for an optimised bandwidth with a gain of 12B for a 12V power supply. Nevertheless, due to production test constraints, the TS615 is tested with the same feedback resistor for 12V and 5V power supplies (910Ω).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC PERFORMANCE						
V_{io}	Input Offset Voltage	T_{amb}		1.25	3.5	mV
		$T_{min.} < T_{amb} < T_{max.}$		2.1		
ΔV_{io}	Differential Input Offset Voltage	T_{amb} = 25°C			2.5	mV
I_{ib+}	Positive Input Bias Current	T_{amb}		6	30	µA
		$T_{min.} < T_{amb} < T_{max.}$		7.8		
I_{ib-}	Negative Input Bias Current	T_{amb}		3	15	µA
		$T_{min.} < T_{amb} < T_{max.}$		3.2		
Z_{IN+}	Input(+) Impedance			82		kΩ
Z_{IN-}	Input(-) Impedance			54		Ω
C_{IN+}	Input(+) Capacitance			1		pF
CMR	Common Mode Rejection Ratio	ΔV_{ic} = ±4.5V	58	63		dB
	20 log ($\Delta V_{ic}/\Delta V_{io}$)	$T_{min.} < T_{amb} < T_{max.}$		61		
SVR	Supply Voltage Rejection Ratio	ΔV_{cc}=±2.5V to ±6V	72	79		dB
	20 log ($\Delta V_{cc}/\Delta V_{io}$)	$T_{min.} < T_{amb} < T_{max.}$		78		
I_{CC}	Total Supply Current per Operator	No load		14	17	mA
DYNAMIC PERFORMANCE and OUTPUT CHARACTERISTIC						
R_{OL}	Open Loop Transimpedance	V_{out} = 7Vp-p, R_L = 25Ω	5	21		MΩ
		$T_{min.} < T_{amb.} < T_{max.}$		8.9		
BW	-3dB Bandwidth	Small Signal V_{out}<20mVp A_V = 12dB, R_L = 25Ω	25	40		MHz
	Full Power Bandwidth	Large Signal V_{out}=3Vp A_V = 12dB, R_L = 25Ω		26		
	Gain Flatness @ 0.1dB	Small Signal V_{out}<20mVp A_V = 12dB, R_L = 25Ω		7		MHz
Tr	Rise Time	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω		10.6		ns
Tf	Fall Time	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω		12.2		ns
Ts	Settling Time	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω		50		ns
SR	Slew Rate	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω	330	410		V/µs
V_{OH}	High Level Output Voltage	R_L=25Ω Connected to GND	4.8	5.1		V
V_{OL}	Low Level Output Voltage	R_L=25Ω Connected to GND		-5.5	-5.2	V
I_{out}	Output Sink Current	V_{out} = -4Vp	-350	-530		mA
		$T_{min.} < T_{amb} < T_{max.}$		-440		
	Output Source Current	V_{out} = +4Vp	330	420		
		$T_{min.} < T_{amb} < T_{max.}$		365		

Note: as described on page 24 (table 71), the TS615 requires a 620Ω feedback resistor for an optimised bandwidth with a gain of 12B for a 12V power supply. Nevertheless, due to production test constraints, the TS615 is tested with the same feedback resistor for 12V and 5V power supplies (910Ω).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NOISE AND DISTORTION						
eN	Equivalent Input Noise Voltage	F = 100kHz		2.5		nV/√Hz
iNp	Equivalent Input Noise Current (+)	F = 100kHz		15		pA/√Hz
iNn	Equivalent Input Noise Current (-)	F = 100kHz		21		pA/√Hz
HD2	2nd Harmonic distortion (differential configuration)	V_{out} = 14Vp-p, A_V = 12dB F= 110kHz, R_L = 50Ω diff.		-87		dBc
HD3	3rd Harmonic distortion (differential configuration)	V_{out} = 14Vp-p, A_V = 12dB F= 110kHz, R_L = 50Ω diff.		-83		dBc
IM2	2nd Order Intermodulation Product (differential configuration)	F1= 100kHz, F2 = 110kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-76		dBc
		F1= 370kHz, F2 = 400kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-75		
IM3	3rd Order Intermodulation Product (differential configuration)	F1 = 100kHz, F2 = 110kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-88		dBc
		F1 = 370kHz, F2 = 400kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-87		

ELECTRICAL CHARACTERISTICS

V_{CC} = ±2.5Volts, R_{fb}=910Ω,T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC PERFORMANCE						
V_{io}	Input Offset Voltage	T_{amb}		0.5	2.5	mV
		$T_{min.} < T_{amb} < T_{max.}$		1.2		
ΔV_{io}	Differential Input Offset Voltage	T_{amb} = 25°C			2.5	mV
I_{ib+}	Positive Input Bias Current	T_{amb}		5	30	µA
		$T_{min.} < T_{amb} < T_{max.}$		8		
I_{ib-}	Negative Input Bias Current	T_{amb}		0.8	11	µA
		$T_{min.} < T_{amb} < T_{max.}$		1.24		
Z_{IN+}	Input(+) Impedance			71		kΩ
Z_{IN-}	Input(-) Impedance			62		Ω
C_{IN+}	Input(+) Capacitance			1.5		pF
CMR	Common Mode Rejection Ratio	ΔV_{ic} = ±1V	55	60		dB
	20 log ($\Delta V_{ic}/\Delta V_{io}$)	$T_{min.} < T_{amb.} < T_{max.}$		58		
SVR	Supply Voltage Rejection Ratio	ΔV_{cc}=±2V to ±2.5V	63	77		dB
	20 log ($\Delta V_{cc}/\Delta V_{io}$)	$T_{min.} < T_{amb.} < T_{max.}$		76		
I_{CC}	Total Supply Current per Operator	No load		11.9	15	mA
DYNAMIC PERFORMANCE and OUTPUT CHARACTERISTICS						
R_{OL}	Open Loop Transimpedance	V_{out} = 2Vp-p, R_L = 10Ω	2	5.4		MΩ
		$T_{min.} < T_{amb.} < T_{max.}$		2.1		
BW	-3dB Bandwidth	Small Signal V_{out}<20mVp A_V = 12dB, R_L = 10Ω	20	30		MHz
	Full Power Bandwidth	Large Signal V_{out} = 1.4Vp A_V = 12dB, R_L = 10Ω		20		
	Gain Flatness @ 0.1dB	Small Signal V_{out}<20mVp A_V = 12dB, R_L = 10Ω		5.7		MHz
Tr	Rise Time	V_{out} = 2.8Vp-p, A_V = 12dB R_L = 10Ω		11		ns
Tf	Fall Time	V_{out} = 2.8Vp-p, A_V = 12dB R_L = 10Ω		11.5		ns
Ts	Settling Time	V_{out} = 2.2Vp-p, A_V = 12dB R_L = 10Ω		39		ns
SR	Slew Rate	V_{out} = 2.2Vp-p, A_V = 12dB R_L = 10Ω	100	130		V/µs
V_{OH}	High Level Output Voltage	R_L=10Ω Connected to GND	1.5	1.75		V
V_{OL}	Low Level Output Voltage	R_L=10Ω Connected to GND		-2.05	-1.8	V
I_{out}	Output Sink Current	V_{out} = -1.25Vp	-350	-470		mA
		$T_{min.} < T_{amb} < T_{max.}$		-450		
	Output Source Current	V_{out} = +1.25Vp	200	270		
		$T_{min.} < T_{amb} < T_{max.}$		245		

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NOISE AND DISTORTION						
eN	Equivalent Input Noise Voltage	F = 100kHz		2.5		nV/√Hz
iNp	Equivalent Input Noise Current (+)	F = 100kHz		15		pA/√Hz
iNn	Equivalent Input Noise Current (-)	F = 100kHz		21		pA/√Hz
HD2	2nd Harmonic distortion (differential configuration)	V_{out} = 6Vp-p, A_V = 12dB F= 110kHz, R_L = 20Ω diff.		-97		dBc
HD3	3rd Harmonic distortion (differential configuration)	V_{out} = 6Vp-p, A_V = 12dB F= 110kHz, R_L = 20Ω diff.		-98		dBc
IM2	2nd Order Intermodulation Product (differential configuration)	F1= 100kHz, F2 = 110kHz V_{out} = 6Vp-p, A_V = 12dB R_L = 20Ω diff.		-86		dBc
		F1= 370kHz, F2 = 400kHz V_{out} = 6Vp-p, A_V = 12dB R_L = 20Ω diff.		-88		
IM3	3rd Order Intermodulation Product (differential configuration)	F1 = 100kHz, F2 = 110kHz V_{out} = 6Vp-p, A_V = 12dB R_L = 20Ω diff.		-90		dBc
		F1 = 370kHz, F2 = 400kHz V_{out} = 6Vp-p, A_V = 12dB R_L = 20Ω diff.		-85		

POWER DOWN MODE FEATURES (The Power Down command is a MOS input featuring a high input impedance)

V_{CC} = ±2.5Volts, 5Volts, ±6Volts or 12Volts, T_{amb} = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{pdw}	Pin (6) Threshold Voltage for Power Down Mode				V
	Low Level	$-V_{CC}$		$-V_{CC}+0.8$	
	High Level	$-V_{CC}+2$		$+V_{CC}$	
Icc_{pdw}	Power Down Mode Total Current Consumption@ V_{CC}=5V		69	80	µA
	Power Down Mode Total Current Consumption@ V_{CC}=12V		148	180	µA
R_{pdw}	Power Down Mode Output Impedance @ V_{CC}=5V		19	23	Ω
	Power Down Mode Output Impedance @ V_{CC}=12V		15.3	19	Ω
C_{pdw}	Power Down Mode Output Capacitance		63		pF

POWER DOWN CONTROL	CIRCUIT STATUS
V_{pdw}=Low Level	Active
V_{pdw}=High Level	Standby

Figure 1 : Load Configuration
Load: R_L=25Ω, V_{CC}=±6V

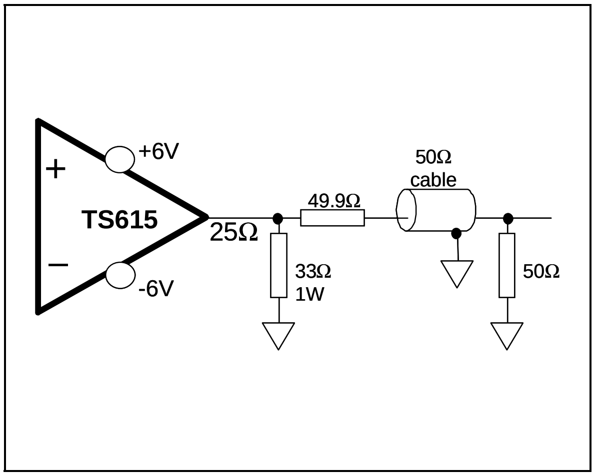


Figure 2 : Closed Loop Gain vs. Frequency
A_V=+1

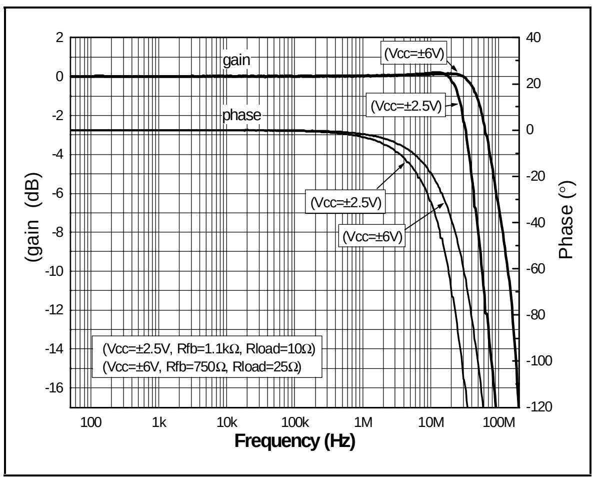


Figure 3 : Closed Loop Gain vs. Frequency
A_V=+2

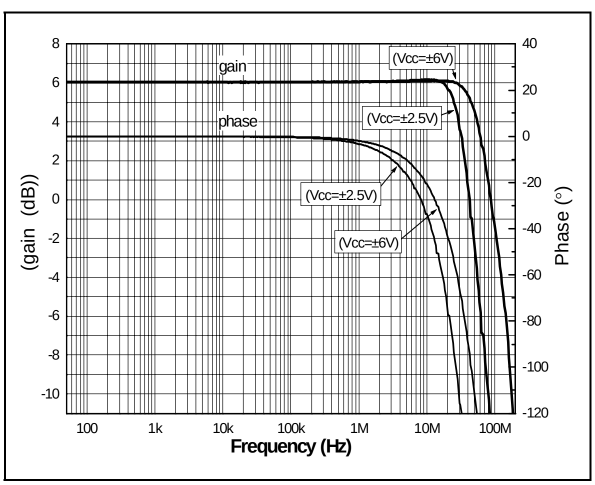


Figure 4 : Load Configuration
Load: R_L=10Ω, V_{CC}=±2.5V

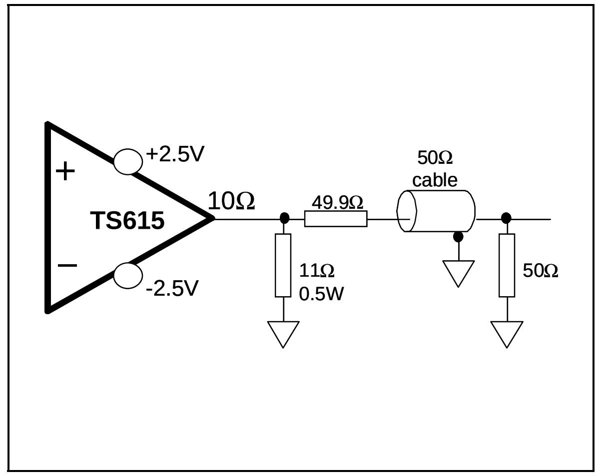


Figure 5 : Closed Loop Gain vs. Frequency
A_V=-1

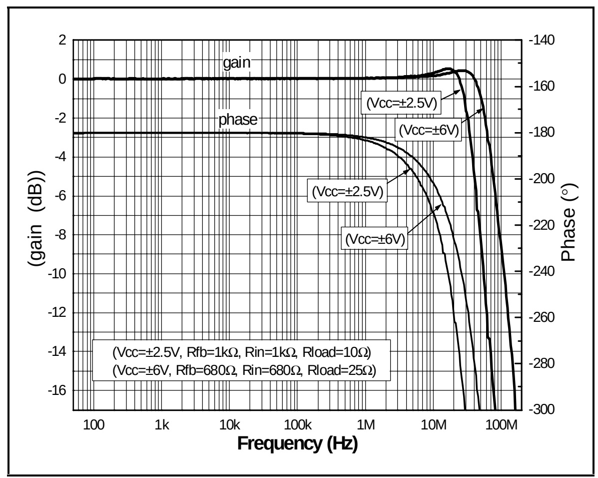


Figure 6 : Closed Loop Gain vs. Frequency
A_V=-2

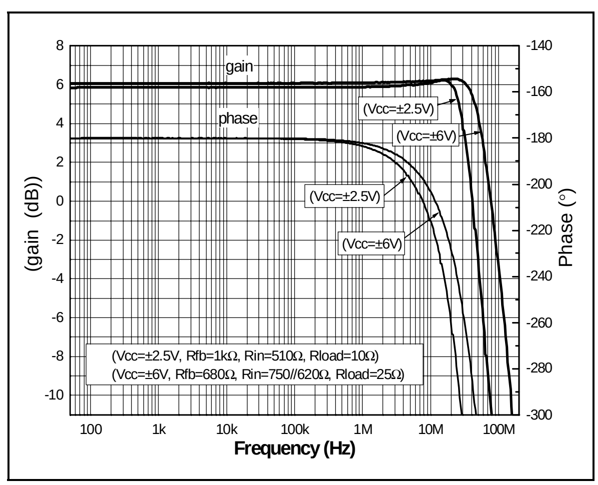


Figure 7 : Closed Loop Gain vs. Frequency
A_V=+4

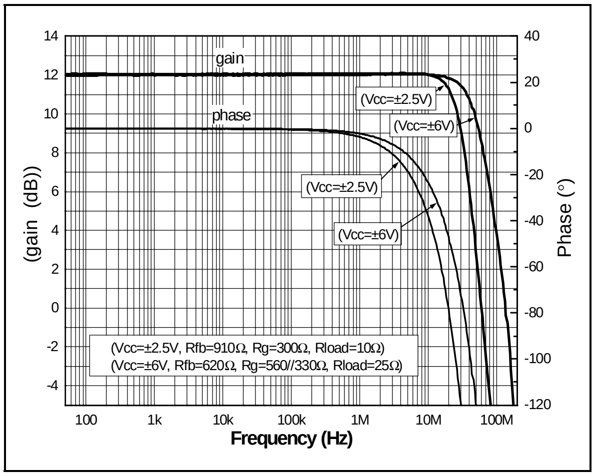


Figure 8 : Closed Loop Gain vs. Frequency
A_V=+8

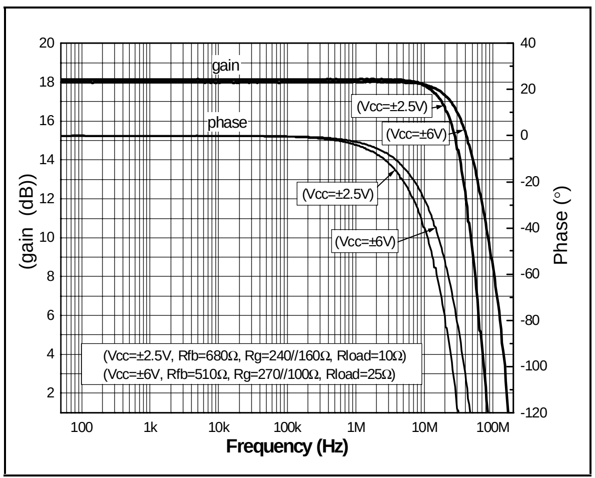


Figure 9 : Bandwidth vs. Temperature
A_V=+4, R_{fb}=910Ω

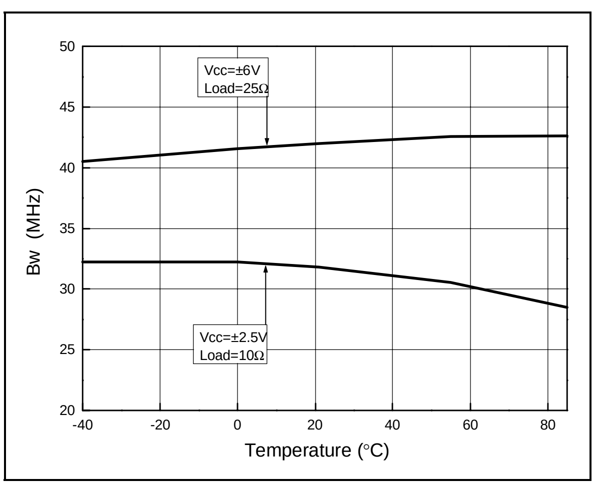


Figure 10 : Closed Loop Gain vs. Frequency
A_V=-4

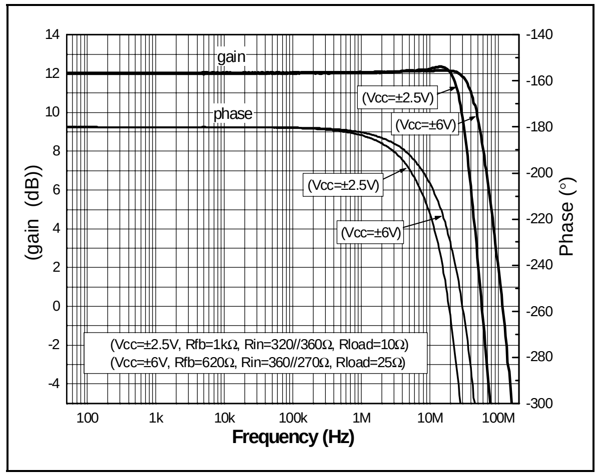


Figure 11 : Closed Loop Gain vs. Frequency
A_V=-8

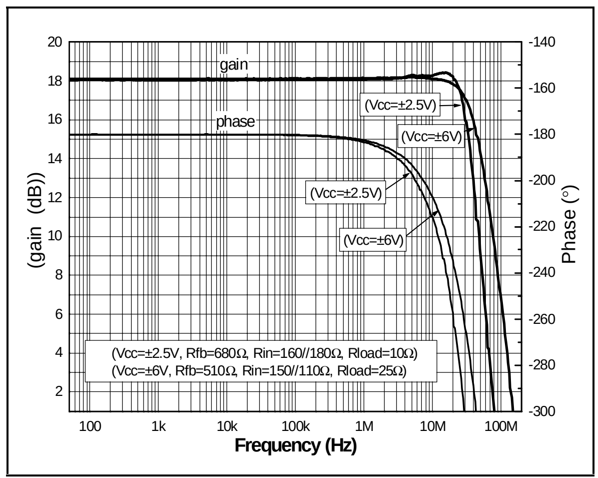


Figure 12 : Positive Slew Rate
A_V=+4, R_{fb}=620Ω, V_{CC}=±6V, R_L=25Ω

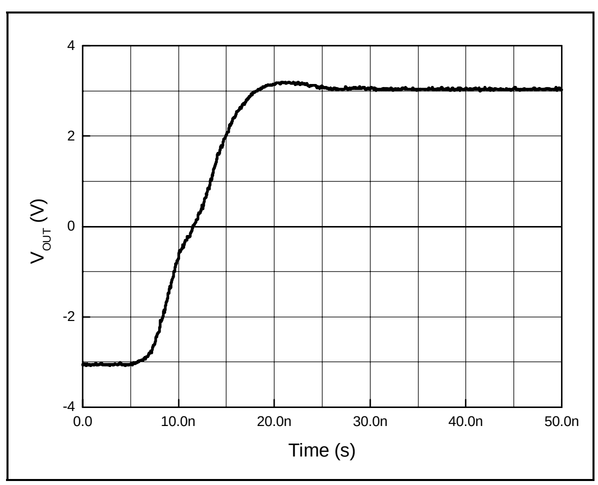


Figure 13 : Positive Slew Rate
A_V=+4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

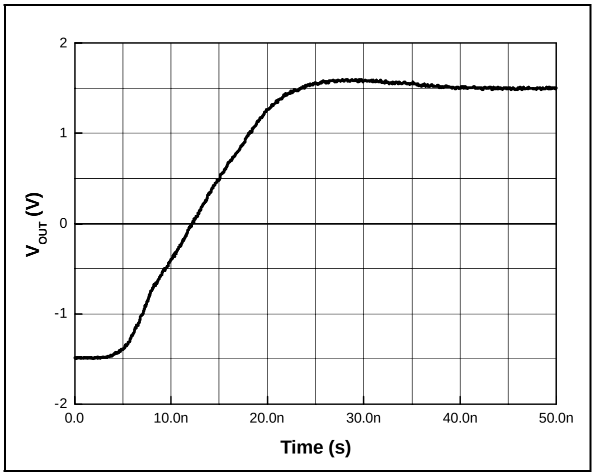


Figure 14 : Negative Slew Rate
A_V=+4, R_{fb}=620Ω, V_{CC}=±6V, R_L=25Ω

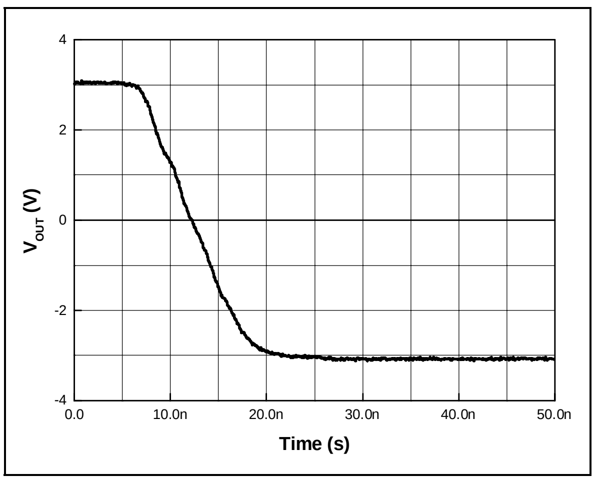


Figure 15 : Negative Slew Rate
A_V=+4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

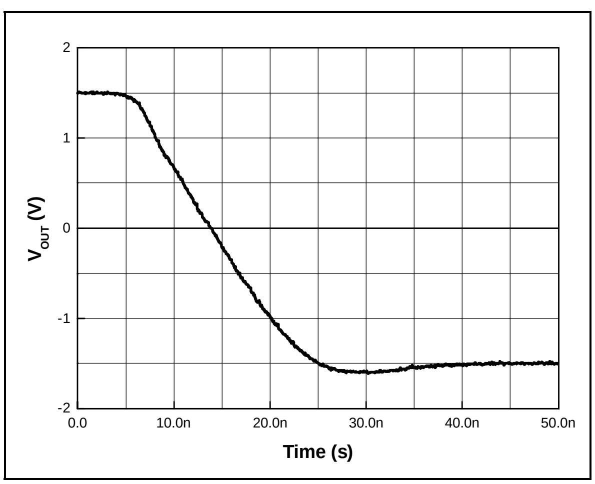


Figure 16 : Positive Slew Rate
A_V= - 4, R_{fb}=620Ω, V_{CC}=±6V, R_L=25Ω

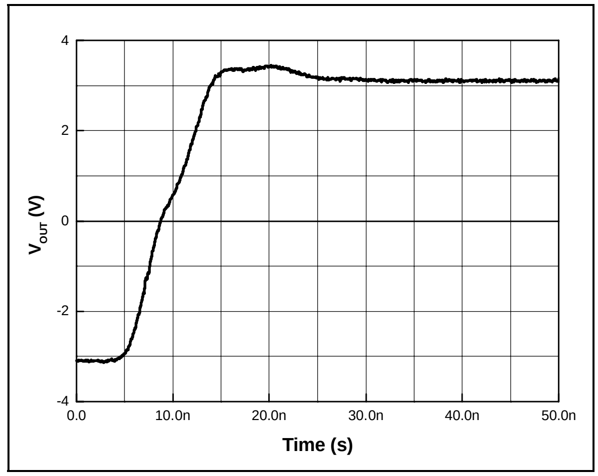


Figure 17 : Positive Slew Rate
A_V= - 4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

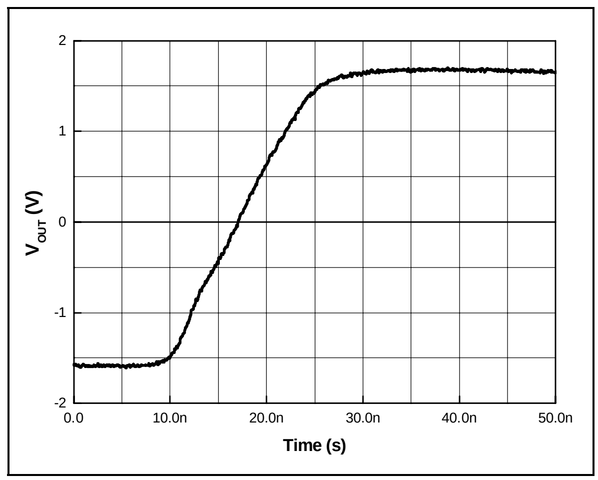


Figure 18 : Negative Slew Rate
A_V= - 4, R_{fb}=620Ω, V_{CC}=±6V, R_L=25Ω

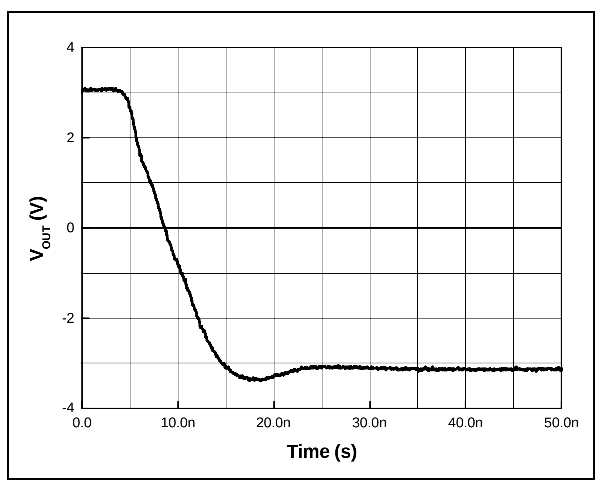


Figure 19 : Negative Slew Rate
A_V= - 4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

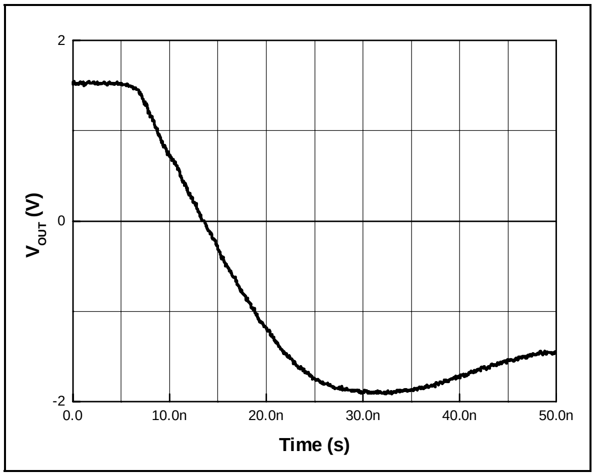


Figure 20 : Slew Rate vs. Temperature
A_V=+4, R_{fb}=910Ω, V_{CC}=±2.5V, R_L=10Ω

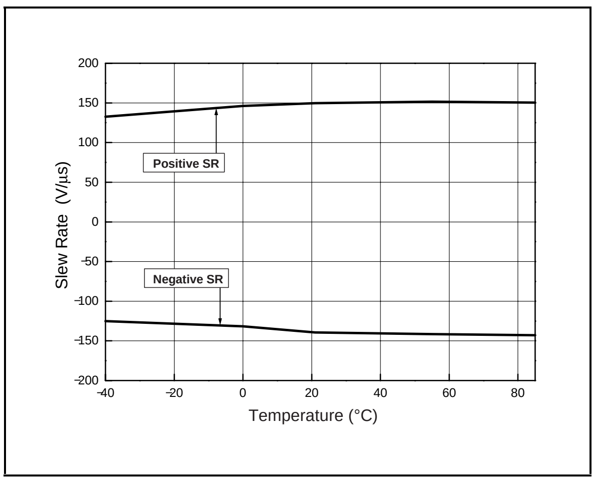


Figure 21 : Slew Rate vs. Temperature
A_V=+4, R_{fb}=910Ω, V_{CC}=±6V, R_L=25Ω

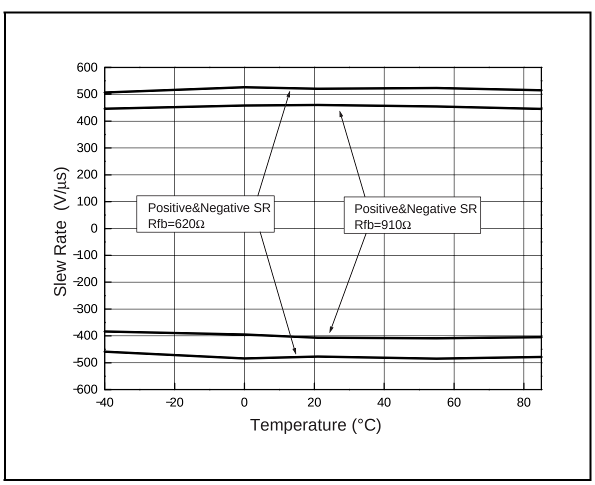


Figure 22 : Input Voltage Noise Level
A_V=+92, R_{fb}=910Ω, Input+ connected to Gnd via 10Ω

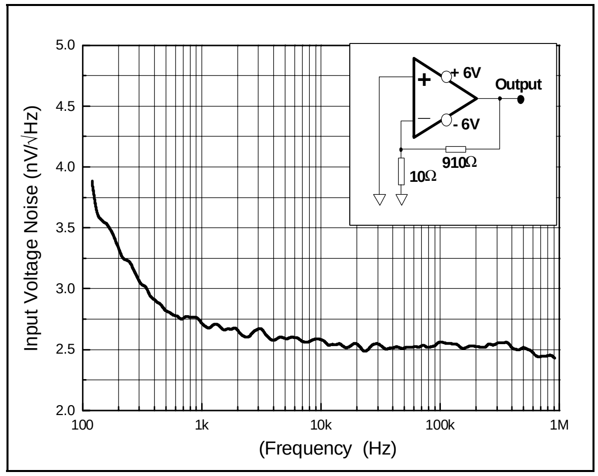


Figure 23 : Transimpedance vs. Temperature
Open Loop

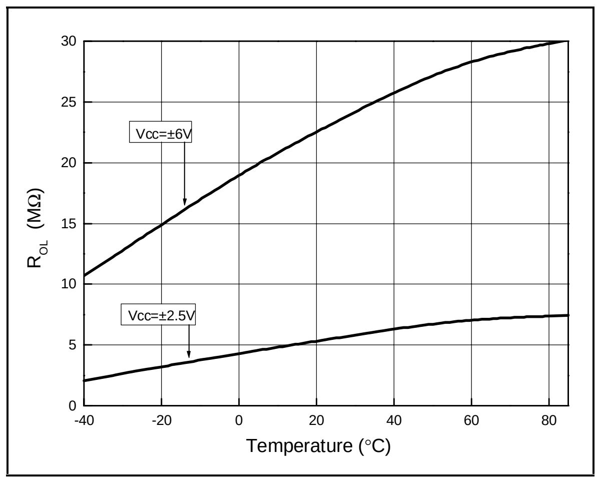


Figure 24 : Icc vs. Power Supply
Open loop, no load

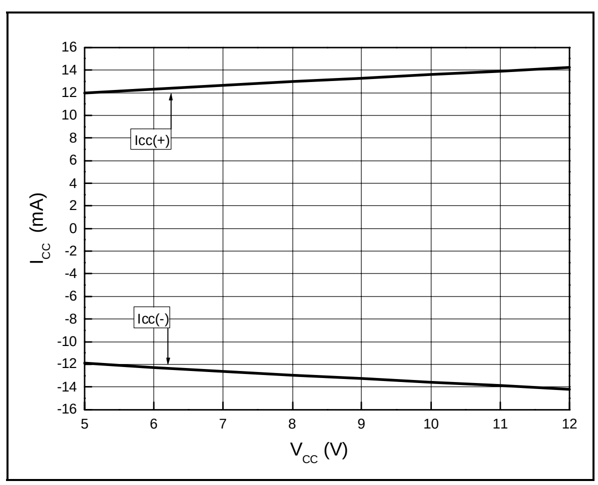


Figure 25 : Iib vs. Power Supply
Open loop, no load

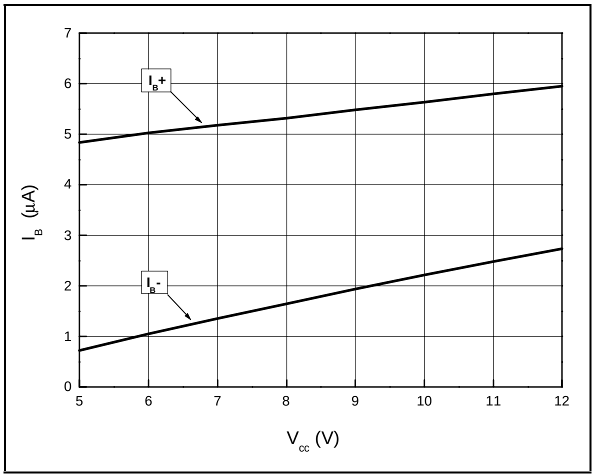


Figure 26 : Iib(-) vs. Temperature
Open loop, no load

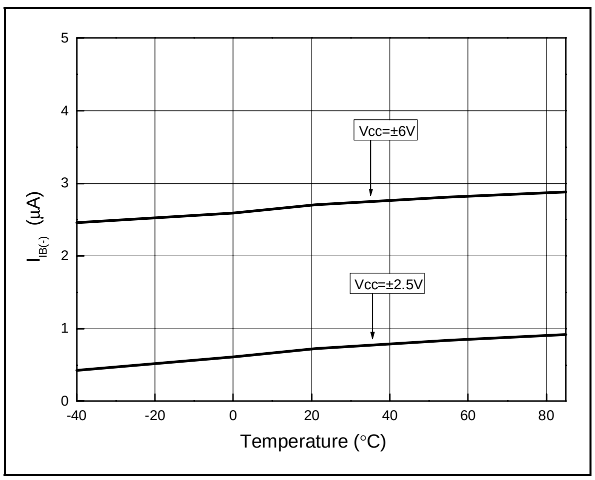


Figure 27 : Icc vs. Temperature
Open loop, no load

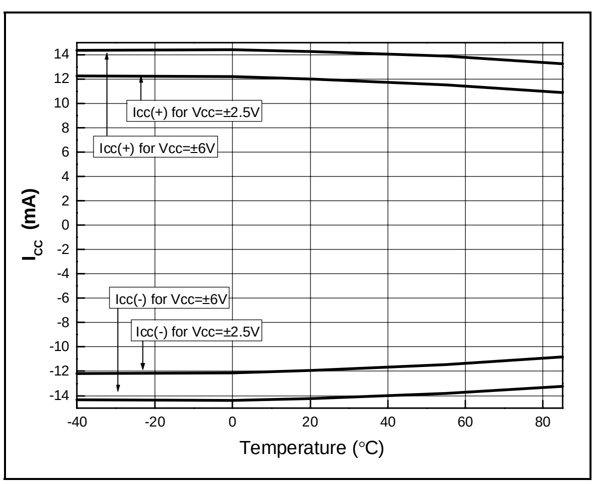


Figure 28 : Iib(+) vs. Temperature
Open loop, no load

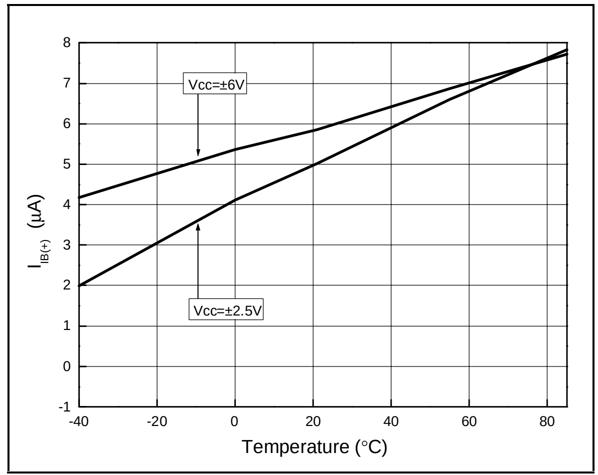


Figure 29 : Voh & Vol vs. Power Supply
Open loop, R_L=25Ω

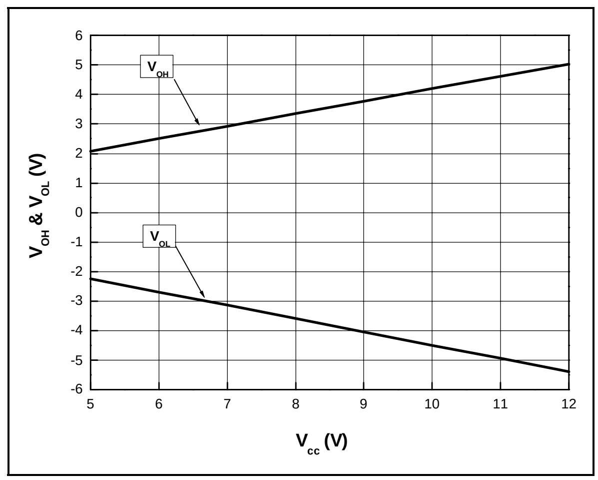


Figure 30 : Voh vs. Temperature
Open loop

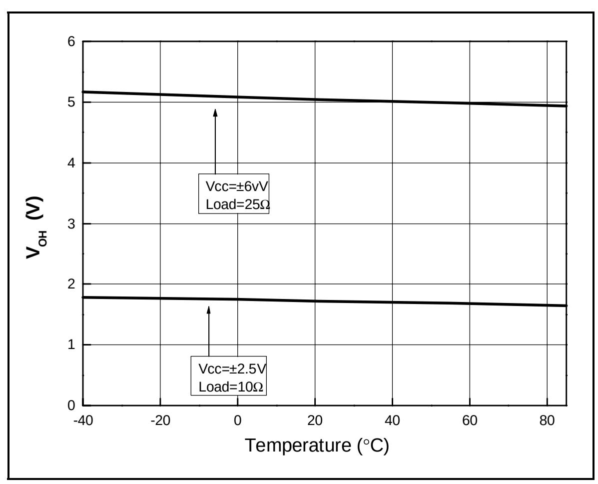


Figure 31 : Vol vs. Temperature
Open loop

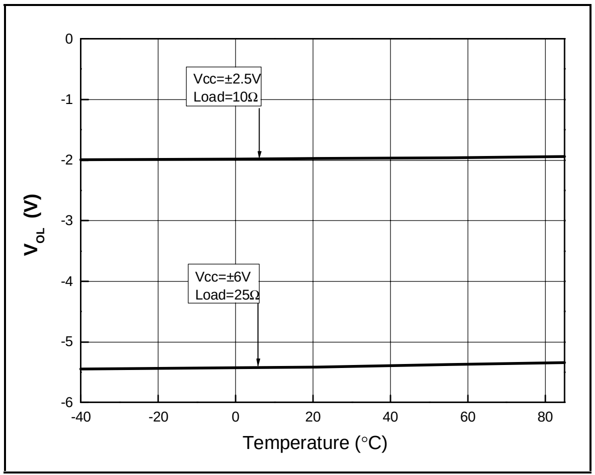


Figure 32 : Differential Vio vs. Temperature
Open loop, no load

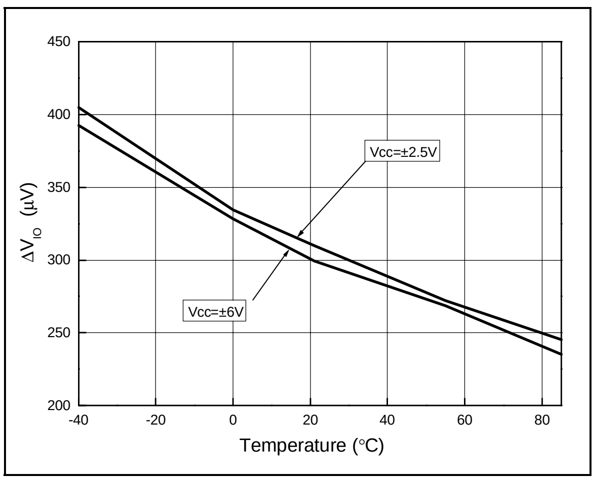


Figure 33 : Vio vs. Temperature
Open loop, no load

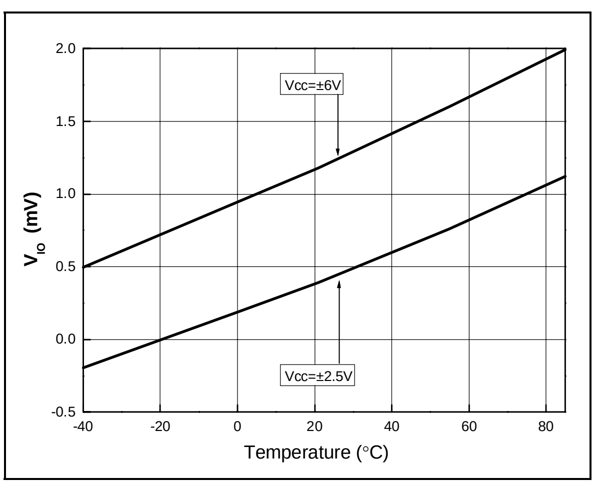


Figure 34 : CMR vs. Temperature
Open loop, no load

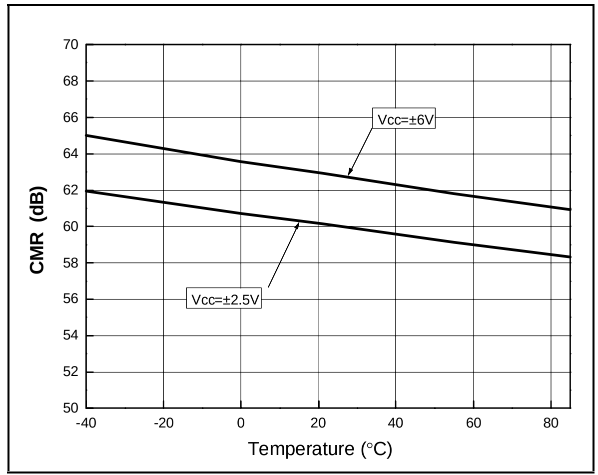


Figure 35 : SVR vs. Temperature
Open loop, no load

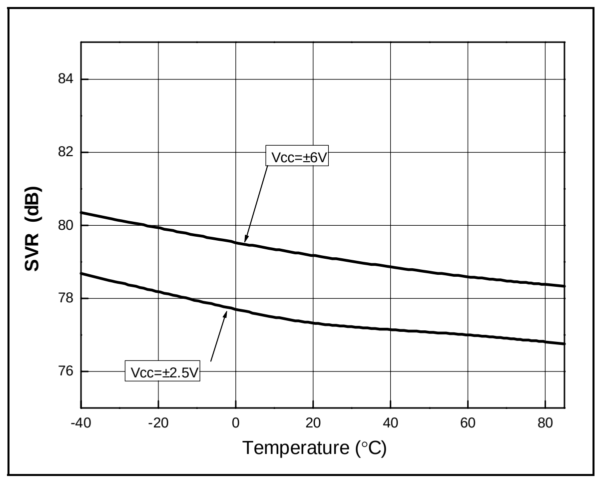


Figure 36 : Iout vs. Temperature
Open loop, V_{CC}=±6V, R_L=10Ω

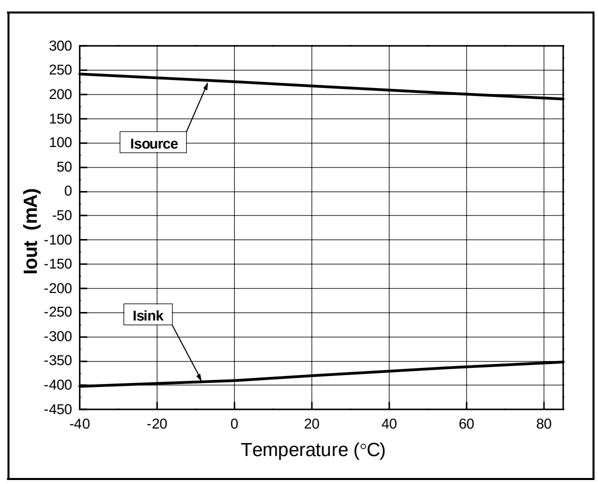


Figure 37 : Iout vs. Temperature
Open loop, V_{CC}=±2.5V, R_L=25Ω

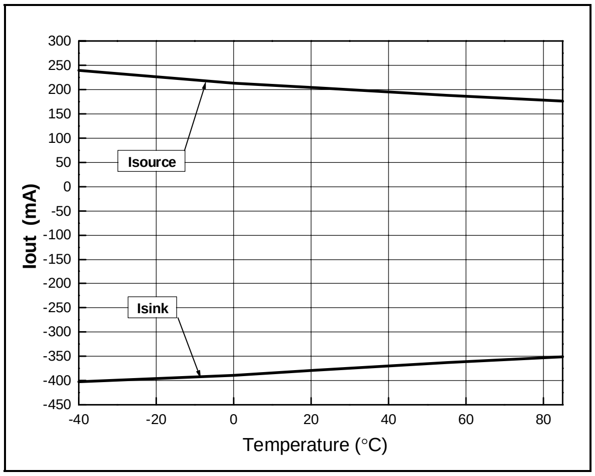


Figure 38 : Maximum Output Amplitude vs. Load
A_V=+4, R_{fb}=620Ω, V_{CC}=±6V

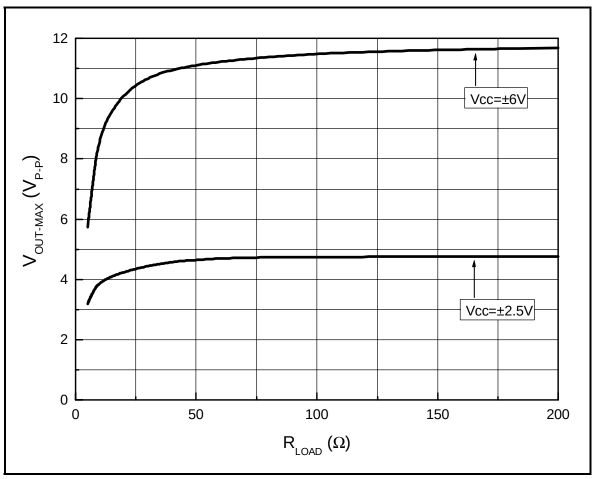


Figure 39 : Isink vs. Output Amplitude.
V_{CC}=±2.5V, Open Loop, no Load

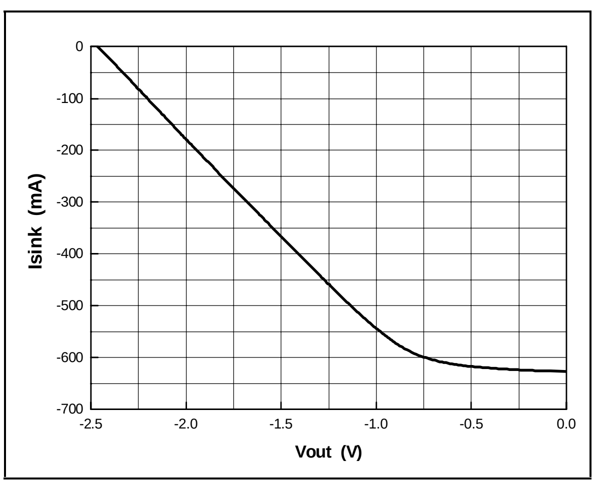


Figure 40 : Isource vs. Output Amplitude.
V_{CC}=±2.5V, Open Loop, no Load

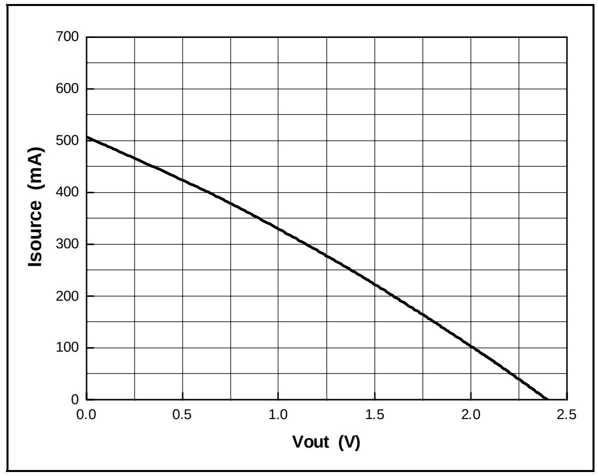


Figure 41 : Isink vs. Output Amplitude
V_{CC}=±6V, Open Loop, no Load

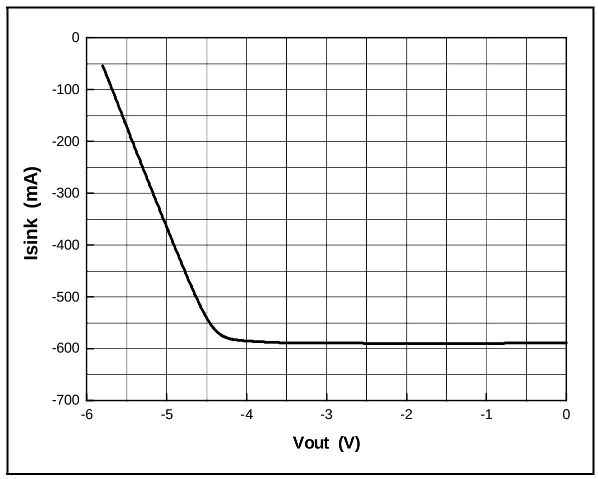


Figure 42 : Isource vs. Output Amplitude
V_{CC}=±6V, Open Loop, no Load

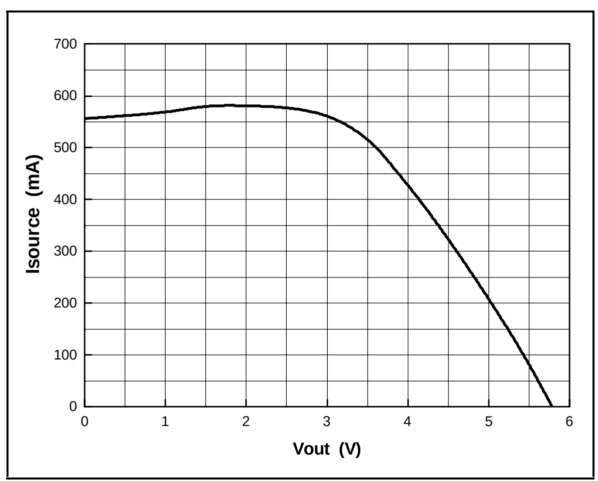


Figure 43 : Icc (Power Down) vs. Temperature
No load, Open Loop

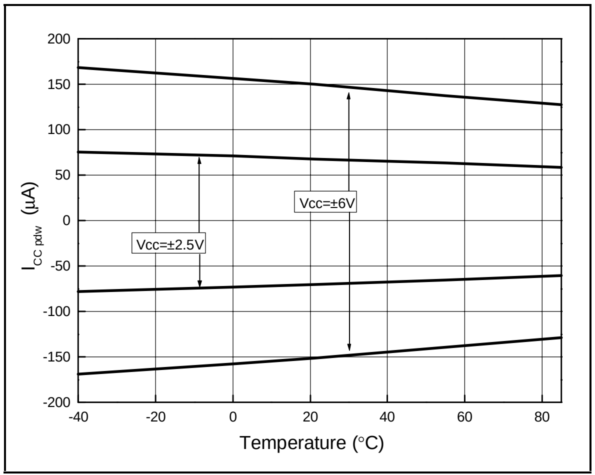
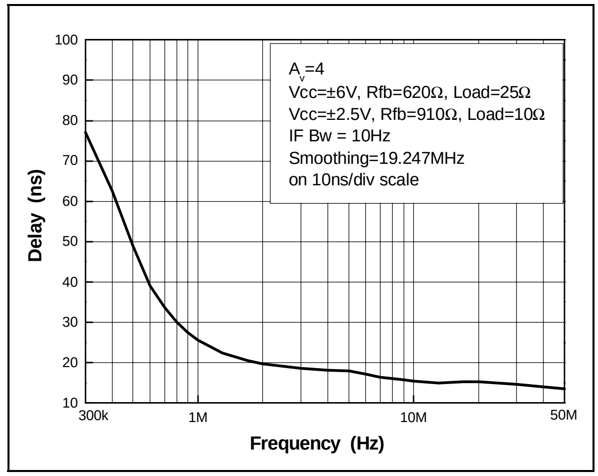


Figure 44 : Group Delay
V_{CC}=±6V, V_{CC}=±2.5V



INTERMODULATION DISTORTION PRODUCT

A non-ideal output of the amplifier can be described by the following development :

$$Vout = C_0 + C_1 V_{in} + C_2 V^2{}_{in} + \ldots C_n V^n{}_{in}$$

due to a non-linearity in the input-output amplitude transfer. In the case of the input is V_{in}=Asinωt, C_0 is the DC component, $C_1(V_{in})$ is the fundamental, C_n is the amplitude of the harmonics of the output signal V_{out}.

A one-frequency (one-tone) input signal contributes to a harmonic distortion. A two-tones input signal contributes to a harmonic distortion and intermodulation product.

This intermodulation product or intermodulation distortion study of a two-tones input signal is the first step of the amplifier characterization of driving capability in the case of a multi-tone signal.

In this case :

$$+ C_2(A\sin\omega_1 t + B\sin\omega_2 t)^2$$

$$\ldots + C_n(A\sin\omega_1 t + B\sin\omega_2 t)^n$$

$$V_{in} = A\sin\omega_1 t + B\sin\omega_2 t$$

$$V_{out} = C_0 + C_1(A\sin\omega_1 t + B\sin\omega_2 t)$$

and :

$$+ C_1(A\sin\omega_1 t + B\sin\omega_2 t)$$

$$-\frac{C_2}{2}\left(A^2\cos 2\omega_1 t + B^2\cos 2\omega_2 t\right)$$

$$+ 2C_2AB(\cos(\omega_1 - \omega_2)t - \cos(\omega_1 - \omega_2)t)$$

$$+\left(3\frac{C_3}{4}\right)\text{¥}$$

$$+\left(C_3A^3\sin 3\omega_1 t + B^3\sin 3\omega_2 t\right)$$

$$+\frac{3C_3A^2B}{2}\left(\sin(2\omega_1 - \omega_2)t - \frac{1}{2}\sin(2\omega_1 + \omega_2)t\right)$$

$$+\frac{3C_3A^2B}{2}\left(\sin(-\omega_1 + 2\omega_2)t - \frac{1}{2}\sin(\omega_1 + 2\omega_2)t\right)$$

$$\ldots + C_n(V_{in})^n$$

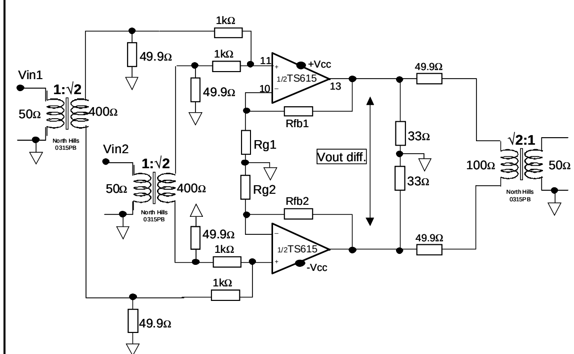
$$V_{out} = C_0 + C_2\left(\frac{A^2 + B^2}{2}\right)$$

$$\left(A^3\sin\omega_1 t + B^3\sin\omega_2 t + 2A^2B\sin\omega_1 t + 2AB^2\sin\omega_2 t\right.$$

In this expression, we recognize the second order intermodulation IM2 by the frequencies (ω_1-ω_2) and (ω_1+ω_2) and the third order intermodulation IM3 by the frequencies (2ω_1-ω_2), (2ω_1+ω_2), (−ω_1+2ω_2) and (ω_1+2ω_2).

The measurement of the intermodulation product of the driver is achieved by using the driver as a mixer by a summing amplifier configuration. By this way, the non-linearity problem of an external mixing device is avoided.

Figure 45 : Non-inverting Summing Amplifier



The following graphs show the IM2 and the IM3 of the amplifier in different configuration. The two-tones input signal is achieved by the multi-source generator Marconi 2026. Each tone has the same amplitude. The measurement is achieved by the spectrum analyzer HP3585A.

Figure 46 : Intermodulation vs. Output Amplitude
370kHz & 400kHz, A_V=+1.5, R_{fb}=1kΩ, R_L=14Ω diff.,V_{CC}=±2.5V

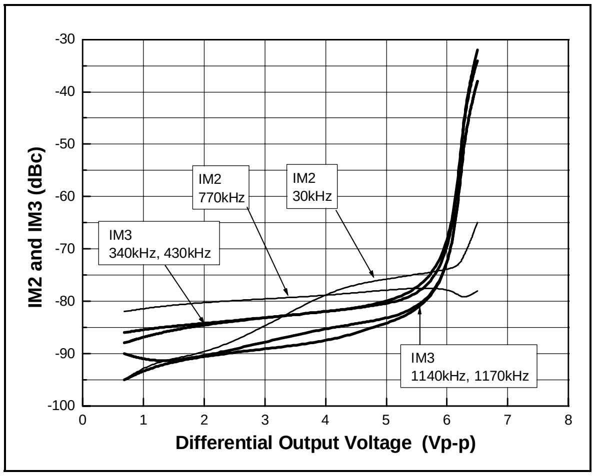


Figure 47 : Intermodulation vs. Output Amplitude
370kHz & 400kHz, A_V=+1.5, R_{fb}=1kΩ, R_L=28Ω diff.,V_{CC}=±2.5V

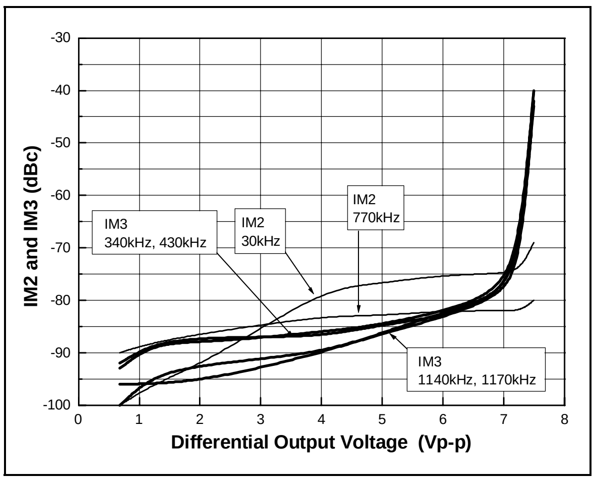


Figure 48 : Intermodulation vs. Gain
370kHz & 400kHz, R_L=20Ω diff., Vout=6Vpp, V_{CC}=±2.5V

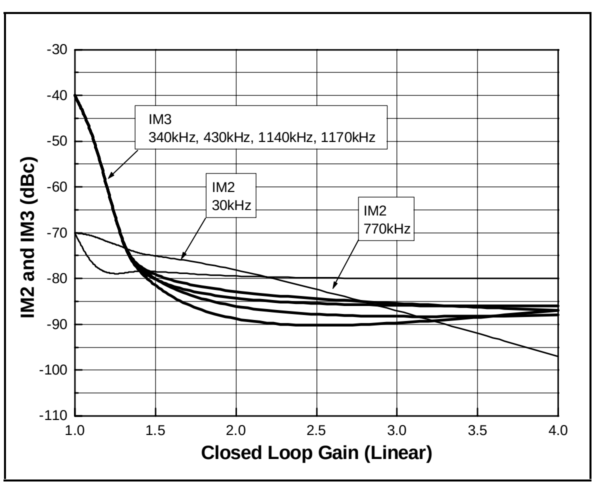


Figure 49 : Intermodulation vs. Load
370kHz & 400kHz, A_V=+1.5, R_{fb}=1kΩ, Vout=6.5Vpp,V_{CC}=±2.5V

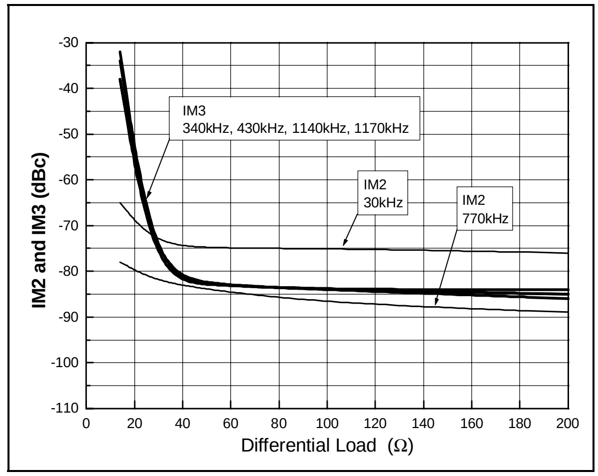


Figure 50 : Intermodulation vs. Output Amplitude
100kHz & 110kHz, A_V=+4, R_{fb}=620Ω, R_L=200Ω diff.,V_{CC}=±6V

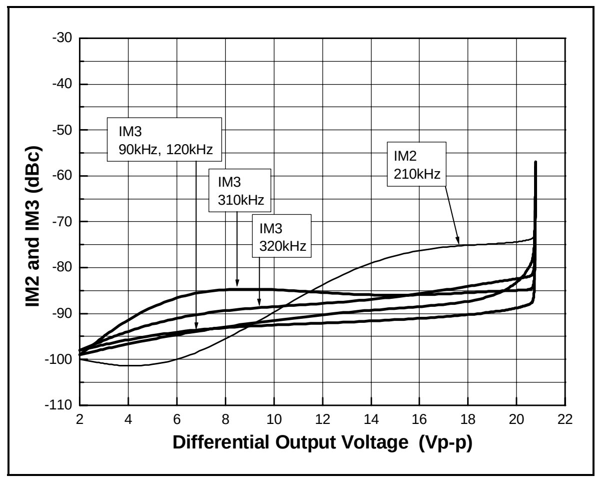


Figure 51 : Intermodulation vs. Output Amplitude
100kHz & 110kHz, A_V=+4, R_{fb}=620Ω, R_L=50Ω diff., V_{CC}=±6V

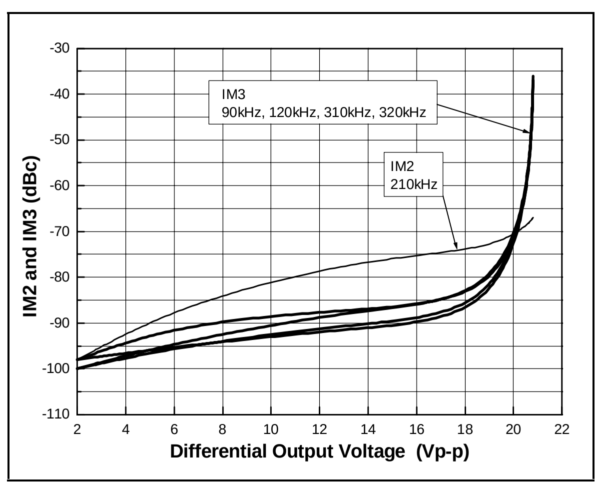


Figure 52 : Intermodulation vs. Frequency Range
A_V=+4, R_{fb}=620Ω, R_L=50Ω diff., Vout=16Vpp, V_{CC}=±6V

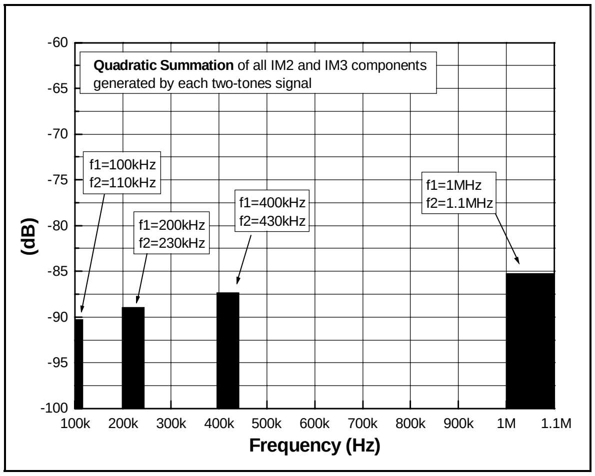


Figure 53 : Intermodulation vs. Output Amplitude
370kHz & 400kHz, A_V=+4, R_{fb}=620Ω, R_L=200Ω diff.,V_{CC}=±6V

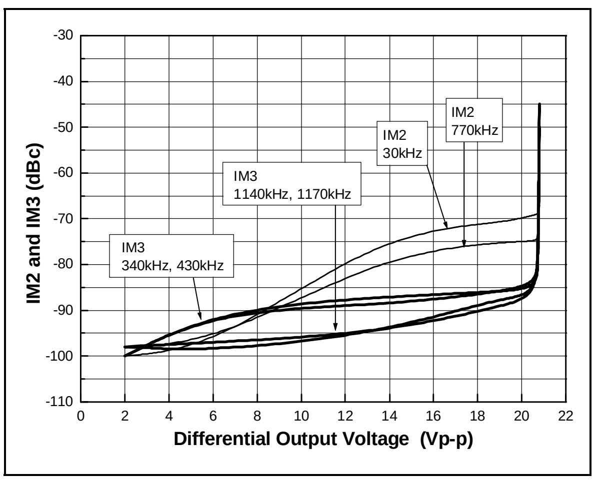
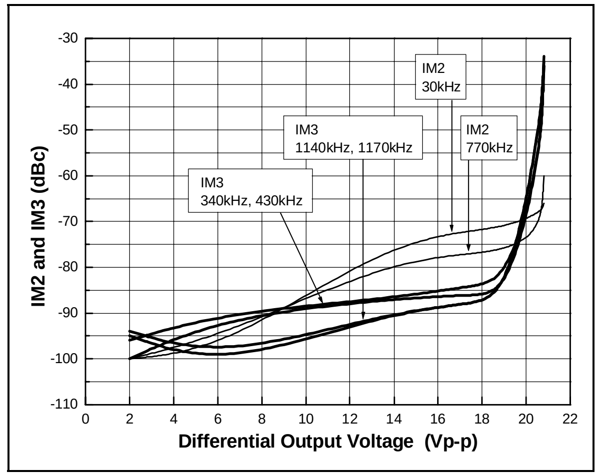


Figure 54 : Intermodulation vs. Output Amplitude
370kHz & 400kHz, A_V=+4, R_{fb}=620Ω, R_L=50Ω diff., V_{CC}=±6V



PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

In this range of frequency, printed circuit board parasites can affect the closed-loop performance.

The implementation of a proper ground plane in both sides of the PCB is mandatory to provide low inductance and low resistance common return. Most important for controlling the gain flatness and the bandwidth are stray capacitances at the output and inverting input. For minimizing the coupling, the space between signal lines and ground plane will be increased. Connections of the feedback components must be as short as possible in order to decrease the associated inductance which affect high frequency gain errors. It is very important to choose external components as small as possible such as surface mounted devices, SMD, in order to minimize the size of all the DC and AC connections.

THERMAL INFORMATION

The TS615 is housed in an Exposed-Pad plastic package. As described on the figure 56, this package uses a lead frame upon which the dice is mounted. This lead frame is exposed as a thermal pad on the underside of the package. The thermal contact is direct with the dice. This thermal path provide an excellent thermal performance.

The thermal pad is electrically isolated from all pins in the package. It should be soldered to a copper area of the PCB underneath the package. Through these thermal paths within this copper area, heat can be conducted away from the package. In this case, the copper area should be connected to ($-V_{CC}$).

Figure 55 : Exposed-Pad Package

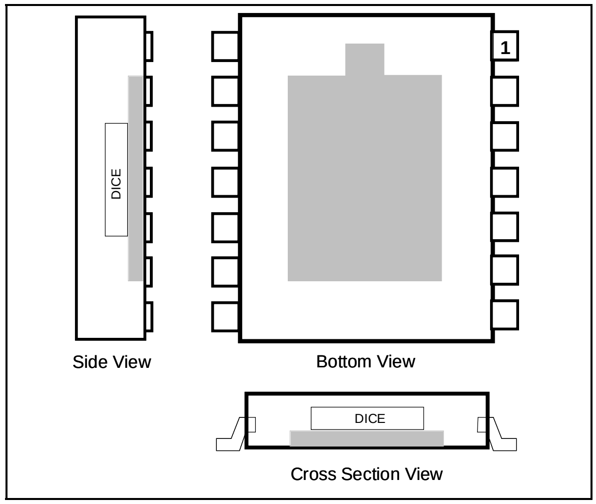


Figure 56 : Evaluation Board

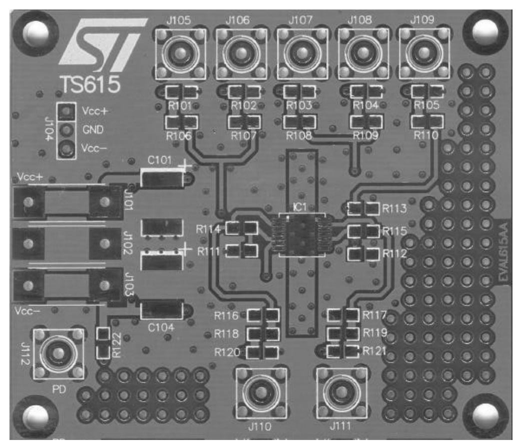


Figure 57 : Schematic Diagram

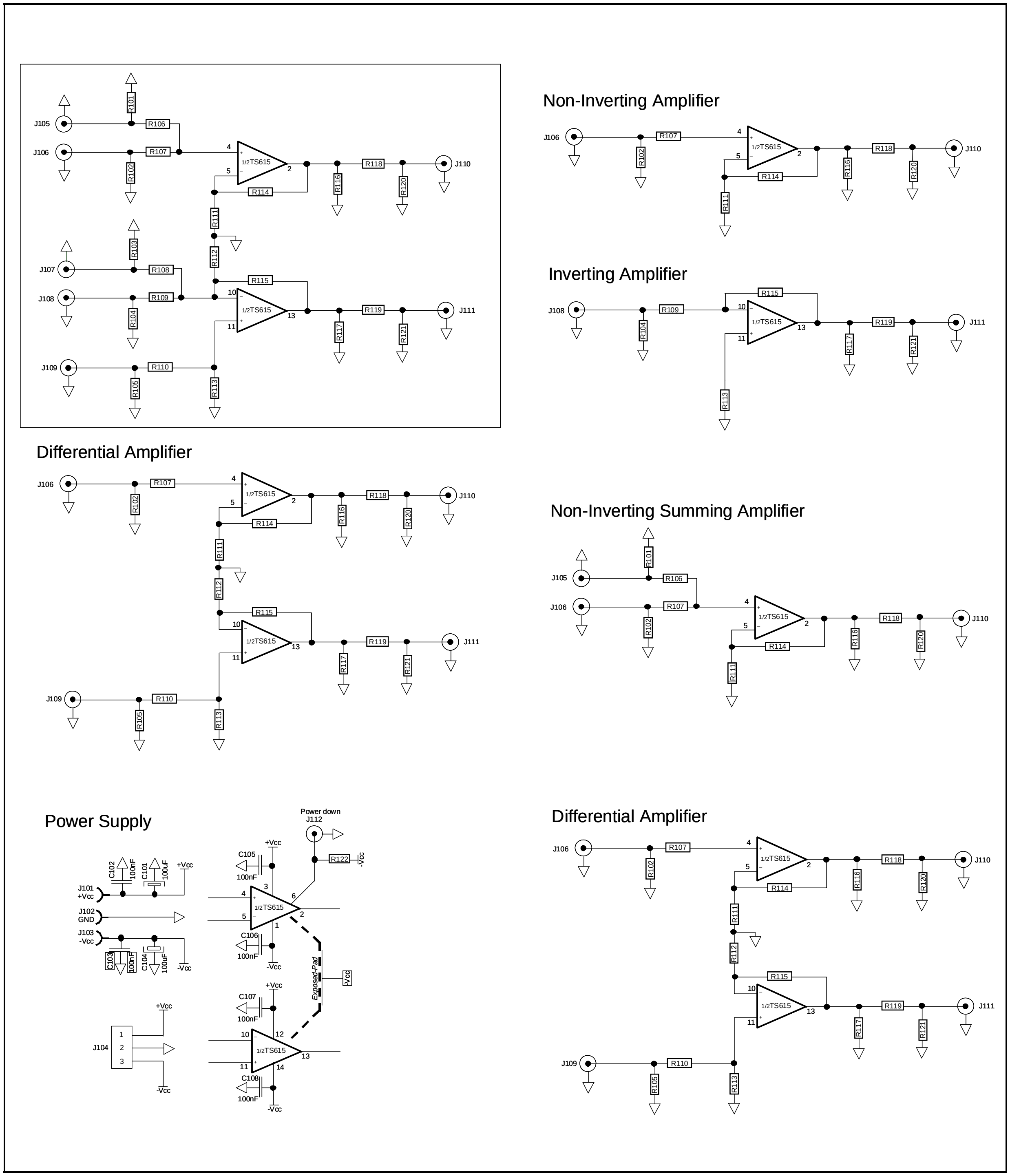


Figure 58 : Component Locations - Top Side

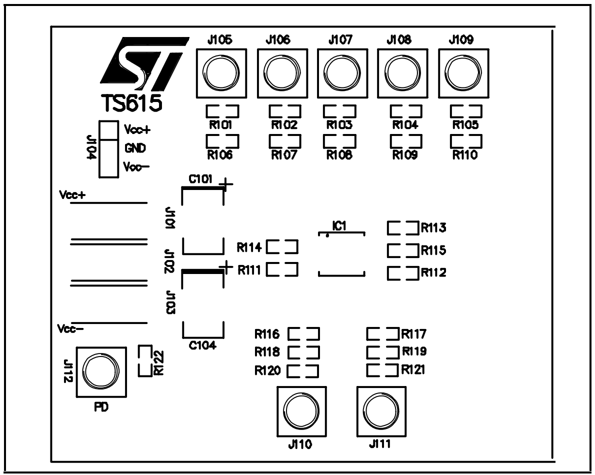


Figure 60 : Top Side Board Layout

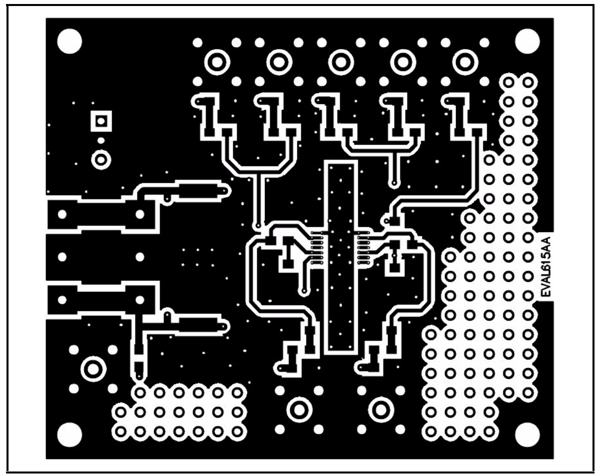


Figure 59 : Component Locations - Bottom Side

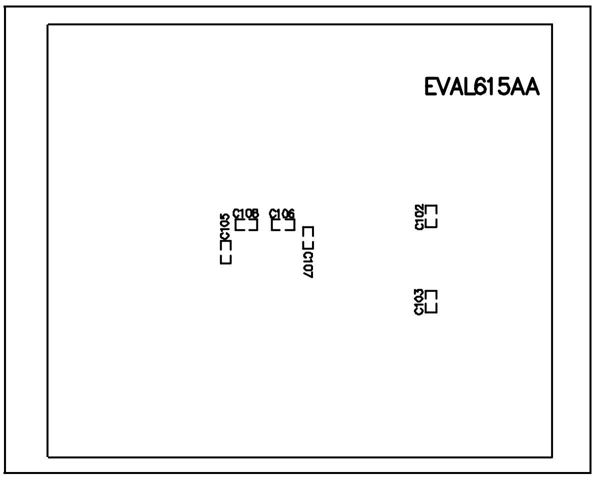
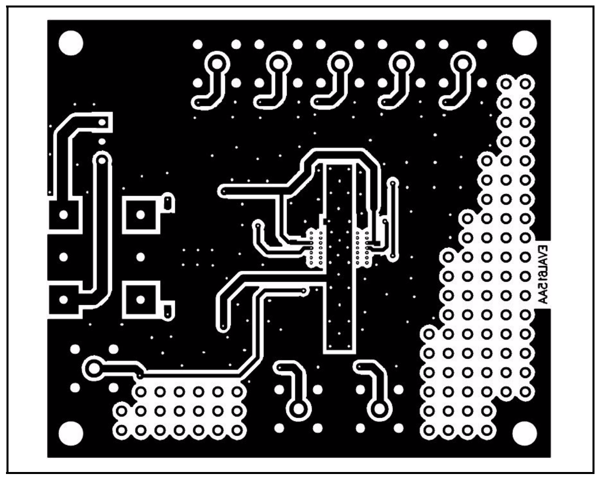
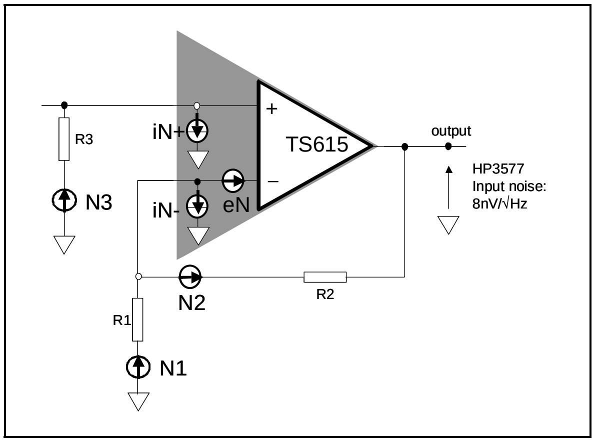


Figure 61 : Bottom Side Board Layout



NOISE MEASUREMENT

Figure 62 : Noise Model



eN : input voltage noise of the amplifier
iNn : negative input current noise of the amplifier
iNp : positive input current noise of the amplifier
The closed loop gain is :

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

The six noise sources are :

$$V2 = iNn \times R2$$

$$V5 = \sqrt{4kTR2}$$

$$V1 = eN \times \left(1 + \frac{R2}{R1}\right)$$

$$V3 = iNp \times R3 \times \left(1 + \frac{R2}{R1}\right)$$

$$V4 = -\frac{R2}{R1} \times \sqrt{4kTR1}$$

$$V6 = \left(1 + \frac{R2}{R1}\right)\sqrt{4kTR3}$$

Assuming the thermal noise of a resistance R as:

$$\sqrt{4kTR\Delta F}$$

with ΔF the specified bandwidth.
On 1Hz bandwidth the thermal noise is reduced to

$$\sqrt{4kTR}$$

k is the Boltzmann's constant equals to 1,374.10-23J/°K. T is the temperature (°K).

The output noise eNo is calculated using the Superposition Theorem. But it is not the sum of all noise sources. The output noise is the square root of the sum of the square of each noise source.

$$eNo = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2}, (eq1)$$

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2$$

$$\ldots + \left(\frac{R2}{R1}\right)^2 \times 4kTR1 + 4kTR2 + \left(1 + \frac{R2}{R1}\right)^2 \times 4kTR3, (eq2)$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

$$eNo = \sqrt{(Measured)^2 - (instrumentation)^2}, (eq3)$$

The input noise is called the Equivalent Input Noise as it is not directly measured but it is evaluated from the measurement of the output divided by the closed loop gain (eNo/g).
After simplification of the fourth and the fifth term of (eq2) we obtain:

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2$$

$$\ldots + g \times 4kTR2 + \left(1 + \frac{R2}{R1}\right)^2 \times 4kTR3, (eq4)$$

Measurement of eN:
We assume a short-circuit on the non-inverting input (R3=0). (eq4) comes:

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2}, (eq5)$$

In order to easily extract the value of eN, the resistance R2 will be chosen as low as possible. In the other hand, the gain must be large enough.
R1=10Ω, R2=910Ω, R3=0, Gain=92
Equivalent Input Noise: 2.57nV/√Hz
Input Voltage Noise: eN=2.5nV/√Hz

Measurement of iNn:
R3=0 and the output noise equation is still the (eq5). This time the gain must be decreased to decrease the thermal noise contribution.
R1=100Ω, R2=910Ω, R3=0, Gain=10.1
Equivalent Input Noise: 3.40nV/√Hz
Negative Input Current Noise: iNn =21pA/√Hz

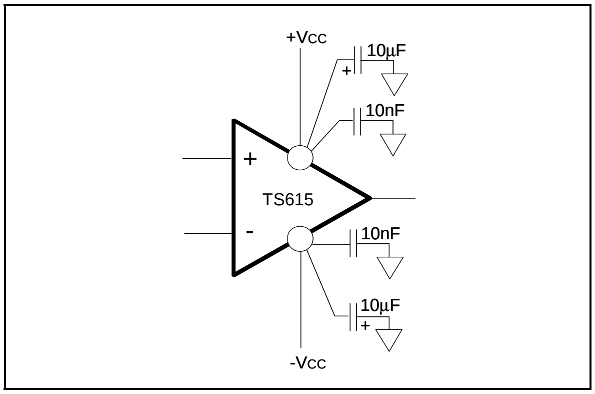
Measurement of iNp:
To extract iNp from (eq3), a resistance R3 is connected to the non-inverting input. The value of R3 must be chosen in order to keep its thermal noise contribution as low as possible against the iNp contribution.
R1=100Ω, R2=910Ω, R3=100Ω, Gain=10.1
Equivalent Input Noise: 3.93nV/√Hz
Positive Input Current Noise: iNp=15pA/√Hz

Conditions: frequency=100kHz, V_{CC}=±2.5V
Instrumentation: Spectrum Analyzer HP3585A
(input noise of the HP3585A: 8nV/√Hz)

POWER SUPPLY BYPASSING

A proper power supply bypassing comes very important for optimizing the performance in high frequency range. Bypass capacitors should be placed as close as possible to the IC pins to improve high frequency bypassing. A capacitor greater than 1µF is necessary to minimize the distortion. For a better quality bypassing a capacitor of 10nF is added following the same condition of implementation. These bypass capacitors must be incorporated for the negative and the positive supply.

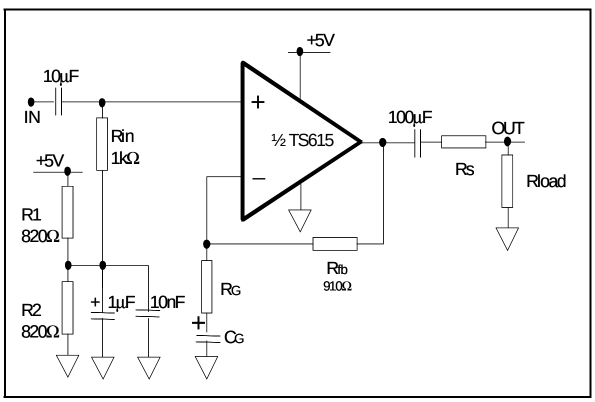
Figure 63 : Circuit for Power Supply Bypassing



SINGLE POWER SUPPLY

The following figure show the case of a 5V single power supply configuration

Figure 64 : Circuit for +5V single supply



The TS615 operates from 12V down to 5V power supplies. This is achieved with a dual power supply of ±6V and ±2.5V or a single power supply of 12V and 5V referenced to the ground. In the case of this asymmetrical supplying, a new biasing is necessary to assume a positive output dynamic range between 0V and $+V_{CC}$ supply rails. Considering the values of V_{OH} and V_{OL}, the amplifier will provide an output dynamic from +0.5V to 10.6V on 25Ω load for a 12V supplying, from 0.45V to 3.8V on 10Ω load for a 5V supplying.

The amplifier must be biased with a mid supply (nominally $+V_{CC}/2$), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply (such as a virtual ground using an operational amplifier), or a two-resistance divider which is the cheapest solution. A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (30µA max.) as the 1% of the current through the resistance divider to keep a stable mid supply, two resistances of 2.2kΩ can be used in the case of a 12V power supply and two resistances of 820Ω can be used in the case of a 5V power supply.

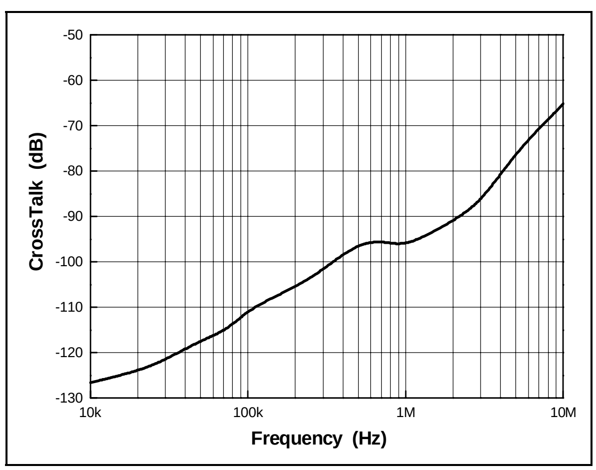
The input provides a high pass filter with a break frequency below 10Hz which is necessary to remove the original 0 volt DC component of the input signal, and to fix it at $+V_{CC}/2$.

CHANNEL SEPARATION - CROSSTALK

The following figure show the crosstalk from an amplifier to a second amplifier. This phenomenon, accented in high frequencies, is unavoidable and intrinsic of the circuit.

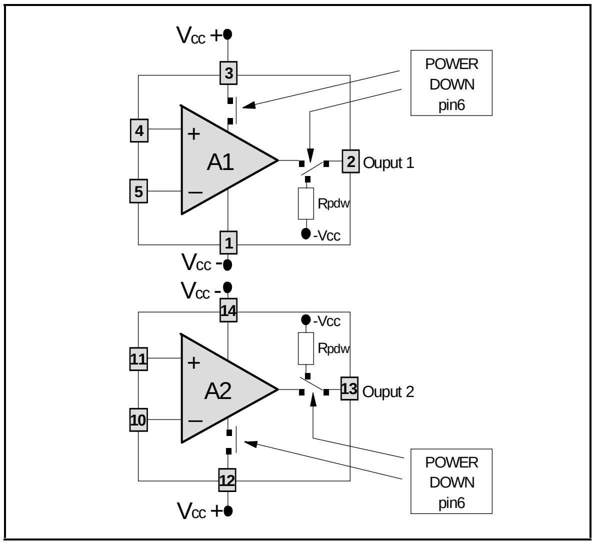
Nevertheless, the PCB layout has also an effect on the crosstalk level. Capacitive coupling between signal wires, distance between critical signal nodes, power supply bypassing, are the most significant points.

Figure 65 : Crosstalk vs. Frequency
A_V=+4, R_{fb}=620Ω, V_{CC}=±6V, Vout=2Vp



POWER DOWN MODE BEHAVIOUR

Figure 66 : Equivalent Schematic



Please note that the short circuited output in power down mode is referenced to ($-V_{CC}$). No problem appears when used in differential mode. Nevertheless, when used in single ended on a load referenced to GND, the ($-V_{CC}$) level contributes to a current consumption through the load. As described on the Figure 68, the interest of featuring an output short circuit in power down mode is to keep the best impedance matching between the system and the twisted pair telephone line when the modem is in sleep mode. By this way, the modem can be waked-up with a signal from the line without any damage of this signal. This concept is particularly intended for the ADSL over voice modems, where the modem in sleep mode, must be waked-up by the phone call.

Figure 67 : Matching in Sleep Mode

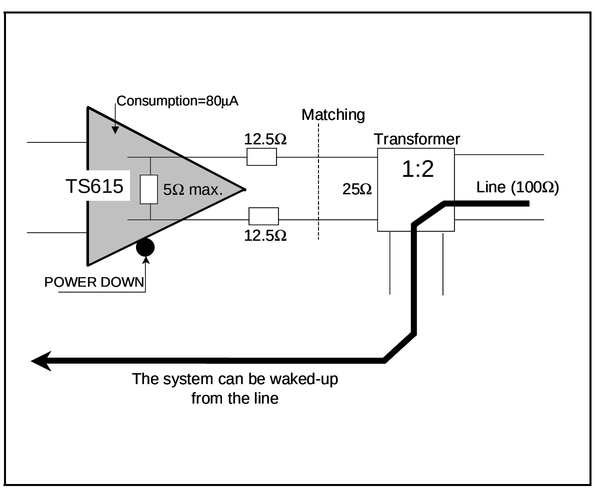


Figure 68 : Standby Mode. Time On>Off

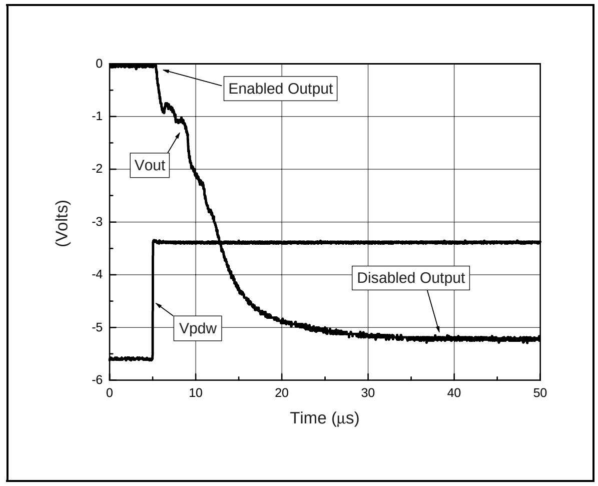


Figure 69 : Standby Mode. Time Off>On

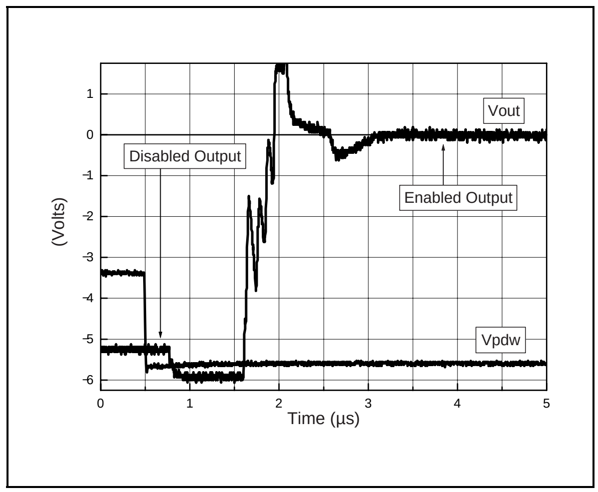
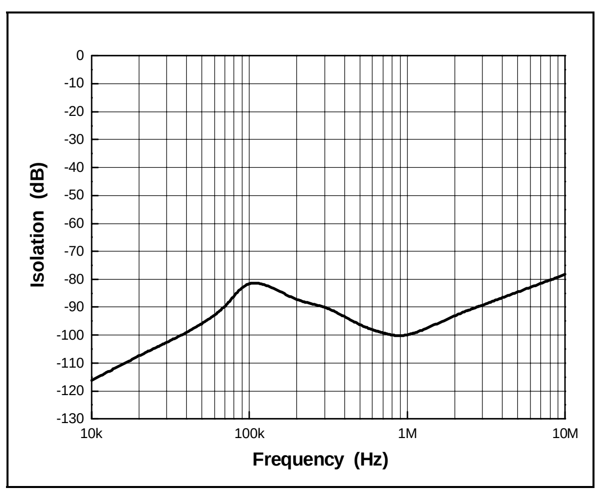


Figure 70 : Standby Mode. Input/Output Isolation vs. Frequency

$A_V=+4$, $R_{fb}=620\Omega$, $V_{CC}=\pm6V$, Vout=3Vp



CHOICE OF THE FEEDBACK CIRCUIT

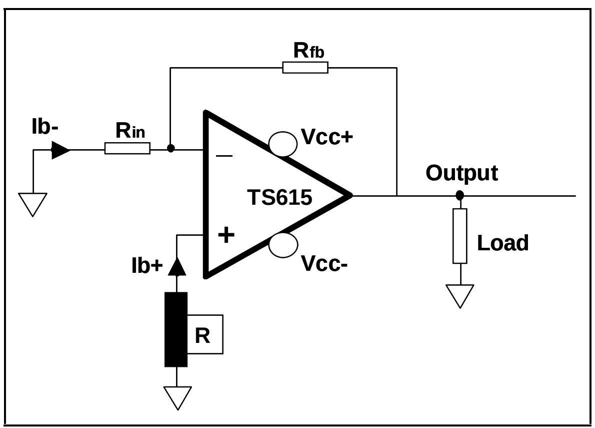
Table 71 : Closed-Loop Gain - Feedback Components

V_{CC} (V)	Gain	R_{fb} (Ω)
±6	+1	750
	+2	680
	+4	620
	+8	510
	-1	680
	-2	680
	-4	620
	-8	510
±2.5	+1	1.1k
	+2	1k
	+4	910
	+8	680
	-1	1k
	-2	1k
	-4	910
	-8	680

INVERTING AMPLIFIER BIASING

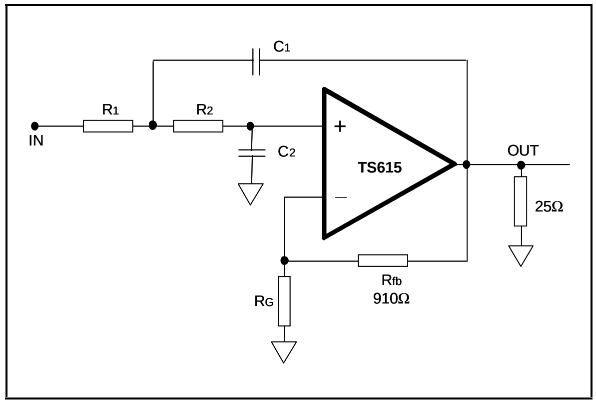
In this case a resistance is necessary to achieve a good input biasing, as R on (fig.30).
This resistance is calculated by assuming the negative and positive input bias current. The aim is to make the compensation of the offset bias current which could affect the input offset voltage and the output DC component. Assuming Ib-, Ib+, R_{in}, R_{fb} and a zero volt output, the resistance R comes: R = R_{in} // R_{fb} .

Figure 72 : Compensation of the Input Bias Current



ACTIVE FILTERING

Figure 73 : Low-Pass Active Filtering. Sallen-Key



The resistors R_{fb} and R_G give directly the gain of the filter as a classical non-inverting amplification configuration :

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

Assuming the following expression as the response of the system:

$$T_{j\omega} = \frac{Vout_{j\omega}}{Vin_{j\omega}} = \frac{g}{1 + 2\zeta\frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^{\ 2}}}$$

the cutoff frequency is not gain dependent and it comes:

$$\omega_c = \frac{1}{\sqrt{R1R2C1C2}}$$

the damping factor comes:

$$\zeta = \frac{1}{2}\omega_c(C_1R_1 + C_1R_2 + C_2R_1 - C_1R_1g)$$

The higher the gain the more sensitive the damping factor is. When the gain is higher than 1 it is preferable to use some very stable resistors and capacitors values.

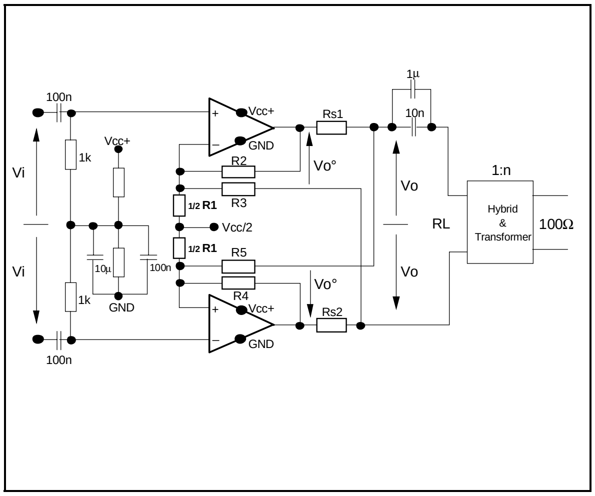
In the case of R1=R2:

$$\zeta = \frac{2C_2 - C_1\frac{R_{fb}}{R_g}}{2\sqrt{C_1C_2}}$$

INCREASING THE LINE LEVEL BY USING AN ACTIVE IMPEDANCE MATCHING

With a passive matching, the output signal amplitude of the driver must be twice the amplitude on the load. To go beyond this limitation an active matching impedance can be used. With this technique, it is possible to keep a good impedance matching with an amplitude on the load higher than the half of the output driver amplitude. This concept is shown in figure 74 for a differential line.

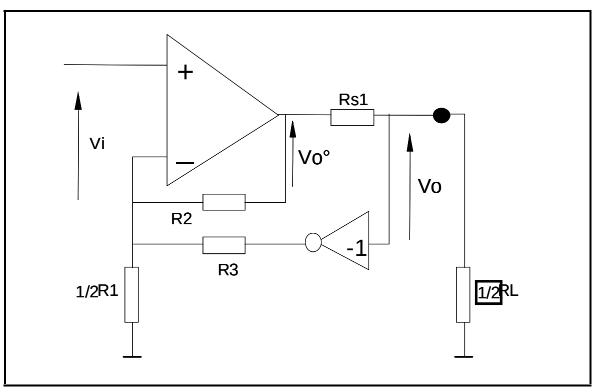
Figure 74 : TS615 as a differential line driver with an active impedance matching



Component Calculation

Let us consider the equivalent circuit for a single ended configuration, Figure75.

Figure 75 : Single ended equivalent circuit



Let us consider the unloaded system. Assuming the currents through R1, R2 and R3

as respectively:

$$\frac{2Vi}{R1},\ \frac{(Vi-Vo°)}{R2} \text{ and } \frac{(Vi+Vo)}{R3}$$

As Vo° equals Vo without load, the gain in this case becomes :

$$G = \frac{Vo(noload)}{Vi} = \frac{1+\frac{2R2}{R1}+\frac{R2}{R3}}{1-\frac{R2}{R3}}$$

The gain, for the loaded system will be (eq1):

$$GL = \frac{Vo(withload)}{Vi} = \frac{1}{2}\frac{1+\frac{2R2}{R1}+\frac{R2}{R3}}{1-\frac{R2}{R3}},(eq1)$$

As shown in figure76, this system is an ideal generator with a synthesized impedance as the internal impedance of the system. From this, the output voltage becomes:

$$Vo = (ViG)-(RoIout),(eq2)$$

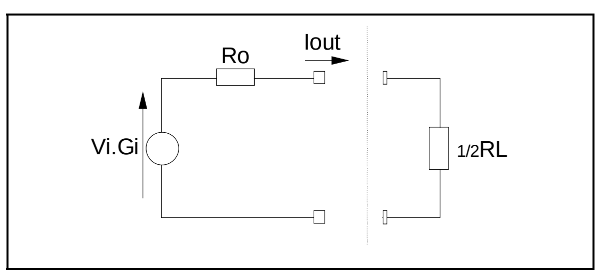
with Ro the synthesized impedance and Iout the output current. On the other hand Vo can be expressed as:

$$Vo = \frac{Vi\left(1+\frac{2R2}{R1}+\frac{R2}{R3}\right)}{1-\frac{R2}{R3}} - \frac{Rs1Iout}{1-\frac{R2}{R3}},(eq3)$$

By identification of both equations (eq2) and (eq3), the synthesized impedance is, with Rs1=Rs2=Rs:

$$Ro = \frac{Rs}{1-\frac{R2}{R3}},(eq4)$$

Figure 76 : Equivalent schematic. Ro is the synthesized impedance



Unlike the level Vo° required for a passive impedance, Vo° will be smaller than 2Vo in our case. Let us write Vo°=kVo with k the matching factor varying between 1 and 2. Assuming that the current through R3 is negligible, it comes the following resistance divider:

$$Ro = \frac{kVoRL}{RL + 2Rs1}$$

After choosing the k factor, Rs will equal to

1/2RL(k-1).

A good impedance matching assumes:

$$Ro = \frac{1}{2}RL,(eq5)$$

From (eq4) and (eq5) it becomes:

$$\frac{R2}{R3} = 1 - \frac{2Rs}{RL},(eq6)$$

By fixing an arbitrary value of R2, (eq6) gives:

$$R3 = \frac{R2}{1 - \frac{2Rs}{RL}}$$

Finally, the values of R2 and R3 allow us to extract R1 from (eq1), and it comes:

$$R1 = \frac{2R2}{2\left(1 - \frac{R2}{R3}\right)GL - 1 - \frac{R2}{R3}},(eq7)$$

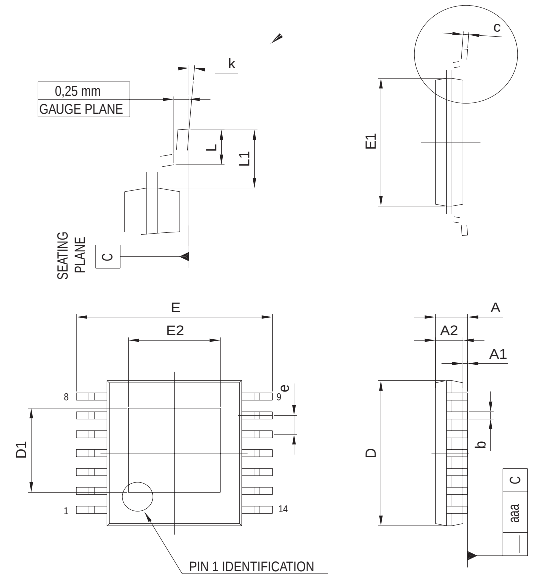
with GL the required gain.

Figure 77 : Components Calculation for Impedance Matching Implementation

GL (gain for the loaded system)	GL is fixed for the application requirements GL=Vo/Vi=0.5(1+2R2/R1+R2/R3)/(1-R2/R3)
R1	2R2/[2(1-R2/R3)GL-1-R2/R3]
R2 (=R4)	Abritrary fixed
R3 (=R5)	R2/(1-Rs/0.5RL)
Rs	0.5RL(k-1)
Load viewed by each driver	kRL/2

PACKAGE MECHANICAL DATA

14 PINS - THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP Exposed-Pad)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.200			0.047
A1			0.150			0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D	4.900	5.000	5.100	0.193	0.197	0.201
D1		3.000			1.18	
E	6.200	6.400	6.600	0.244	0.252	0.260
E1	4.300	4.400	4.500	0.169	0.173	0.177
E2		3.000			1.18	
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0d		8d	0d		8d
aaa			0.100			0.004