



TEA6422

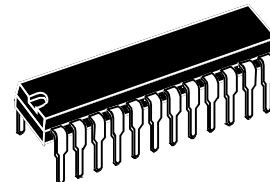
BUS-CONTROLLED AUDIO MATRIX

- 6 Stereo Inputs
- 3 Stereo Outputs
- Gain Control 0 dB/Mute for each Output
- Cascadable (2 different addresses)
- Serial Bus Controlled
- Very Low Noise
- Very Low Distorsion
- Fully ESD Protected
- Wide Audio Dynamic Range ($3 V_{RMS}$)

DESCRIPTION

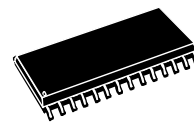
The TEA6422 switches 6 stereo audio inputs on 3 stereo outputs.

All the switching possibilities are changed through the I²C BUS.



SHRINK DIP24
(Shrink Plastic Package)

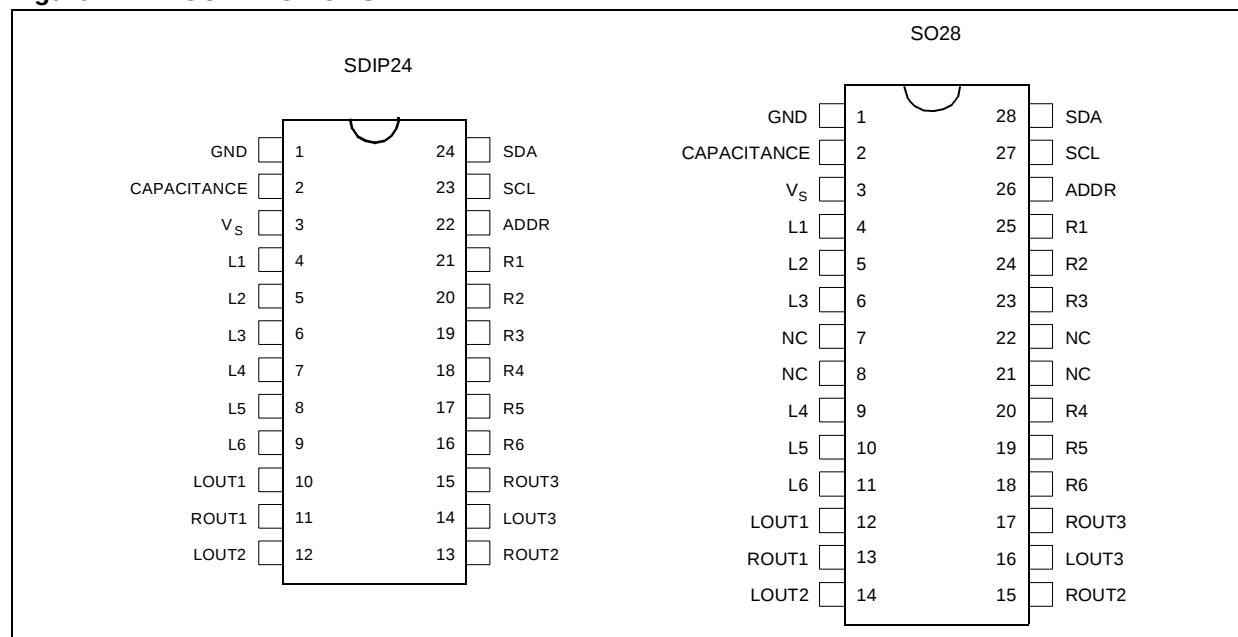
ORDER CODE: TEA6422



SO28
(Plastic Monopackage)

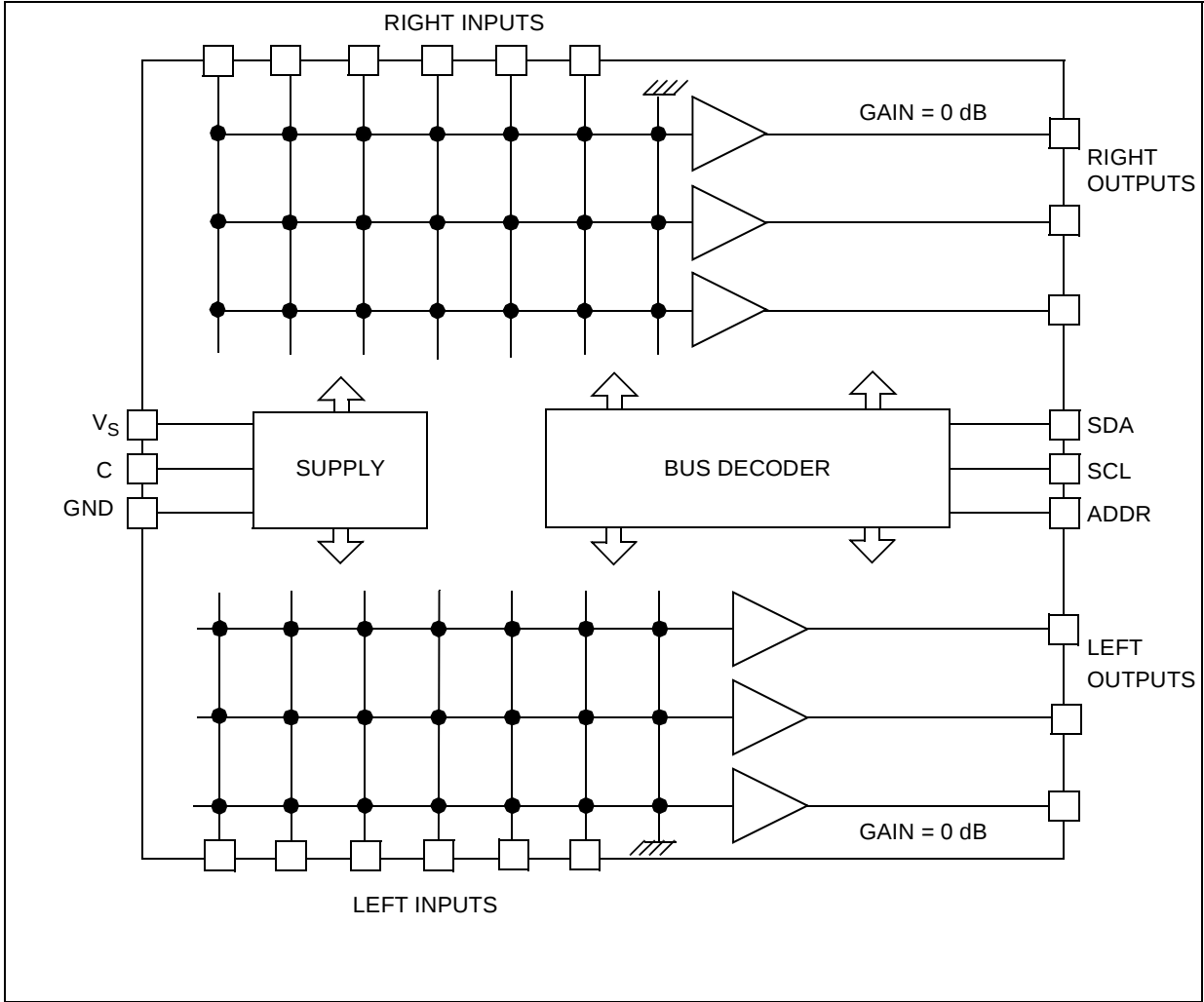
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Figure 1. PIN CONNECTIONS



TEA6422

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	12	V
T _{oper}	Operating Temperature	0, + 70	°C
T _{stg}	Storage Temperature	- 20, + 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th(j-a)}	Junction - ambient Thermal Resistance	SDIP24	75 °C/W
		SO28	75 °C/W

ELECTRICAL CHARACTERISTICS

$T_A = 25\text{ }^{\circ}\text{C}$, $V_S = 9\text{ V}$, $R_L = 10\text{ k}\Omega$, $R_G = 600\text{ }\Omega$, $f = 1\text{ kHz}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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SUPPLY

V_S	Supply Voltage		8	10	11	V
I_S	Supply Current			3	8	mA
SVR	Ripple Rejection	$V_{IN} = 500\text{mV}_{\text{RMS}}$, $f = 1\text{kHz}$	70	80		dB

MATRIX

V_{IN}	Input DC Level			$V_{CC}/2$		V
R_I	Input Resistance		30	50	100	$\text{k}\Omega$
C_S	Channel Separation	$V_{IN} = 2V_{\text{RMS}}$, $f = 1\text{kHz}$	80	90		dB

OUTPUT BUFFER

V_{OUT}	Output DC Level			$V_{CC}/2$		V
R_{OUT}	Output Resistance			50	100	Ω
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		μV
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1V_{\text{RMS}}$		110		dB
G	Gain		-1	0	+ 1	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{\text{RMS}}$		0.01	0.05	%
V_{CL}	Clipping Level	$d = 0.3\%$, $V_S = 10\text{ V}$	2.8	3		V_{RMS}
R_L	Output Load Resistance		2			$\text{k}\Omega$

I²C BUS CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
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SCL

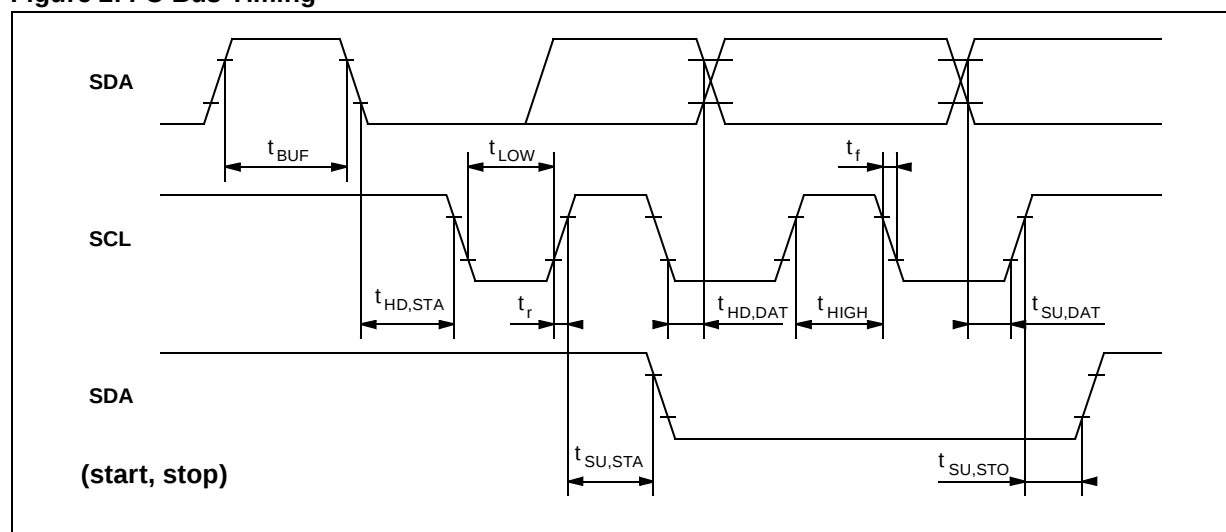
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	$V_{CC} + 0.5$	V
I_{LI}	Input Leakage Current	$V_I = 0 \text{ to } V_{CC}$	- 10	+ 10	μA
f_{SCL}	Clock Frequency		0	100	kHz
t_R	Input Rise Time	1.5V to 3V		1000	ns
t_F	Input Fall Time	3V to 1.5V		300	ns
C_I	Input Capacitance			10	pF

SDA

V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	$V_{CC} + 0.5$	V
I_{LI}	Input Leakage Current	$V_I = 0 \text{ to } V_{CC}$	- 10	+ 10	μA
C_I	Input Capacitance			10	pF
t_R	Input Rise Time	1.5V to 3V		1000	ns
t_F	Input Fall Time	3V to 1.5V		300	ns
V_{OL}	Low Level Output Voltage	$I_{OL} = 3\text{mA}$		0.4	V
t_F	Output Fall Time	3V to 1.5V		250	ns
C_L	Load Capacitance			400	pF

TIMING

t_{LOW}	Clock Low Period		4.7		μs
t_{HIGH}	Clock High Period		4.0		μs
$t_{SU, DAT}$	Data Set-up Time		250		ns
$t_{HD, DAT}$	Data Hold Time		0	340	ns
$t_{SU, STO}$	Set-up Time from Clock High to Stop		4.0		μs
t_{BUF}	Start Set-up Time following a Stop		4.7		μs
$t_{HD, STA}$	Start Hold Time		4.0		μs
$t_{SU, STA}$	Start Set-up Time following Clock Low-to High Transition		4.7		μs

Figure 2. I²C Bus Timing

POWER ON RESET

After power-on reset all outputs are in mute mode

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset	Start of Reset	Incr. V_{CC}			2.5	V
		Decr. V_{CC}			4.2	V
	End of Reset	Incr. V_{CC}	4.5			V

SOFTWARE SPECIFICATION**1. Chip address**

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

2. Data bytes

Output select

X	0	0	X	X	I_2	I_1	I_0	Output 1
	0	1						Output 2
	1	0						Output 3

Input select

X	Q_1	Q_0	X	X	0	0	0	Input 1
					0	0	1	Input 2
					0	1	0	Input 3
					0	1	1	Input 4
					1	0	0	Input 5
					1	0	1	Input 6
					1	1	0	Mute

X = don't care - MSB is transmitted first

Example : 010XX100 connects output 3 with input 5.

Figure 3. Distorsion Level versus Input Voltage

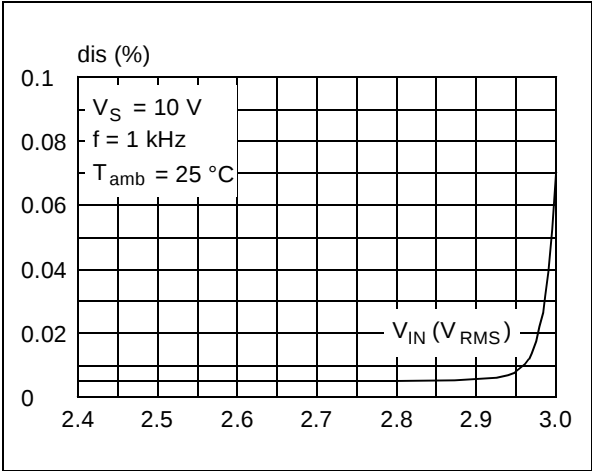


Figure 4. Supply Voltage Rejection versus Frequency ($V_{IN} = 500\text{ mV}_{RMS}$)

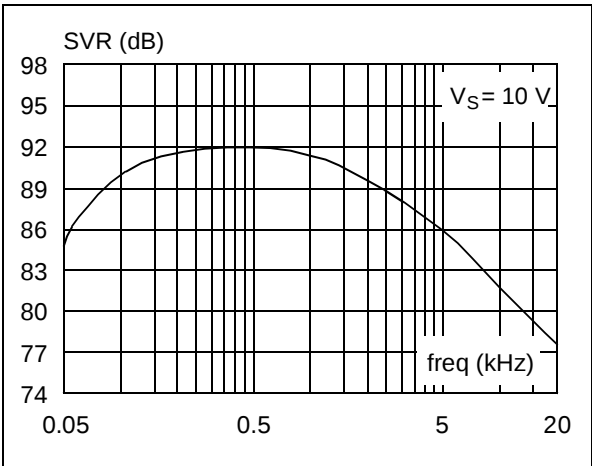
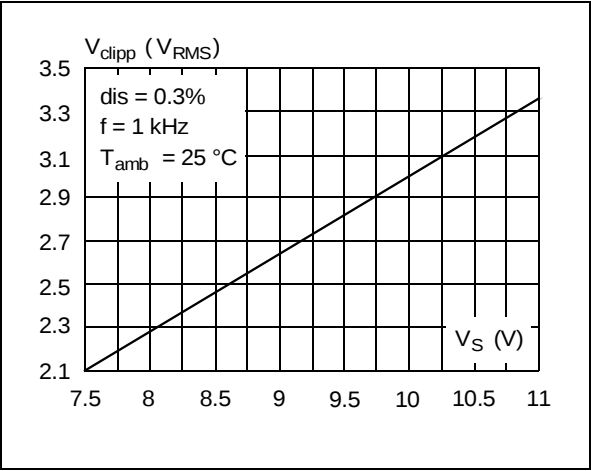


Figure 5. Clipping Level versus Supply Voltage



PIN CONFIGURATIONS (SDIP24 Package)

Figure 6. Audio IN

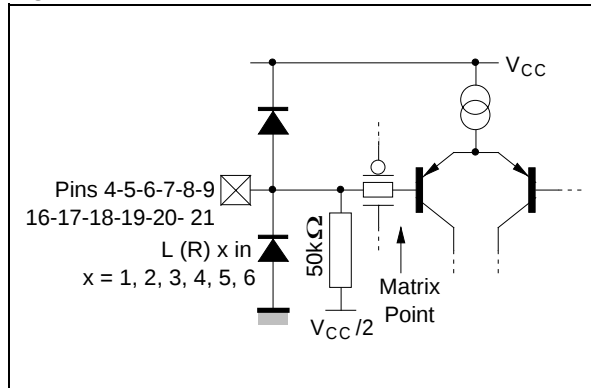


Figure 8. Audio OUT

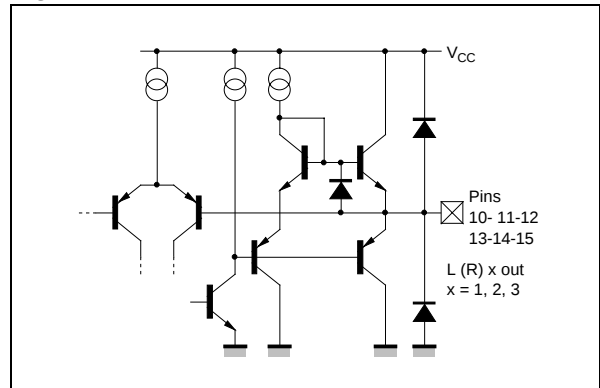


Figure 7. ADDR

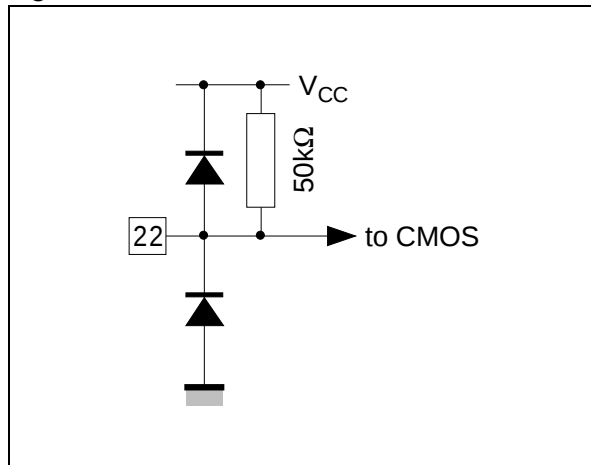


Figure 9. Bus Inputs (SDA, SCL)

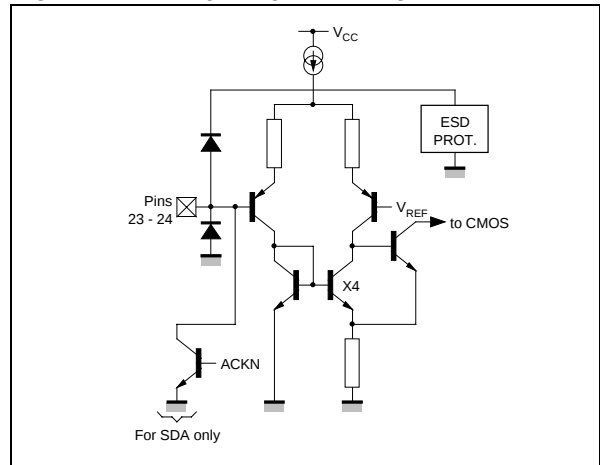
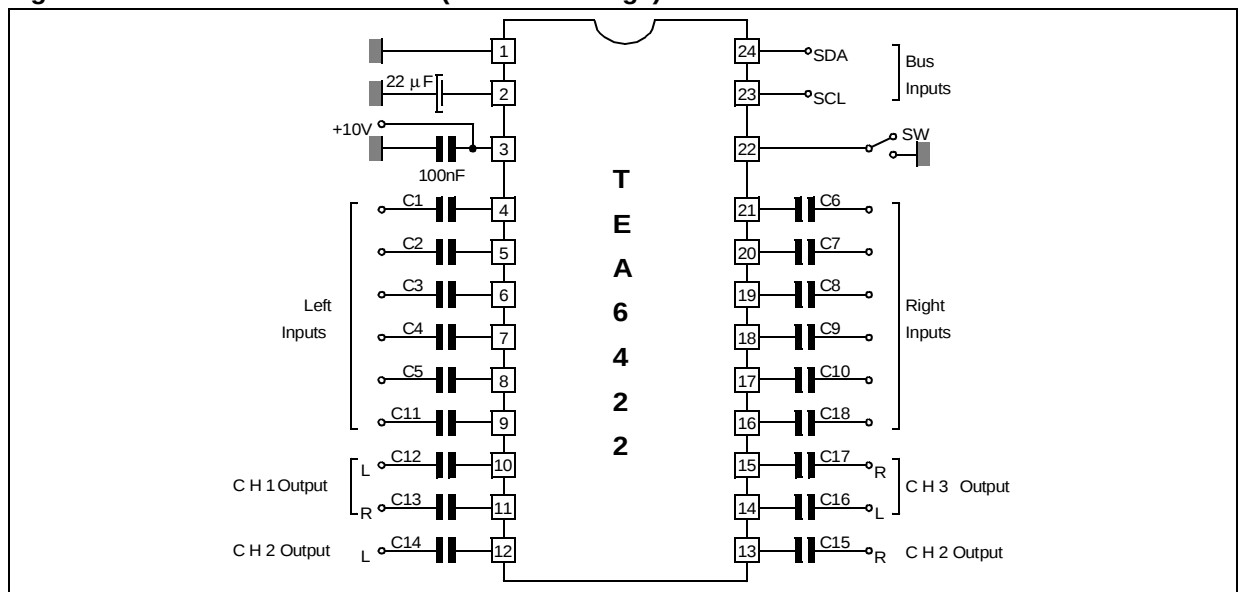


Figure 10. TYPICAL APPLICATION (SDIP24 Package)

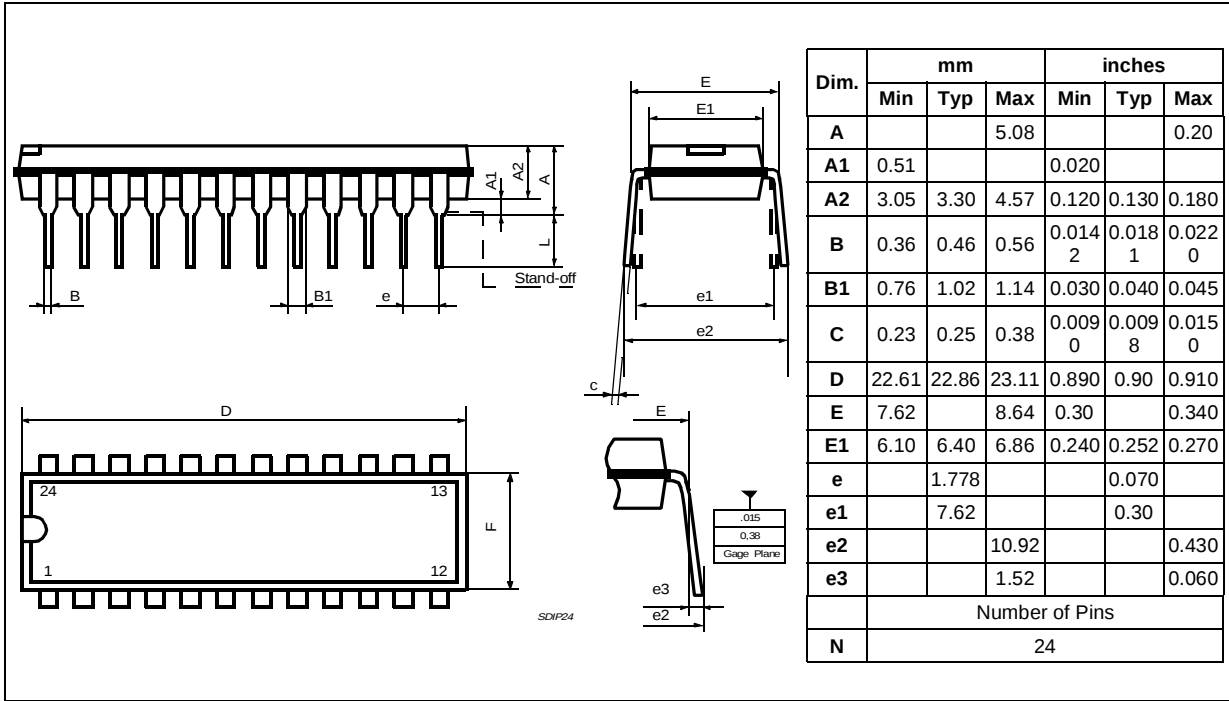


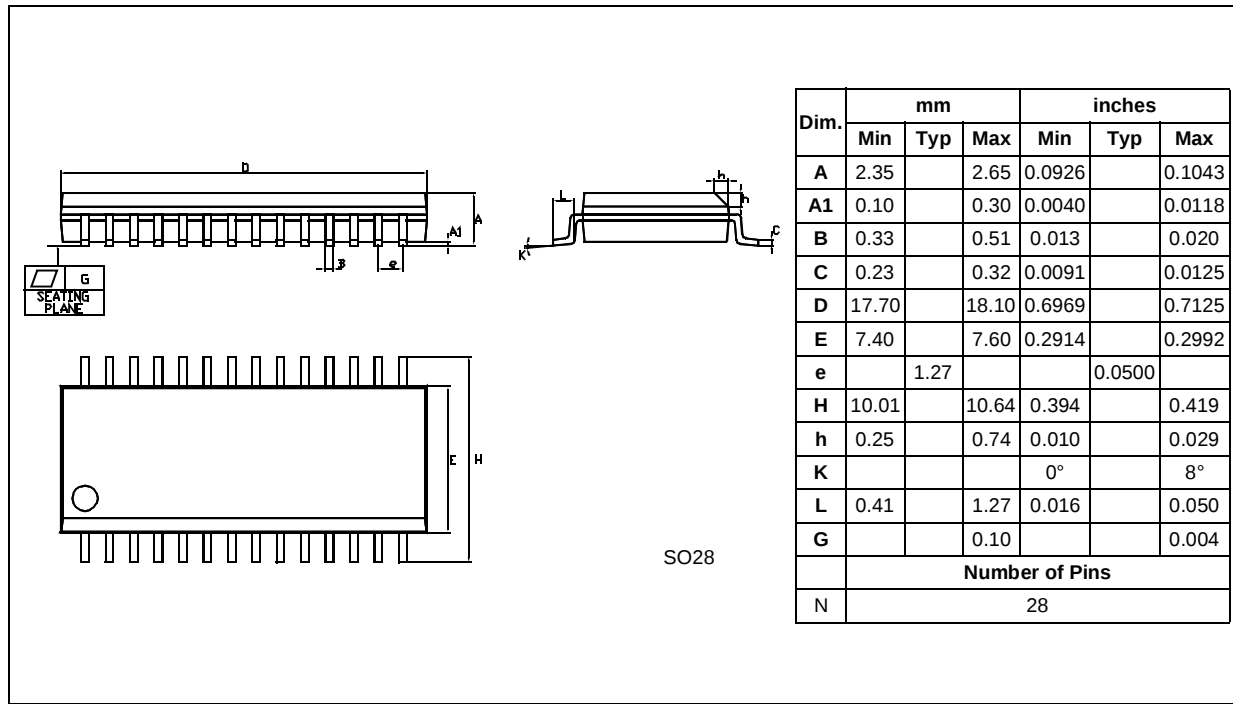
TEA6422

PACKAGE MECHANICAL DATA

24 PINS - PLASTIC SHRINK

Figure 11. 24-Pin Shrink Plastic Dual In Line Package



PACKAGE MECHANICAL DATA**28 PINS - PLASTIC MICROPACKAGE****Figure 12. 28-Pin Plastic Small Outline Package, 300-mil Width**

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