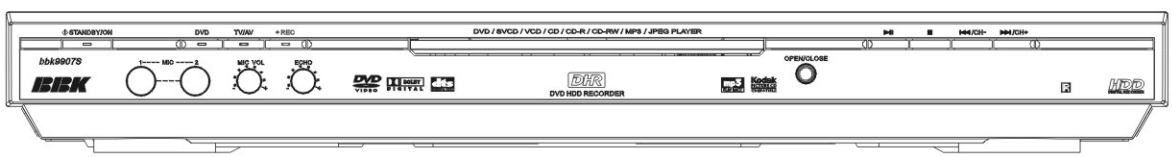
SERVICE MANUAL

bbk9907S



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PREFACE

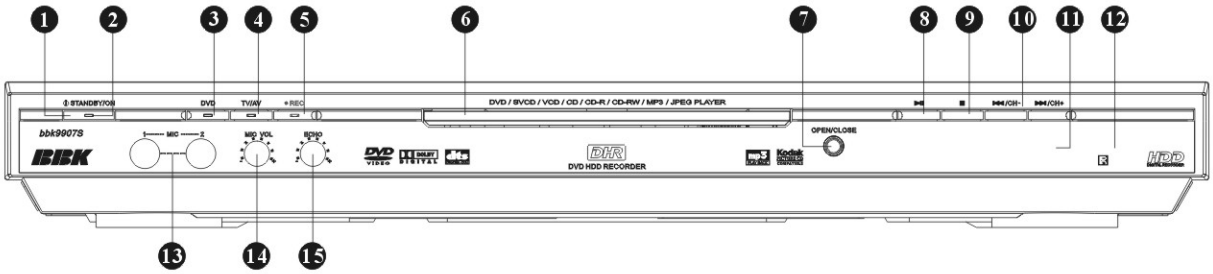
INTRODUCTION

This player has the functions of playing DVD, TV playback and HDD recording. You can play several kinds of discs and record your favourite contents onto HDD. The tuner is set inside the player, so you can watch TV programs when you connect the CATV cable. The time shift function ensures that you will not miss any wonderful program. You can realize TV playback function through FORWARD, BACKWARD, SLOW and PAUSE operation to the time-shifted programs; meanwhile you can record this time-shifted program onto HDD. The timing record function also ensures that you will not miss any wonderful program. As long as you set the beginning time, length and quality grade of the recording, the player will automatically start to record your scheduled programs. Certainly you can also watch and record AV source signal from VCR, VCD, digital camera and digital video camera through AV or S-Video terminal. The advanced picture in picture function can also make you monitor TV and AV programs when watching DVD discs. The player also has MP3 music and JPEG picture copy functions to facilitate you in making characteristic personal AV storeroom.

FEATURES

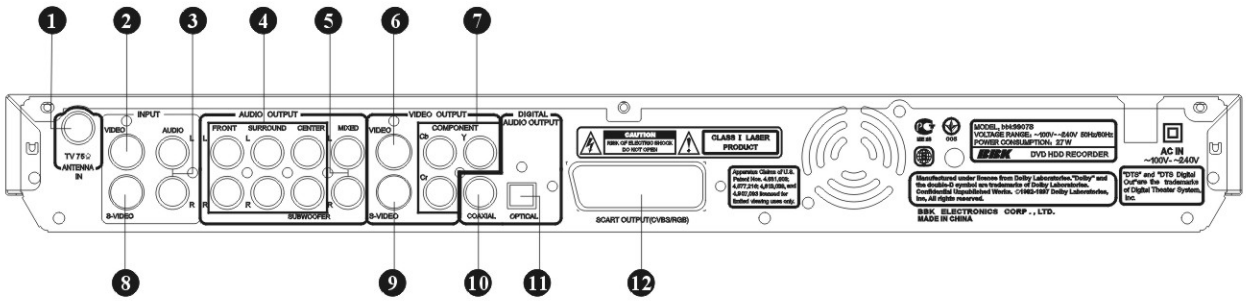
- Powerful function of digital video VCR
  - 40G-capacity built-in hard disc enables a recording of nearly 30 hours.
  - MPEG-II real time digital encoding technology is adopted in the high quality video recording, and it supports 4 recording modes with DVD quality as the maximum.
  - The unique time shifting function is able to realize several functions as to TV program and external input signal, such as pause, fast forward, fast backward, and slow playback, which will last for as long as 2 hours.
  - **Press and Record, Press and Stop video recording modes.**
  - Intelligent appointment timer recording function supports varied groups of video recording in different time periods, and you will not miss any excellence.
  - It is able to record TV program or external AV signal while you are watching DVD program or the recorded program. You may also record the disc onto the hard disc.
  - The advanced picture in picture function will enable you to monitor TV programs or the external AV signal while you are watching DVD program.
  - A powerful management function for recorded programs will enable you to preview, play, delete, lock, or name the recorded program as you like.
  - With the TV Tuner/AV/S-Video input terminal, it is convenient to record any program sources such as the signal from CATV/Disc Player/Video camera.
  - Built-in TV Tuner enables auto-searching, manual searching, fine-tuning,channel naming, moving, skipping, deleting and other functions.
  - A powerful hard disc management function can realize such operations as scanning, and formatting.
  - The updated MP3 and JPEG copying function will store your favorite MP3 music and JPEG picture onto the hard disc.
- Complete function of DVD player
  - It can play DVD, SVCD, VCD, CD-DA, MP3, CD-R (in audio or video format), CD-RW (in audio or video format), HDCD, Kodak PICTURE CD and other formats of discs.
  - Built-in 5.1CH Dolby digital surround sound decoder, independent Dolby 5.1-channel output, 2-channel output, optical and coaxial digit audio output.
  - SCART output, Composite video output, S terminal output, YCbCr output.
  - Multi angle, multi subtitle, multi language, multi picture proportions, focus alteration, Russian/ English OSD.
  - It supports varied searching methods such as title, chapter, time, track, etc.
  - PAL/NTSC recording and output selections.
  - A super wide scope of working voltage (~100V-~240V, 50/60HZ), and a super low standby power consumption (the standby power consumption ≤1W).
  - Karaoke function.

FRONT PANEL



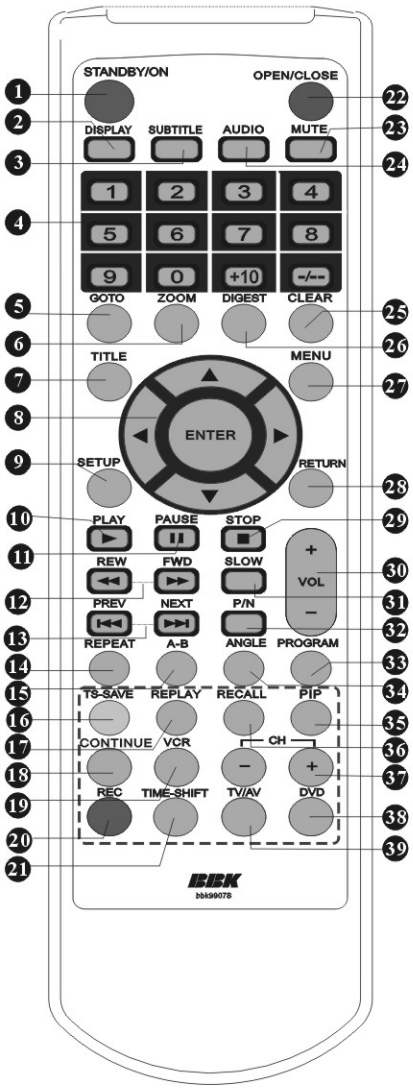
1. Standby/On button
   Switch between standby and working modes
2. Standby Indicator Light
   Red light is off while working, and on while in standby mode.
3. DVD Function button
   Switch to DVD working mode
4. TV/AV Function button
   Switch in TV/AV/S terminal working mode
5. REC button
   Player will start recording after pressing
6. DISC Tray
   Put a disc in the tray with the mark upward
7. Open/Close button
   Open/close the tray
8. Play/Pause button
   Switch between play and pause
9. Stop button
   Stop playing or recording or time shifting after pressing
10. Next/Prev,CH+/CH- button
    Selecting between the up and down tracks/chapters or channels
11. VFD
    Display the current working condition
12. Infrared Sensor
13. MIC INPUT
    Microphone input
14. MIC VOL
    Control microphone volume
15. ECHO
    Control the echo level of microphone

REAR PANEL



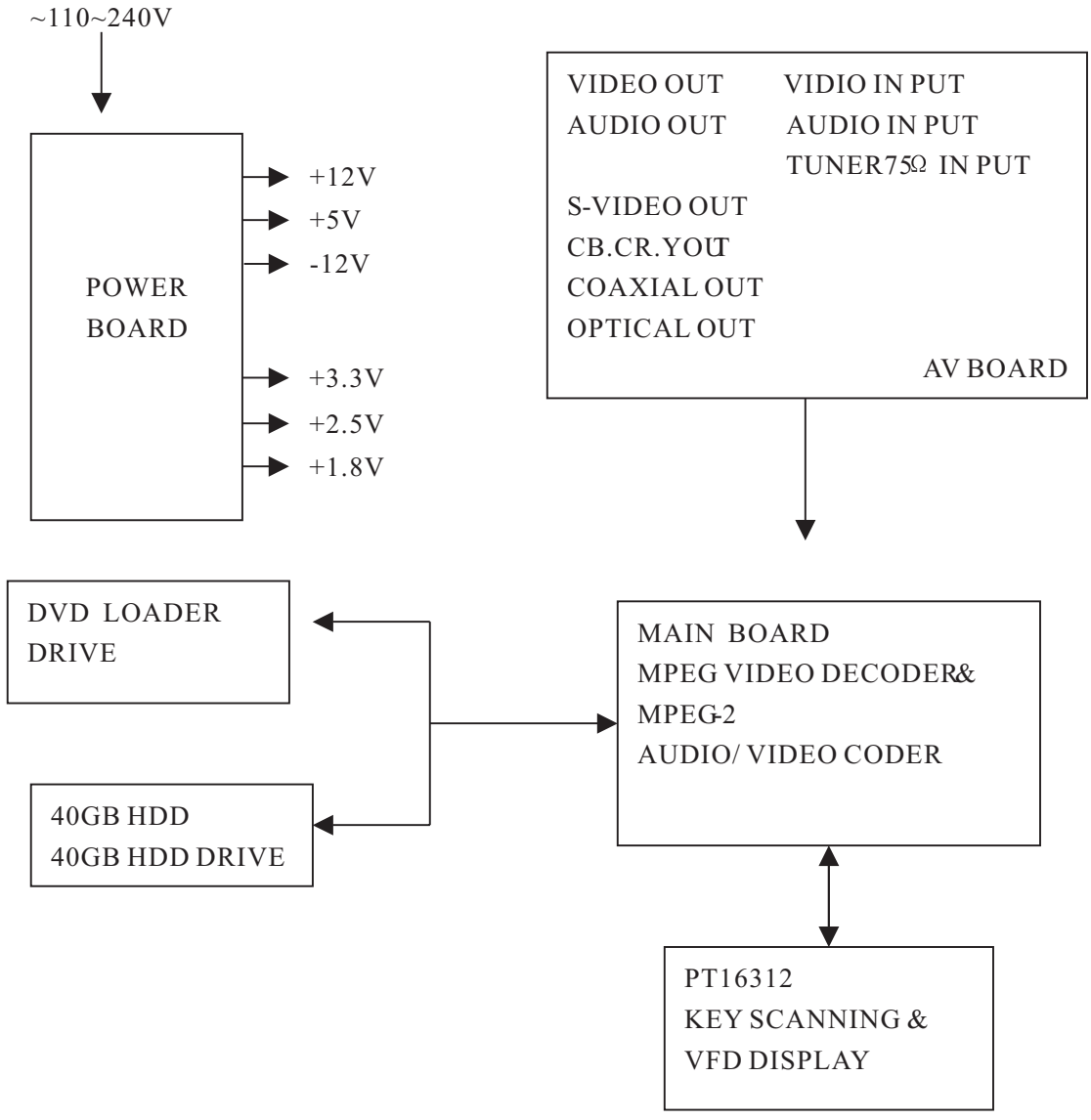
1. TV TUNER input terminal
2. COMPOSITE VIDEO input terminal
3. AUDIO input terminal
4. 5.1CH AUDIO output terminals
5. MIXED AUDIO output terminals
6. COMPOSITE VIDEO output terminal
7. COMPONENT VIDEO output terminals
8. S-VIDEO input terminal
9. S-VIDEO output terminal
10. COAXIAL output terminal for digital audio
11. OPTICAL output terminal for digital audio
12. SCART output terminal for audio and video

BUTTONS ON THE REMOTE CONTROL

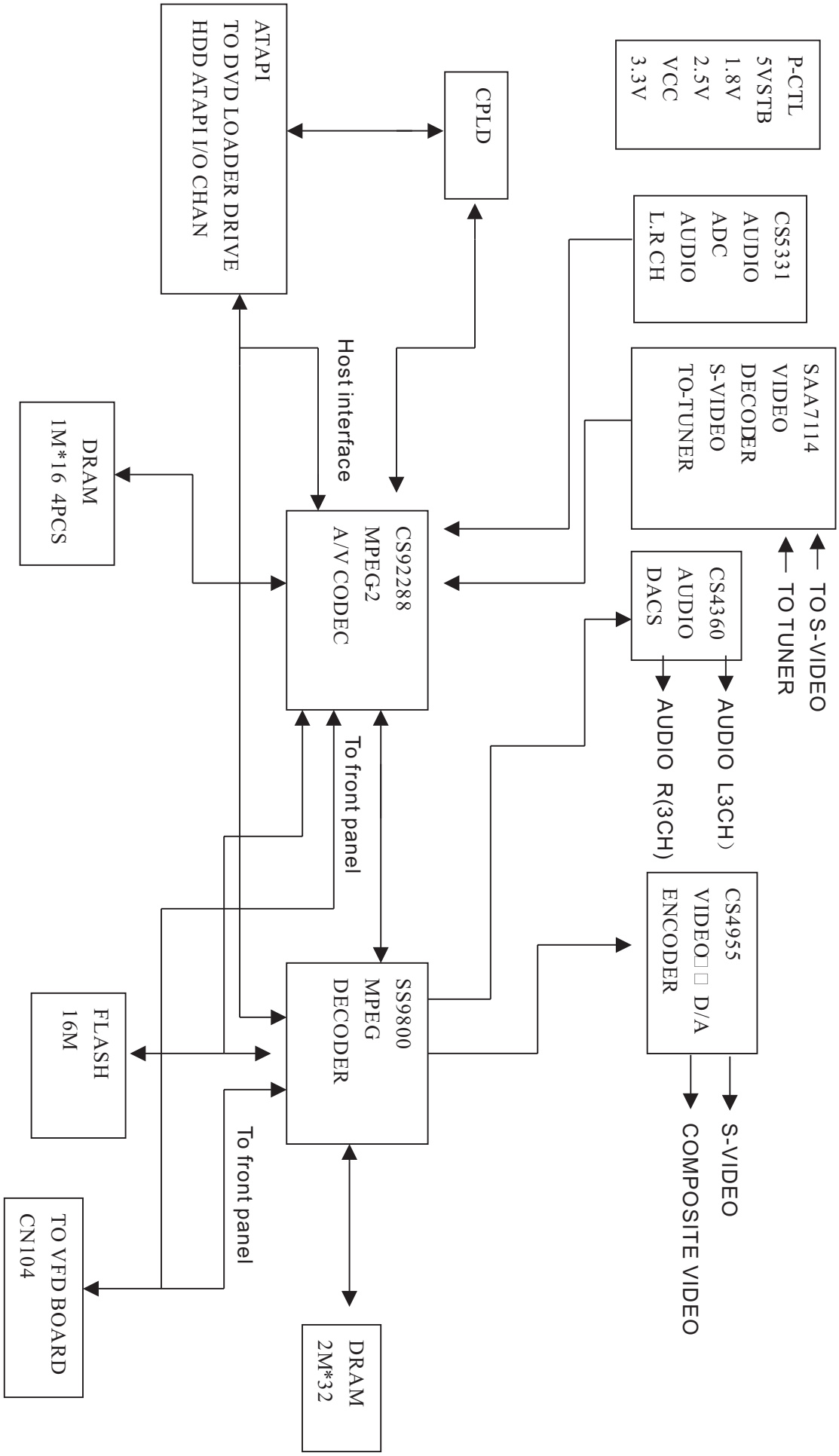


1. [STANDBY/ON] button
   Switch between standby and working condition.
2. [DISPLAY] button
   Open/close the screen display
3. [SUBTITLE] button
   Select subtitle languages
4. [NUMBER] button
   Used to input numbers
5. [GOTO] button
   Search specified time/track/title/chapter
6. [ZOOM] button
   Amplify/restore the current picture
7. [TITLE] button
   Display the title of the disc. Users will be allowed to select specified segment after activating.
8. [CURSOR] button
   Used to select the direction of OSD picture
9. [SETUP] button
   Open the setup menu
10. [PLAY] button
    Play
11. [PAUSE] button
    Pause
12. [REW]/[FWD] button
    Fast backward/fast forward playback
13. [PREV]/[NEXT] button
    Return to the last track/chapter, or advance to the next track/chapter
14. [REPEAT] button
    Repeat playback
15. [A-B] button
    Repeat the specified segment (A-B)
16. [TS-SAVE]button
    Store the buffered time-shifted program
17. [REPLAY] button
    Play from 5 seconds ago
18. [CONTINUE] button
    After pressing REC key and starting recording, this key can be used to set how long it will last before it stops and whether the player stops automatically after recording finishes.(Refer to page29)
19. [VCR] button
    Enter or exit from the reception condition of the video magnetic tape program (Refer to page 30)
20. [REC] button
    Start recording
21. [TIME-SHIFT] button
    Buffering the current program
22. [OPEN/CLOSE] button
    Open/Close the tray
23. [MUTE] button
    Stop/Restore the sound output
24. [AUDIO] button
    Switch the sound channels
25. [CLEAR] button
    Used to delete MP3 file or JPEG file or timer-recording plan.
26. [DIGEST] button
    Used to preview nine pictures
27. [MENU] button
    When VCD2.0 disc is played, it is used to switch between ON or OFF of the menu. When DVD disc is played, it is used to return to the root directory.
28. [RETURN] button
    Return to the upper menu
29. [STOP] button
    Stop playing or time shifting or recording
30. [VOL+/-] button
    Tuning the sound volume
31. [SLOW] button
    Play in a slow speed
32. [P/N]button
    PAL/NTSC system switch
33. [PROGRAM] button
    In TV/AV/S terminal mode, press PROGRAM key to show the recorded programs in the hard disc for selection.
34. [ANGLE] button
    Changing the viewing angle
35. [PIP] button
    Please refer to PICTURE IN PICTURE FUNCTION in page 39
36. [RECALL] button
    Skip to the previous channel
37. [CH+/-] button
    Switch TV channels
38. [DVD] button
    Switch to DVD mode
39. [TV/AV] button
    Switch in TV/AV/S terminal modes

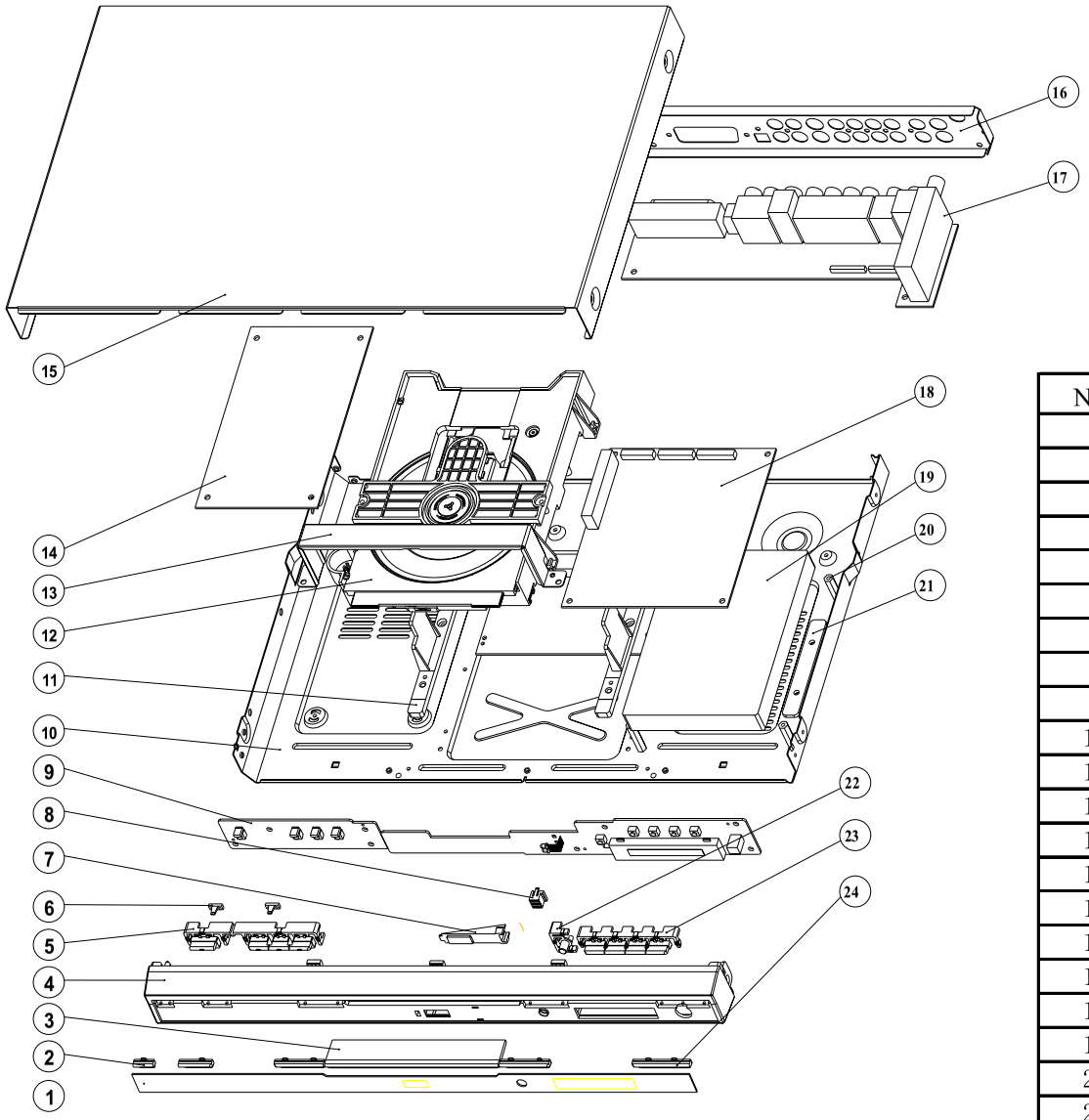
BLOCK DIAGRAM



SCHEMATIC DIAGRAM

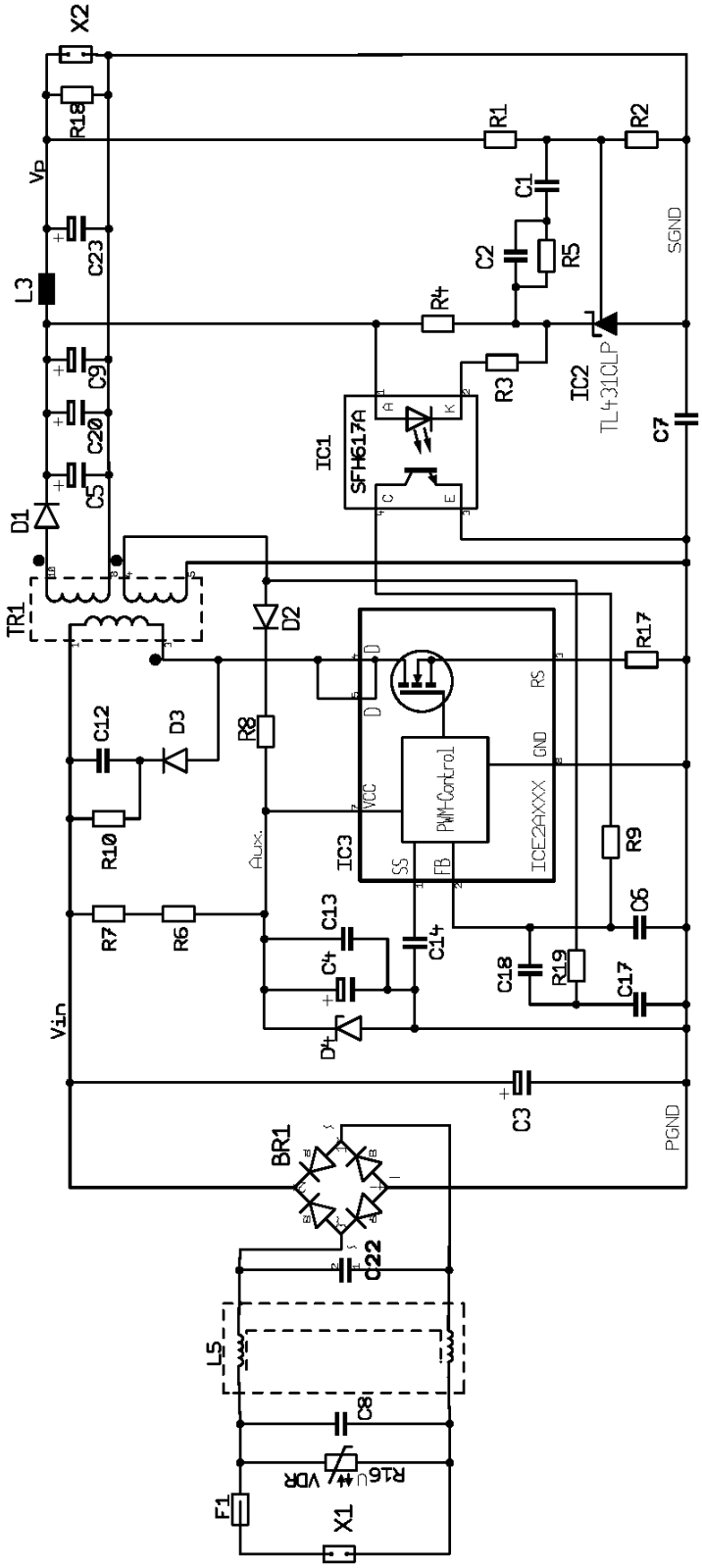


EXPLODED VIEW



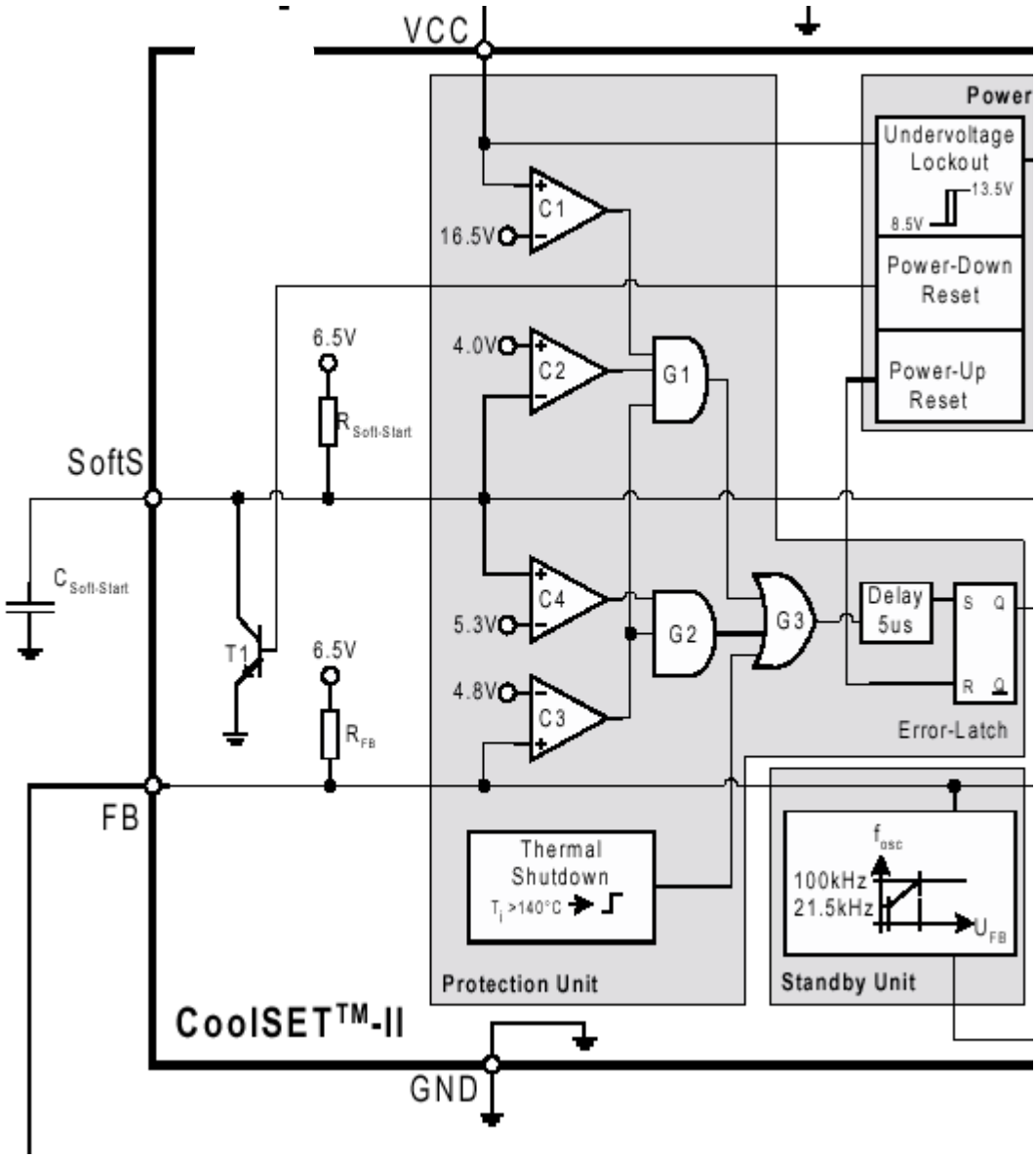
NO.	ITEM NAME	MATERIAL	QUANTITY
1	Mirror bar	pc	1
2	Left decorative bar	ABS	3
3	Tray door	ABS	1
4	Front panel	ABS	1
5	Left four-key button	ABS	1
6	Small light conductor	PMMA	4
7	Big light conductor	PMMA	1
8	LED stander	PS	1
9	VFD driver board		1
10	Chasis	SECC	1
11	Loader mechanism	PS	1
12	DVD loader		1
13	Iron stand	SECC	1
14	Power board		1
15	Top cover	SECC	1
16	Rear panel	SECC	1
17	AV board		1
18	Main board		1
19	Hard disc		1
20	Copper column		4
21	Rubber pad	RUBBER	2
22	Open/close button	ABS	1
23	Right four-key button	ABS	1
24	Right decorative bar	ABS	1

Circuit Diagram: ***ICE2AXXX for OFF ¨C Line Switch Mode Power Supplies***



Protection Functions

The block diagram displayed in Fig. 4 shows the interal functions of the protection unit. The comparators C1, C2, C3 and C4 compare the soft-start and feedback-pin voltages. Logic gates connected to the comparator outputs ensure the combination of the signals and enables the setting of the “Error-Latch”.



Overload and Open-Loop Protection

- Feedback voltage **(VFB)** exceeds 4.8V and soft start voltage **(VSS)** is above 5.3V (soft start is completed) **(t1)**
- After a 5µs delay the **CoolMOS** is switched off **(t2)**
- Voltage at Vcc – Pin **(VCC)** decreases to 8.5V **(t2)**
- Control logic is switched off **(t3)**
- Start-up resistor charges Vcc capacitor **(t3)**
- Operation starts again with soft start after Vcc voltage has exceeded 13.5V **(t4)**

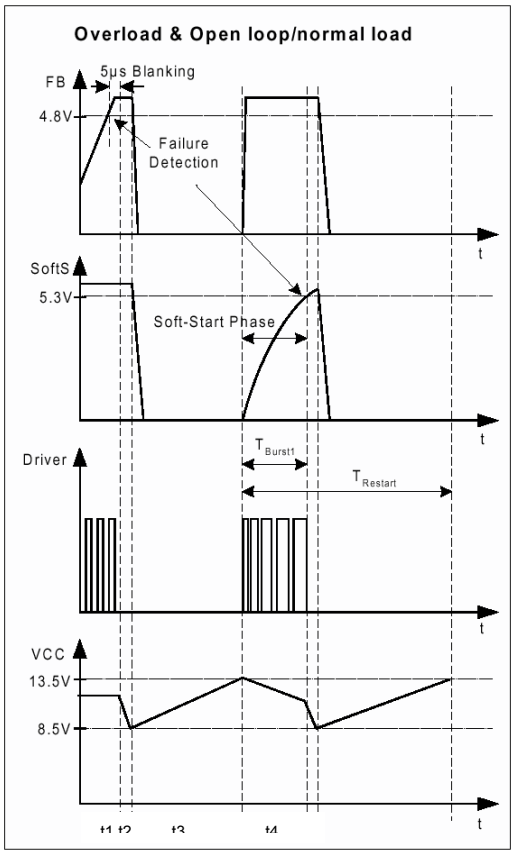


Fig. 6

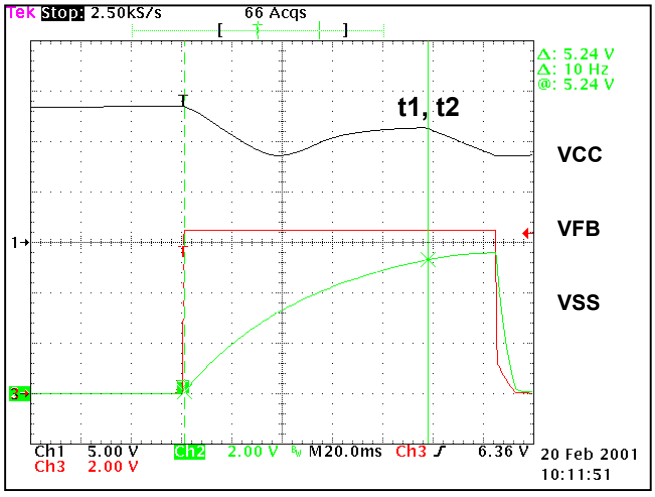
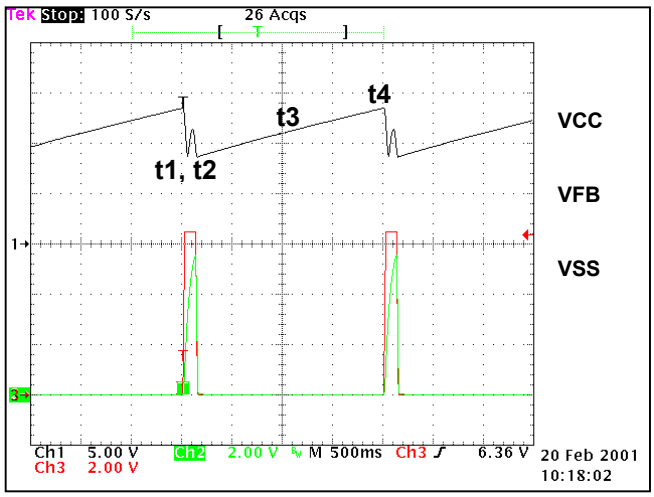


Fig. 7



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[4] **Herfurth Michael,**
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[5] **Herfurth Michael,**
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[6] **Infineon Technologies,** *Datasheet,*
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Off – Line SMPS Current Mode Controller with 650V/800V ***CoolMOS™*** *on Board,*

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Fundamentals of Power Electronics

CS98000

Internet DVD (iDVD) Chip Solution

Features

- Powerful Dual 32-bit RISCs >160MIPS
- Software based on popular RTOS, C/C++
- MPEG video decoder supports DVD, VCD, VCD 3.0, SVCD standards
- Video input with picture-in-picture & zoom
- 8-bit multi-region OSD w/vertical flicker filter
- Universal subpicture unit for DVD and SVCD
- PAL<->NTSC Scaling ~ Transcoding
- Supports SDRAM and FLASH memories
- Powerful 32-bit Audio DSP >80 MIPS
- Decodes: 5.1 channel AC-3, MPEG Stereo
- Plays MP-3 CDs (a MP-3 CD =12 albums)
- Karaoke echo mix and pitch shift
- Optional 3-D Virtual, bass & treble control
- 8-channel dual-zone PCM output
- IEC-60958/61937 Out: AC-3, DTS, MPEG
- Multi-Mode Serial Audio I/O: I2S & AC-Link
- AV Bus or ATAPI interface or DVD/CD/HD
- GPIO support for all common sub-circuits

Description

Overall the CS98000 Crystal DVD Processor is targeted as a market specific consumer entertainment processor empowering new product classes with the inclusion of a DVD player as a fundamental feature. This integrated circuit when used with all the other Crystal mixed signal data converters, DSPs and high quality factory firmware enables the conception and rapid design of market leading internet age products like:

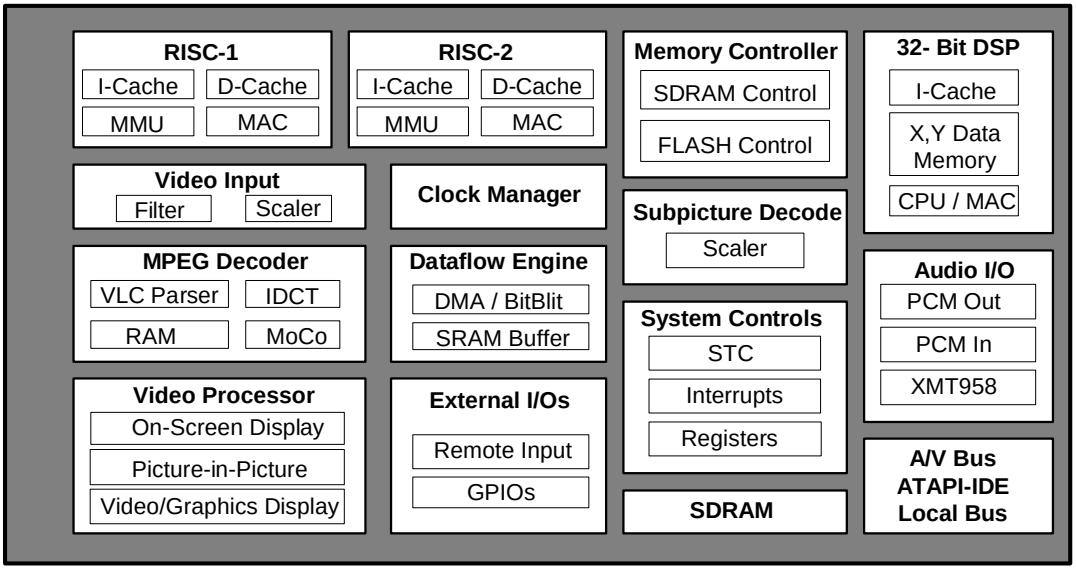
- DVD A/V Mini-System
- Home Media Controller
- Combination DVD Player
- Car/SUV Entertainment Unit

Future Firmware Enhancements:

- Web I/O via AC-Link Input & Built-in Soft Modem
- DVD Audio Navigation
- MLP Decoder, DTS Decoder, AAC Decoder
- MP-3 Encoder, Ripping Controller

ORDERING INFORMATION

CS98000-CQ	0° to 70° C	208-pin
CS98010-CQ	0° to 70° C	128-pin



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

6. PIN DESCRIPTION

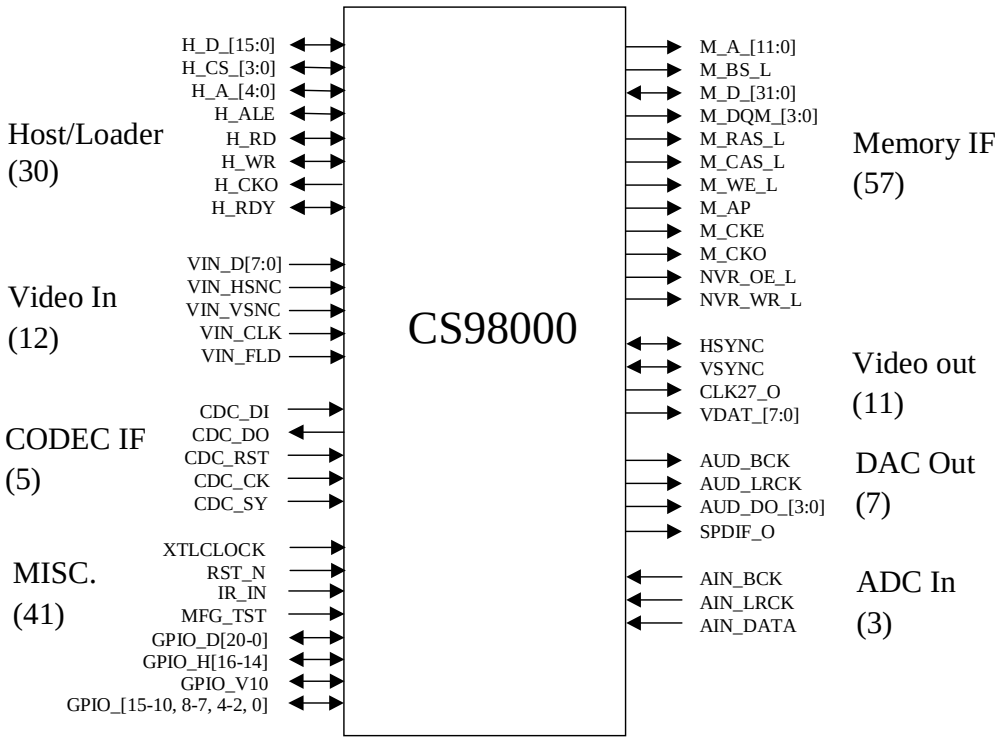


Table 5 lists the conventions used to identify the pin type and direction in the table that follows.

I	Input
IS	Input, with schmitt trigger
ID	Input, with pull down resistor
IU	Input, with pull up resistor
O	Output
O4	Output – 4mA drive
O8	Output – 8mA drive
T4	Tri-State-able Output – 4mA drive
B	Bi-direction
B4	Bi-direction – 4mA drive
B4U	Bi-direction – 4mA drive, with pull-up
B8U	Bi-direction – 8mA drive, with pull-up
B4S	Bi-direction – 4mA drive, with schmitt trigger
B4SU	Bi-direction – 4mA drive, with pull-up and schmitt trigger
Pwr	+2.5V or +3.3V power supply voltage
Gnd	Power supply ground
Name_N	Low active
Name_L	Low active

Table 5. Pin Type legend

6.1 Pin Assignments

Table 6 lists the pin number, pin name and pin type for the 208 pin CS98000 package. The primary function and pin direction is shown for all signal pins. For some signal pins, a secondary function and direction are also shown. For pins having more than one function, the primary function is chosen when the chip is reset.

Pin	Name	Type	Primary Function	Dir	Secondary Function	Dir	Note
1	VDD_PLL	Pwr	PLL Power 2.5V				
2	M_A_11	O8	SDRAM Address[11]	O	ROM/NVRAM Address[11]	O	
3	M_A_10	O8	SDRAM Address[10]	O	ROM/NVRAM Address[10]	O	
4	GPIO_D18	B4U	GenioDVD[18]	B	System Clock PLL Bypass	I	
5	M_A_9	O8	SDRAM Address[9]	O	ROM/NVRAM Address[9]	O	
6	M_A_8	O8	SDRAM Address[8]	O	ROM/NVRAM Address8]	O	
7	M_A_7	O8	SDRAM Address[7]	O	ROM/NVRAM Address[7]	O	
8	GPIO_D16	B4SU	GenioDVD[16]	B			
9	M_A_6	O8	SDRAM Address[6]	O	ROM/NVRAM Address[6]	O	
10	M_A_5	O8	SDRAM Address[5]	O	ROM/NVRAM Address[5]	O	
11	M_A_4	O8	SDRAM Address[4]	O	ROM/NVRAM Address[4]	O	
12	GPIO_D17	B4U	GenioDVD[17]	B			
13	M_A_3	O8	SDRAM Address[3]	O	ROM/NVRAM Address[3]	O	
14	M_A_2	O8	SDRAM Address[2]	O	ROM/NVRAM Address[2]	O	
15	M_A_1	O8	SDRAM Address[1]	O	ROM/NVRAM Address[1]	O	
16	M_A_0	O8	SDRAM Address[0]	O	ROM/NVRAM Address[0]	O	
17	GPIO_D19	B4U	GenioDVD[19]	B	Memory Clock PLL Bypass	I	
18	VSS_IO	Gnd	I/O Ground				
19	M_CKO	O8	SDRAM Clock	O			
20	VDD_IO	Pwr	I/O Power 3.3V				
21	M_BS_L	O8	SDRAM Bank Select	O			
22	M_CKE	B8	SDRAM Clock Enable	O	GenioMis(7)	B	
23	M_AP	O8	SDRAM Auto Pre-charge	O			
24	M_RAS_L	O8	SDRAM Row Strobe	O			
25	M_CAS_L	O8	SDRAM Column Strobe	O			
26	GPIO_D20	B4U	GenioDVD[20]	B			
27	M_WE_L	O8	SDRAM Write Enable	O			
28	M_DQM_0	O8	SDRAM DQM[0]	O			
29	M_DQM_1	O8	SDRAM DQM[1]	O			
30	GPIO_D0	B4U	GenioDVD[0]	B			
31	M_DQM_2	O8	SDRAM DQM[2]	O			
32	M_DQM_3	O8	SDRAM DQM[3]	O			
33	M_D_8	B8U	SDRAM Data[8]	B	ROM/NVRAM Data[8]	B	
34	GPIO_D1	B4U	GenioDVD[1]	B			
35	VSS_IO	Gnd	I/O Ground				

Table 6. Pin assignments

36	VSS_CORE	Gnd	Core Ground				
37	M_D_7	B8U	SDRAM Data[7]	B	ROM/NVRAM Data[7]	B	
38	VDD_IO	Pwr	I/O Power 3.3V				
39	GPIO_D2	B4U	GenioDVD[2]	B			
40	M_D_9	B8U	SDRAM Data[9]	B	ROM/NVRAM Data[9]	B	
41	VDD_CORE	Pwr	Core Power 2.5V				
42	M_D_6	B8U	SDRAM Data[6]	B	ROM/NVRAM Data[6]	B	
43	GPIO_D3	B4U	GenioDVD[3]	B			
44	M_D_10	B8U	SDRAM Data[10]	B	ROM/NVRAM Data[10]	B	
45	M_D_5	B8U	SDRAM Data[5]	B	ROM/NVRAM Data[5]	B	
46	M_D_11	B8U	SDRAM Data[11]	B	ROM/NVRAM Data[11]	B	
47	GPIO_D4	B4U	GenioDVD[4]	B			
48	M_D_4	B8U	SDRAM Data[4]	B	ROM/NVRAM Data[4]	B	
49	M_D_12	B8U	SDRAM Data[12]	B	ROM/NVRAM Data[12]	B	
50	GPIO_D5	B4U	GenioDVD[5]	B			
51	M_D_3	B8U	SDRAM Data[3]	B	ROM/NVRAM Data[3]	B	
52	UNUSED		may leave unconnected				
53	UNUSED		may leave unconnected				
54	M_D_13	B8U	SDRAM Data[13]	B	ROM/NVRAM Data[13]	B	
55	M_D_2	B8U	SDRAM Data[2]	B	ROM/NVRAM Data[2]	B	
56	M_D_14	B8U	SDRAM Data[14]	B	ROM/NVRAM Data[14]	B	
57	GPIO_D6	B4U	GenioDVD[6]	B			
58	VSS_IO	Gnd	I/O Ground				
59	M_D_1	B8U	SDRAM Data[1]	B	ROM/NVRAM Data[1]	B	
60	M_D_15	B8U	SDRAM Data[15]	B	ROM/NVRAM Data[15]	B	
61	GPIO_D7	B4U	GenioDVD[7]	I		B	
62	M_D_0	B8U	SDRAM Data[0]	B	ROM/NVRAM Data[0]	B	
63	VSS_CORE	Gnd	Core Ground				
64	M_D_24	B8U	SDRAM Data[24]	B	ROM/NVRAM Address[20]	O	
65	GPIO_D11	B4U	GenioDVD[11]	B			
66	VDD_CORE	Pwr	Core Power 2.5V				
67	M_D_23	B8U	SDRAM Data[23]	B	ROM/NVRAM Address[19]	O	
68	M_D_25	B8U	SDRAM Data[23]	B	ROM/NVRAM Address[21]	O	
69	GPIO_D10	B4U	GenioDVD[10]	B			
70	M_D_22	B8U	SDRAM Data[22]	B	ROM/NVRAM Address[18]	O	
71	M_D_26	B8U	SDRAM Data[26]	B	ROM/NVRAM Address[22]	O	
72	M_D_21	B8U	SDRAM Data[21]	B	ROM/NVRAM Address[17]	O	
73	GPIO_D9	B4U	GenioDVD[9]	B			
74	M_D_27	B8U	SDRAM Data[27]	B	ROM/NVRAM Address[23]	O	
75	M_D_20	B8U	SDRAM Data[20]	B	ROM/NVRAM Address[16]	O	
76	M_D_28	B8U	SDRAM Data[28]	B			

Table 6. Pin assignments (Continued)

77	GPIO_D8	B4U	GenioDVD[8]	B			
78	M_D_19	B8U	SDRAM Data[19]	B	ROM/NVRAM Address[15]	O	
79	M_D_29	B8U	SDRAM Data[29]	B			
80	M_D_18	B8U	SDRAM Data[18]	B	ROM/NVRAM Address[14]	O	
81	NV_WE_L	B4U	NVRAM Write Enable	O	GenioMis[8]	B	
82	VSS_CORE	Gnd	Core Ground				
83	M_D_30	B8U	SDRAM Data[30]	B	ROM/NVRAM Decode Low	O	
84	VDD_CORE	Pwr	Core Power 2.5V				
85	H_ALE	B4U	Host Address Latch	O	GenioHst[13]	B	
86	M_D_17	B8U	SDRAM Data[18]	B	ROM/NVRAM Address[13]	O	
87	M_D_31	B8U	SDRAM Data[31]	B	ROM/NVRAM Decode High	O	
88	M_D_16	B8U	SDRAM Data[16]	B	ROM/NVRAM Address[12]	O	
89	GPIO_H14	B4U	GenioHst[14]	B			
90	NV_OE_L	O4	ROM/NVRAM Output Enable	O			
91	VDD_IO	Pwr	I/O Power 3.3V				
92	H_RD	B4S	Host Read Strobe	O	DVD Data Strobe	I	1
93	H_WR	B4	Host Write Strobe	O	DVD Data Enable	I	1
94	GPIO_H15	B4U	GenioHst[15]	B			
95	H_RDY	B4	Host Ready	I	DVD Data Ready	O	1
96	VSS_IO	Gnd	I/O Ground				
97	H_A_2	B4	Host Address[2]	O	GenioHst[10]	B	1
98	GPIO_H16	B4U	GenioHst[16]	B			
99	H_A_1	B4	Host Address[1]	O	GenioHst[9]	B	1
100	H_A_0	B4	Host Address[0]	O	GenioHst[8]	B	1
101	H_CS_1	B4	Host Chip Select [1]	O	DVD Error	I	1
102	H_A_4	B4	Host Address[4]	O	GenioHst[12]	B	1
103	VSS_CORE	Gnd	Core Ground				
104	VSS_PLL	Gnd	PLL Ground				
105	VDD_PLL	Pwr	PLL Power 2.5V				
106	H_CS_0	B4	Host Chip Select[0]	O	DVD Start Sector	I	1
107	H_A_3	B4	Host Address[3]	O	GenioHst[11]	B	1
108	VDD_CORE	Pwr	Core Power 2.5V				
109	H_D_15	B4	Host Data[15]	B	CD Data	I	1, 2
110	H_D_14	B4	Host Data[14]	B	CD Left Right Clock	I	1, 2
111	H_CS_3	B4	Host Chip Select[3]	O	GenioHst[18]	B	1
112	H_D_13	B4S	Host Data[13]	B	CD Clock	I	1, 2
113	H_D_12	B4	Host Data[12]	B	CD Error	I	1, 2
114	H_D_11	B4	Host Data[11]	B	DVD Control Data In	I	1, 2
115	H_CS_2	B4	Host Chip Select[2]	O	GenioHst[17]	B	1
116	H_D_10	B4	Host Data[10]	B	DVD Control Data Out	O	1, 2

Table 6. Pin assignments (Continued)

117	H_D_9	B4	Host Data[9]	B	DVD Control Ready	I	1, 2
118	H_D_8	B4	Host Data[8]	B	DVD Control Clock	O	1, 2
119	VSS_IO	Gnd	I/O Ground				
120	H_CKO	B4	Host Clock	O	GenioHst[19]	B	1
121	H_D_7	B4	Host Data[7]	B	DVD Data[7]	I	1
122	H_D_6	B4	Host Data[6]	B	DVD Data[6]	I	1
123	H_D_5	B4	Host Data[5]	B	DVD Data[5]	I	1
124	AUD_BCK	B4	Audio Out Bit Clock	O	GenioMis[3]	B	
125	H_D_4	B4	Host Data[4]	B	DVD Data[4]	I	1
126	VSS_CORE	Gnd	Core Ground				
127	H_D_3	B4	Host Data[3]	B	DVD Data[3]	I	1
128	AUD_LRCK	O4	Audio Out LR Clock	O			
129	VDD_CORE	Pwr	Core Power 2.5V				
130	H_D_2	B4	Host Data[2]	B	DVD Data[2]	I	1
131	VDD_IO	Pwr	I/O Power 3.3V				
132	H_D_1	B4	Host Data[1]	B	DVD Data[1]	I	1
133	AUD_DO_2	B4	Audio Out Data[2]	O	GenioMis[2]	B	
134	H_D_0	B4	Host Data[0]	B	DVD Data[0]	I	1
135	AUD_DO_0	O4	Audio Out Data[0]	O			
136	AUD_DO_1	B4	Audio Out Data[1]	O	GenioMis[1]	B	
137	AIN_BCK	IU	Audio In Bit Clock	I			
138	VSS_CORE	Gnd	Core Ground				
139	AIN_LRCK	IU	Audio In LR Clock	I			
140	AIN_DATA	B4U	Audio In Data	I	GenioMis[0]	B	
141	VDD_CORE	Pwr	Core Power 2.5V				
142	CDC_DI	IU	Serial CODEC Data In	I			
143	VSS_IO	Gnd	I/O Ground				
144	CDC_DO	T4	Serial CODEC Data Out	O			
145	VIN_CLK	IU	Video Input Clock	I			
146	CDC_RST	T4	Serial CODEC Reset	O			
147	CDC_CK	IU	Serial CODEC Bit Clock	I			
148	CDC_SY	B4U	Serial CODEC Sync	B			
149	GPIO_V10	B4U	GenioMis[26]	B			
150	GPIO_D15	B4U	GenioDvd[15]				
151	GPIO_D14	B4U	GenioDvd[14]				
152	GPIO_D13	B4SU	GenioDvd[13]				
153	VIN_VSNC	B4U	Video Input Vsync	I	GenioMis[25]	B	
154	CLK27_O	B4U	Video Output Clock	O	GenioMis[6]	B	
155	GPIO_D12	B4U	GenioDvd[12]				
156	VDD_PLL	Pwr	PLL Power 2.5V				
157	VSS_PLL	Gnd	PLL Ground				

Table 6. Pin assignments (Continued)

158	VSS_CORE	Gnd	Core Ground				
159	HSYNC	B4U	Video Output Hsync	O	GenioMis[4]	B	
160	VIN_HSYNC	B4U	Video Input Hsync	I	GenioMis[24]	B	
161	VDD_CORE	Pwr	Core Power 2.5V				
162	VSYNC	B4U	Video Output Vsync	O	GenioMis[5]	B	
163	VDAT_0	O4	Video Output Data[0]	O			
164	VIN_D0	B4U	Video Input Data[0]	I	GenioMis[16]	B	
165	VDAT_1	O4	Video Output Data[1]	O			
166	VDAT_2	O4	Video Output Data[2]	O			
167	VDAT_3	O4	Video Output Data[3]	O			
168	VIN_D1	B4U	Video Input Data[1]	I	GenioMis[17]	B	
169	VDAT_4	O4	Video Output Data[4]	O			
170	VDAT_5	O4	Video Output Data[5]	O			
171	UNUSED		may leave unconnected				
172	VDAT_6	O4	Video Output Data[6]	O			
173	VDAT_7	O4	Video Output Data[7]	O			
174	GPIO_0	B4U	General Purpose IO[0]	B	Audio PLL Input Bypass	I	
175	VIN_D2	B4U	Video Input Data[2]	I	GenioMis[18]	B	
176	VSS_CORE	Gnd	Core Ground				
177	AUD_DO_3	B4U	Audio Out Data[3]	O	General Purpose IO[1]	B	
178	VDD_CORE	Pwr	Core Power 2.5V				
179	VIN_D3	B4U	Video Input Data[3]	I	GenioMis[19]	B	
180	VDD_IO	Pwr	I/O Power 3.3V				
181	GPIO_2	B4U	General Purpose IO[2]	B			
182	VSS_IO	Gnd	I/O Ground				
183	GPIO_3	B4U	General Purpose IO[3]	B			
184	VIN_D4	B4U	Video Input Data[4]	I	GenioMis[20]	B	
185	GPIO_4	B4U	General Purpose IO[4]	B			
186	SCL	B4U	I^2C Clock	B	General Purpose IO[5]	B	
187	SDA	B4U	I^2C Data	B	General Purpose IO[6]	B	
188	GPIO_7	B4U	General Purpose IO[7]	B			
189	VIN_D5	B4U	Video Input Data[5]	I	GenioMis[21]	B	
190	GPIO_8	B4U	General Purpose IO[8]	B			
191	AUD_XCLK	B4U	Audio 256x/384x Clock	B	General Purpose IO[9]	B	
192	GPIO_10	B4U	General Purpose IO[10]	B			
193	VIN_D6	B4U	Video Input Data[6]	I	GenioMis[22]	B	
194	GPIO_11	B4U	General Purpose IO[11]	B			
195	GPIO_12	B4U	General Purpose IO[12]	B			
196	GPIO_13	B4U	General Purpose IO[13]	B			
197	GPIO_14	B4U	General Purpose IO[14]	B			
198	VIN_D7	B4U	Video Input Data[7]	I	GenioMis[23]	B	

Table 6. Pin assignments (Continued)

158	VSS_CORE	Gnd	Core Ground				
159	HSYNC	B4U	Video Output Hsync	O	GenioMis[4]	B	
160	VIN_HSYNC	B4U	Video Input Hsync	I	GenioMis[24]	B	
161	VDD_CORE	Pwr	Core Power 2.5V				
162	VSYNC	B4U	Video Output Vsync	O	GenioMis[5]	B	
163	VDAT_0	O4	Video Output Data[0]	O			
164	VIN_D0	B4U	Video Input Data[0]	I	GenioMis[16]	B	
165	VDAT_1	O4	Video Output Data[1]	O			
166	VDAT_2	O4	Video Output Data[2]	O			
167	VDAT_3	O4	Video Output Data[3]	O			
168	VIN_D1	B4U	Video Input Data[1]	I	GenioMis[17]	B	
169	VDAT_4	O4	Video Output Data[4]	O			
170	VDAT_5	O4	Video Output Data[5]	O			
171	UNUSED		may leave unconnected				
172	VDAT_6	O4	Video Output Data[6]	O			
173	VDAT_7	O4	Video Output Data[7]	O			
174	GPIO_0	B4U	General Purpose IO[0]	B	Audio PLL Input Bypass	I	
175	VIN_D2	B4U	Video Input Data[2]	I	GenioMis[18]	B	
176	VSS_CORE	Gnd	Core Ground				
177	AUD_DO_3	B4U	Audio Out Data[3]	O	General Purpose IO[1]	B	
178	VDD_CORE	Pwr	Core Power 2.5V				
179	VIN_D3	B4U	Video Input Data[3]	I	GenioMis[19]	B	
180	VDD_IO	Pwr	I/O Power 3.3V				
181	GPIO_2	B4U	General Purpose IO[2]	B			
182	VSS_IO	Gnd	I/O Ground				
183	GPIO_3	B4U	General Purpose IO[3]	B			
184	VIN_D4	B4U	Video Input Data[4]	I	GenioMis[20]	B	
185	GPIO_4	B4U	General Purpose IO[4]	B			
186	SCL	B4U	I^2C Clock	B	General Purpose IO[5]	B	
187	SDA	B4U	I^2C Data	B	General Purpose IO[6]	B	
188	GPIO_7	B4U	General Purpose IO[7]	B			
189	VIN_D5	B4U	Video Input Data[5]	I	GenioMis[21]	B	
190	GPIO_8	B4U	General Purpose IO[8]	B			
191	AUD_XCLK	B4U	Audio 256x/384x Clock	B	General Purpose IO[9]	B	
192	GPIO_10	B4U	General Purpose IO[10]	B			
193	VIN_D6	B4U	Video Input Data[6]	I	GenioMis[22]	B	
194	GPIO_11	B4U	General Purpose IO[11]	B			
195	GPIO_12	B4U	General Purpose IO[12]	B			
196	GPIO_13	B4U	General Purpose IO[13]	B			
197	GPIO_14	B4U	General Purpose IO[14]	B			
198	VIN_D7	B4U	Video Input Data[7]	I	GenioMis[23]	B	

Table 6. Pin assignments (Continued)

Pin Descriptions

Table 1. Pin Details of EM638165

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>CLK</td><td>Input</td><td>Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.</td></tr>
<tr><td>CKE</td><td>Input</td><td>Clock Enable: CKE activates(HIGH) and deactivates(LOW) the CLK signal. If CKE goes low synchronously with clock(set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.</td></tr>
<tr><td>BA0,BA1</td><td>Input</td><td>Bank Select: BA0,BA1 input select the bank for operation.
<table>
<tr><th>BA1</th><th>BA0</th><th>Select Bank</th></tr>
<tr><td>0</td><td>0</td><td>BANK #A</td></tr>
<tr><td>0</td><td>1</td><td>BANK #B</td></tr>
<tr><td>1</td><td>0</td><td>BANK #C</td></tr>
<tr><td>1</td><td>1</td><td>BANK #D</td></tr>
</table></td></tr>
<tr><td>A0-A11</td><td>Input</td><td>Address Inputs: A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 2M available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set command.</td></tr>
<tr><td>CS#</td><td>Input</td><td>Chip Select: CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.</td></tr>
<tr><td>RAS#</td><td>Input</td><td>Row Address Strobe: The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.</td></tr>
<tr><td>CAS#</td><td>Input</td><td>Column Address Strobe: The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."</td></tr>
</table>

Pin Descriptions

Table 1. Pin Details of EM638165

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
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<table>
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<tr><td>0</td><td>0</td><td>BANK #A</td></tr>
<tr><td>0</td><td>1</td><td>BANK #B</td></tr>
<tr><td>1</td><td>0</td><td>BANK #C</td></tr>
<tr><td>1</td><td>1</td><td>BANK #D</td></tr>
</table></td></tr>
<tr><td>A0-A11</td><td>Input</td><td>Address Inputs: A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 2M available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set command.</td></tr>
<tr><td>CS#</td><td>Input</td><td>Chip Select: CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.</td></tr>
<tr><td>RAS#</td><td>Input</td><td>Row Address Strobe: The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.</td></tr>
<tr><td>CAS#</td><td>Input</td><td>Column Address Strobe: The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."</td></tr>
</table>

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note (1), (2))

Command	State	CKE_{n-1}	CKE_n	DQM	BA0,1	A10	A0-9,11	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	X	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

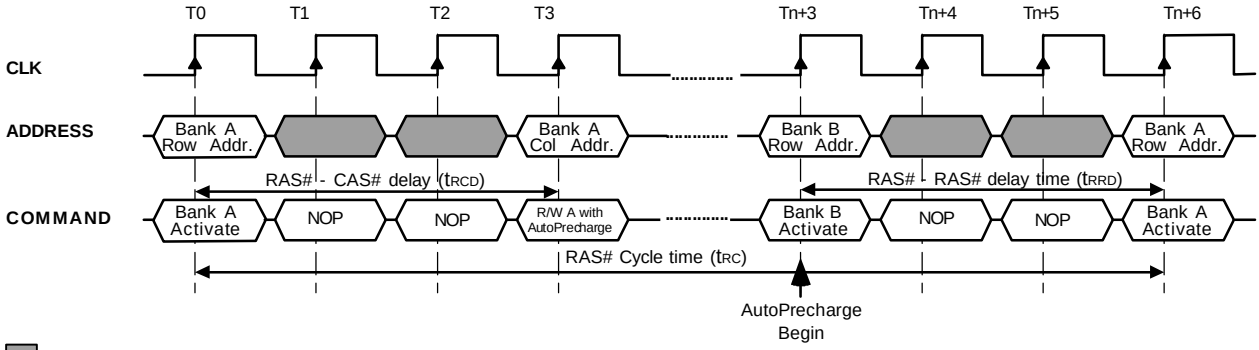
Note: 1. V=Valid X=Don't Care L=Low level H=High level
2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BS signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle, device state is clock suspend mode.

Commands

1 BankActivate

(RAS# = "L", CAS# = "H", WE# = "H", BAs = Bank, A0-A11 = Row Address)

The BankActivate command activates the idle bank designated by the BA0,1 signals. By latching the row address on A0 to A11 at the time of this command, the selected row access is initiated. The read or write operation in the same bank can occur after a time delay of t_{RCD}(min.) from the time of bank activation. A subsequent BankActivate command to a different row in the same bank can only be issued after the previous active row has been precharged (refer to the following figure). The minimum time interval between successive BankActivate commands to the same bank is defined by t_{RC}(min.). The SDRAM has four internal banks on the same chip and shares part of the internal circuitry to reduce chip area; therefore it restricts the back-to-back activation of the four banks. t_{RRD}(min.) specifies the minimum time required between activating different banks. After this command is used, the Write command and the Block Write command perform the no mask write operation.



: "H" or "L"

BankActivate Command Cycle (Burst Length = n, CAS# Latency = 3)

2 BankPrecharge command

(RAS# = "L", CAS# = "H", WE# = "L", BAs = Bank, A10 = "L", A0-A9 and A11 = Don't care)

The BankPrecharge command precharges the bank disignated by BA signal. The precharged bank is switched from the active state to the idle state. This command can be asserted anytime after t_{RAS}(min.) is satisfied from the BankActivate command in the desired bank. The maximum time any bank can be active is specified by t_{RAS}(max.). Therefore, the precharge function must be performed in any active bank within t_{RAS}(max.). At the end of precharge, the precharged bank is still in the idle state and is ready to be activated again.

3 PrechargeAll command

(RAS# = "L", CAS# = "H", WE# = "L", BAs = Don't care, A10 = "H", A0 -A9 and A11 = Don't care)

The PrechargeAll command precharges all banks simultaneously and can be issued even if all banks are not in the active state. All banks are then switched to the idle state.

4 Read command

(RAS# = "H", CAS# = "L", WE# = "H", BAs = Bank, A10 = "L", A0-A7 = Column Address)

The Read command is used to read a burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least t_{RCD}(min.) before the Read command is issued. During read bursts, the valid data-out element from the starting column address will be available following the CAS# latency after the issue of the Read command. Each subsequent data-out element will be valid by the next positive clock edge (refer to the following figure). The DQs go into high-impedance at the end of the burst unless other command is initiated. The burst length, burst sequence, and CAS# latency are determined by the mode register, which is already programmed. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).

NTSC/PAL Digital Video Encoder

Features

- Six DACs providing simultaneous composite, S-video, and RGB or Component YUV outputs
- Programmable DAC output currents for low imped-ance (37.5 Ω) and high impedance (150 Ω) loads.
- Multi-standard support for NTSC-M, NTSC-JAPAN, PAL (B, D, G, H, I, M, N, Combination N)
- ITU R.BT656 input mode supporting EAV/SAV codes and CCIR601 Master/Slave input modes
- Programmable HSYNC and VSYNC timing
- Multistandard Teletext (Europe, NABTS, WST) support
- VBI encoding support
- Wide-Screen Signaling (WSS) support, EIA-J CPX1204
- NTSC closed caption encoder with interrupt
- CS4955 supports Macrovision copy protection Version 7
- Host interface configurable for parallel or I^2C compatible operation
- On-chip voltage reference generator
- +3.3 V or +5 V operation, CMOS, low-power modes, tri-state DACs

Description

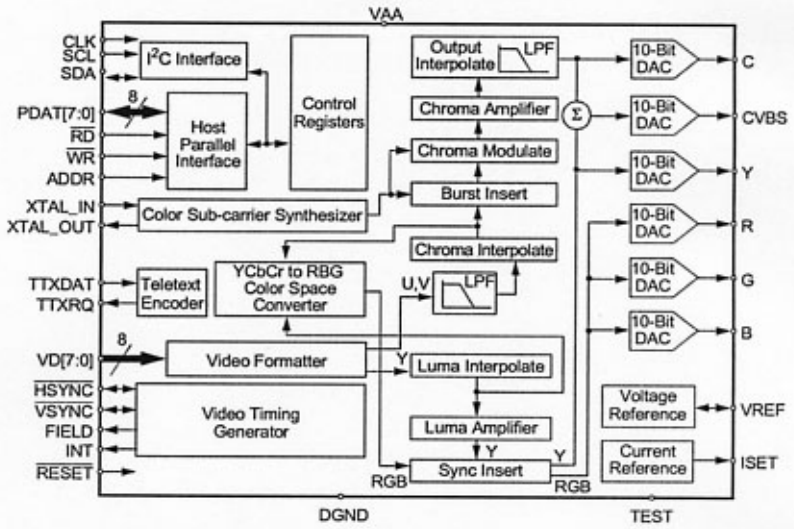
The CS4954/5 provides full conversion from digital video formats YCbCr or YUV into NTSC and PAL Composite, Y/C (S-video) and RGB, or YUV analog video. Input formats can be 27 MHz 8-bit YUV, 8-bit YCbCr, or ITU R.BT656 with support for EAV/SAV codes. Video output can be formatted to be compatible with NTSC-M, NTSC-J, PAL-B,D,G,H,I,M,N, and Combination N systems. Closed Caption is supported in NTSC. Teletext is supported for NTSC and PAL.

Six 10-bit DACs provide two channels for an S-Video output port, one or two composite video outputs, and three RGB or YUV outputs. Two-times oversampling reduces the output filter requirements and guarantees no DAC-related modulation components within the specified bandwidth of any of the supported video standards.

Parallel or high-speed I^2C compatible control interfaces are provided for flexibility in system design. The parallel interface doubles as a general purpose I/O port when the CS4954/5 is in I^2C mode to help conserve valuable board area.

ORDERING INFORMATION

CS4954-CQ	48-pin TQFP
CS4955-CQ	48-pin TQFP



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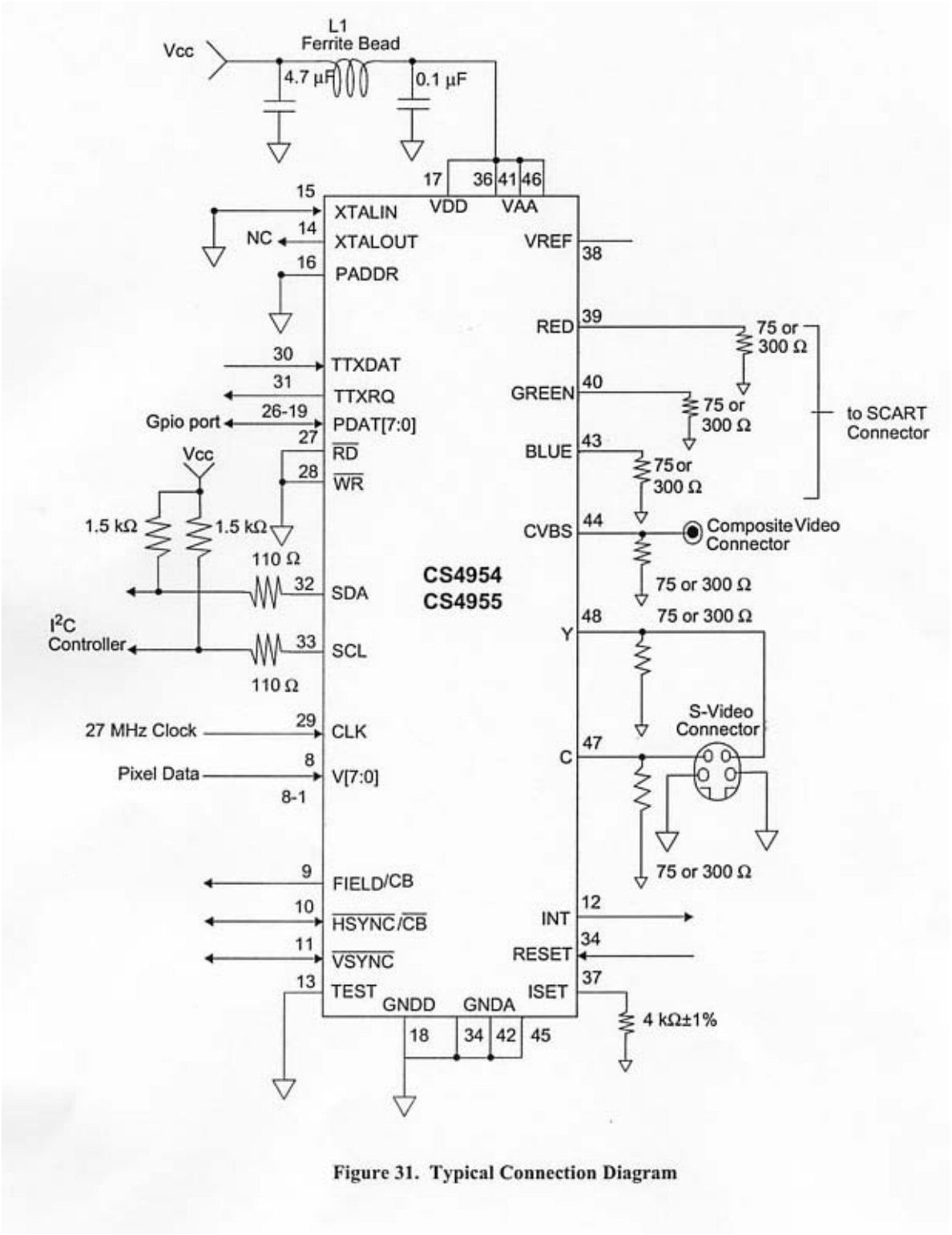


Figure 31. Typical Connection Diagram

Pin Name	Pin Number	Type	Description
V [7:0]	8, 7, 6, 5, 4, 3, 2, 1	IN	Digital video data inputs
CLK	29	IN	27 MHz input clock
PADDR	16	IN	Address enable line
XTAL_IN	15	IN	subcarrier crystal input
XTAL_OUT	14	OUT	subcarrier crystal output
$\overline{\text{HSYNC}}$/$\overline{\text{CB}}$	10	I/O	Active low horizontal sync, or composite blank signal
$\overline{\text{VSYNC}}$	11	I/O	Active low vertical sync.
FIELD/CB	9	OUT	Video field ID. Selectable polarity or composite blank
$\overline{\text{RD}}$	27	IN	Host parallel port read strobe, active low
$\overline{\text{WR}}$	28	IN	Host parallel port write strobe, active low
PDAT [7:0]	19, 20, 21, 22, 23, 24, 25, 26	I/O	Host parallel port/ general purpose I/O
SDA	32	I/O	I^2C data
SCL	33	IN	I^2C clock input
CVBS	44	CURRENT	Composite video output
Y	48	CURRENT	Luminance analog output
C	47	CURRENT	Chrominance analog output
R	39	CURRENT	Red analog output
G	40	CURRENT	Green analog output
B	43	CURRENT	Blue analog output
VREF	38	I/O	Internal voltage reference output or external reference input
ISET	37	CURRENT	DAC current set
TTXDAT	30	IN	Teletext data input
TTXRQ	31	OUT	Teletext request output
INT	12	OUT	Interrupt output, active high
$\overline{\text{RESET}}$	34	IN	Active low master RESET
TEST	13	IN	TEST pin. Ground for normal operation
VAA	36, 41, 46	PS	+ 5 V or + 3.3 V supply (must be same as VDD)
GNDD	18	PS	Ground
VDD	17	PS	+5 V or 3.3 V supply (must be same as VAA)
GNDA	35, 42, 45	PS	Ground

Table 10. Device Pin Descriptions

24-Bit, 192 kHz 6 Channel D/A Converter

Features

- 24-Bit Conversion
- 102 dB Dynamic Range
- -90 dB THD+N
- +3 V to +5 V Power Supply
- Digital Volume Control with Soft Ramp
  - 119 dB Attenuation
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Low Power Consumption
  - 105 mW with 3 V supply
- ATAPI Mixing
- Low Clock Jitter Sensitivity
- Popguard Technology® for Control of Clicks and Pops

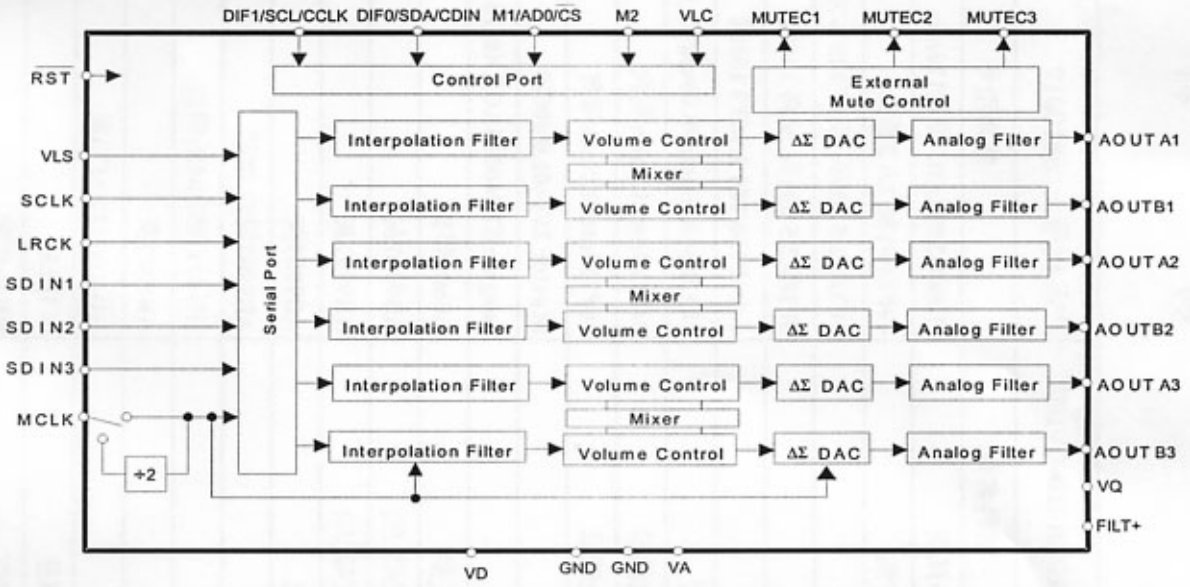
Description

The CS4360 is a complete 6-channel digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4360 accepts data at audio sample rates from 4 kHz to 200 kHz, consumes very little power and operates over a wide power supply range. These features are ideal for cost-sensitive, multi-channel audio systems including DVD players, A/V receivers, set-top boxes, digital TVs and VCRs, mini-component systems, and mixing consoles.

ORDERING INFORMATION

CS4360-KS	-10 to 70 °C	28-pin SOIC
CS4360-BS	-40 to 85 °C	28-pin SOIC
CS4360-KZ	-10 to 70 °C	28-pin TSSOP
CS4360-BZ	-40 to 85 °C	28-pin TSSOP
CDB4360		Evaluation Board



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2. TYPICAL CONNECTION DIAGRAM

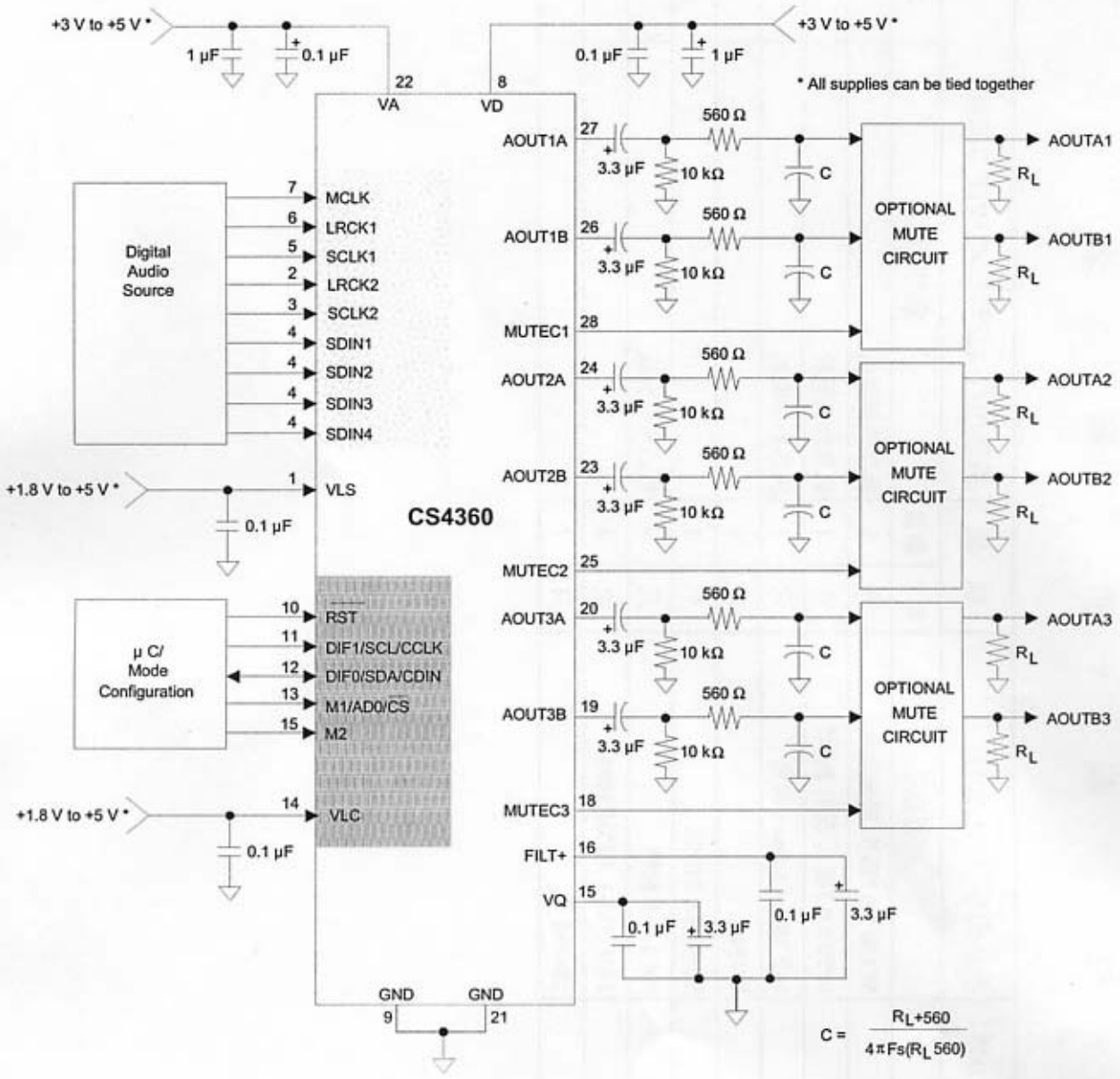
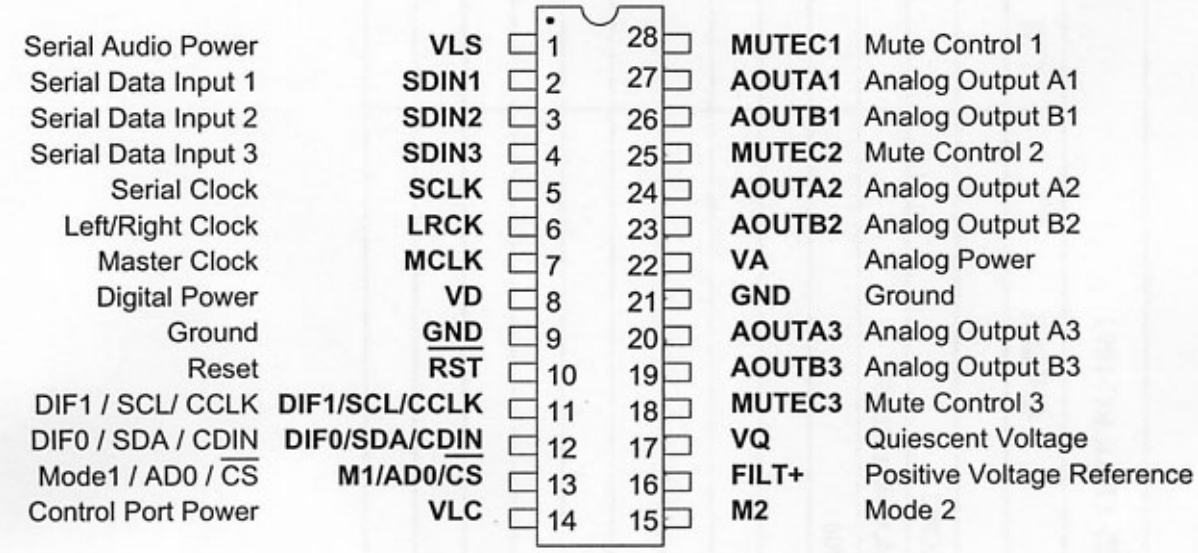


Figure 4. Typical Connection Diagram

5. PIN DESCRIPTION



Pin Name	#	Pin Description
VLS	1	**Serial Audio Interface Power** (*Input*) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages. Applies to pins 2-7.
SDIN1 SDIN2 SDIN3	2 3 4	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data. SDIN1 corresponds to AOUT1x, SDIN2 corresponds to AOUT2x and SDIN3 corresponds to AOUT3x.
SCLK	5	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
LRCK	6	**Left / Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
MCLK	7	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 6 illustrates several standard audio sample rates and the required master clock frequency.
VD	8	**Digital Power** (*Input*) - Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	9 21	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
$\overline{\text{RST}}$	10	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low. The control port cannot be accessed when Reset is low.
VLC	14	**Control Port Interface Power** (*Input*) - Determines the required signal level for the control port and provides power for bidirectional control port pins. Refer to the Recommended Operating Conditions for appropriate voltages. Applies to pins 10-13 and 15.
FILT+	16	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to GND as shown in the Typical Connection Diagram.

VQ	17	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less than the maximum specified in the Analog Characteristics and Specifications section.
VA	22	**Analog Power** (*Input*) - Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
AOUTA1 AOUTB1 AOUTA2 AOUTB2 AOUTA3 AOUTB3	19 20 23 24 26 27	**Analog Outputs** (*Output*) - The full scale analog line output level is specified in the Analog Characteristics specifications table.
MUTEC1 MUTEC2 MUTEC3	18 25 28	**Mute Control** (*Output*) - The Mute Control pin goes high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. The use of an external mute circuit is not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
Control Port Definitions		
SCL/CCLK	11	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in Two-Wire mode as shown in the Typical Connection Diagram.
SDA/CDIN	12	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in Two-Wire format and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDIN is the input data line for the control port interface in SPI format.
AD0/$\overline{CS}$	13	**Address Bit 0 (Two-Wire) / Control Port Chip Select (SPI)** (*Input/Output*) - AD0 is a chip address pin Two-Wire format; $\overline{CS}$ is the chip select signal for SPI format.
Stand-Alone Definitions		
DIF1 DIF0	11 12	**Digital Interface Format** (*Input*) - The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format selection. Refer to Table 4.

DIF1	DIF0	DESCRIPTION
0	0	Left Justified, up to 24-bit data
0	1	I^2S, up to 24-bit data
1	0	Right Justified, 16-bit data
1	1	Right Justified, 24-bit data

Table 4. Digital Interface Formats - Stand Alone Mode

M1 M2	13 15	**Mode Selection** (*Input*) - Determines the operational mode of the device as detailed in Table 5.

M2	M1	MODE
0	0	Single-Speed without de-emphasis (4 to 50 kHz sample rates)
0	1	Single-Speed with de-emphasis (32 to 48 kHz sample rates)
1	0	Double-Speed (50 to 100 kHz sample rates)
1	1	Quad-Speed (100 to 200 kHz sample rates)

Table 5. Mode Selection

Sample Rate (kHz)	MCLK (MHz)				
	256x	384x	512x	768x	1024x*
32	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	11.2896	16.9344	22.5792	32.7680	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

* Requires MCLKDIV bit = 1

Table 6. Single-Speed Mode Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x*
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

* Requires MCLKDIV bit = 1

Table 7. Double-Speed Mode Common Clock Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x*
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

* Requires MCLKDIV bit = 1

Table 8. Quad-Speed Mode Common Clock Frequencies

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Use of this product in any manner that complies with the MPEG-2 video standard as defined in ISO documents IS 13818-1 (including annexes C, D, F, J, and K), IS 13818-2 (including annexes A, B, C, and D, but excluding scalable extensions), and IS 13818-4 (only as it is needed to clarify IS 13818-2) is expressly prohibited without a license under applicable patents in the MPEG-2 patent portfolio, which license is available from MPEG LA, L.L.C. 250 Steele Street, Suite 300, Denver, Colorado 80296.

Overview

The CS92288 is a real time MPEG-2 audio/video encoder and decoder (CODEC), with system multiplexor/demultiplexor and on-screen display (OSD). For video coding, the CS92288 fully complies with the ISO/IEC 13818 Main Level @ Main Profile (ML@MP) or with the ISO/IEC 11172 (MPEG-1) formats. For audio encoding, the CS92288 supports a variety of audio formats, including MPEG-1 or MPEG-2 audio (all Layers) and Dolby Digital (AC-3).

In encode mode, the CS92288 accepts digital video in ITU-R BT.601 (CCIR-601) or ITU-R BT.656 (CCIR-656) formats, and digital audio in LPCM format. The input video is filtered and then encoded to produce a compressed bitstream in either MPEG-1 or MPEG-2 ML@MP syntax. The audio is compressed in either MPEG or Dolby Digital formats. The compressed video and audio streams are multiplexed to produce an MPEG-compliant program bit stream.

In decode mode, the CS92288 accepts an MPEG program bit stream or audio and video elementary streams and produces ITU-R BT.601 or BT.656 video and LPCM audio outputs.

The CS92288 is designed to provide a high degree of integration and ease of system design. It makes an ideal solution for a variety of MPEG-based audio/visual applications, such as PC-based content creation, VCD and DVD-RAM players/recorders, set-top boxes, and time-shift recording. For example, a single CS92288 is adequate for a complete Super VCD (SVCD) player/recorder.

For the evaluation of the CS92288, Cirrus Logic provides a PC-based Evaluation Board, window drivers, and application software. In addition, Cirrus Logic offers a complete reference design for a stand-alone MPEG-based video recorder/player. This design allows designers and manufacturers a quick entry to the digital recording markets.

Features

- Single Chip Real Time MPEG-2 Audio/Video CODEC with system Mux/Demux and On-screen Display (OSD)
- Supports MPEG-1 audio/video encoding and decoding
- Supports Dolby Digital audio encoding and decoding
- Programmable system mux/demux supports DVD, VCD, and SVCD encoding and decoding
- 8-bit OSD support (2-b text, 2-b to 8-b graphics)
- Support for Constant Bit Rate (CBR) and one-pass Variable Bit Rate (VBR)
  - IPB-pictures, CBR (average), VBR (max) up to 15Mbps.
  - I-pictures only to 30Mbps
- Proprietary High Performance Motion Estimation
- Low external SDRAM memory:
  - 8 Mbytes for D1, 2B picture format
- Supports Multiple Resolutions & Scan Rates
  - NTSC: (720, 704, 640, 544, 480, 352) x 480 or 352 x 240 (CIF), and 176x112 (QCIF) at 30 or 29.97 Hz
  - PAL: (720, 704, 640, 544, 480, 352) x 576 or 352 x 288 (CIF), and 176x144 (QCIF) at 25 Hz
- Integrated video pre and post processor
- 108 MHz operating frequency with separate 27 MHz input video clock
- **Video Preprocessor**
  - Accepts ITU-R BT.601 4:2:2 and D1 input formats
  - 4:2:2 to 4:2:0 Conversion
  - Built-in, programmable, pre-processing filters
  - Half Horizontal Resolution (HHR), SIF decimation filtering, or Two-Thirds Horizontal resolution filtering
  - Temporal filtering
  - Automatic inverse telecine
  - Sync Extraction
- **Video Encoder**
  - Real Time Encoding of MPEG-2 Main Level/Main Profile digital video
    - ISO/IEC 13818-2 compliant
    - SP@ML, MP@LL, MP@ML
    - Video Streams up to 13.5Mpels/s (16-bit) and 27Mpel/s (8-bit)
  - Real Time Encoding of MPEG-1
  - Support for Full D1, 2/3 D1, 1/2 D1, CIF, and QCIF

- Constant Bit Rate Support: up to 15Mbps (IPB frames) and 30Mbps (I frame only)
- Variable Bit Rate Support:
  - Real-time one-pass rate control
  - User-selectable average bitrate
- Proprietary High Performance Motion Estimation Engine
  - Half-pel accuracy
  - Horizontal Search Ranges: ±63.5, ±31.5, ±15.5, ±7.5 Pel/Frame
  - Vertical Search Range: ±31.5, ±15.5, ±7.5 Pel/Frame
- Guaranteed to operate at 30 frames/second
- Field-based or Frame-based DCT
- Field, 16x8, and frame-mode prediction
- Programmable encoding parameters
  - I and P-picture interval
  - quantization matrices
  - Encoding time
  - Average bitrate, upper and lower bitrate bounds
  - Active Picture Area Selection

- **Video Decoder**
  - Decodes ML@MP MPEG-2 video and MPEG-1 video
  - Support Full D1, 2/3 D1, 1/2 D1, CIF, and QCIF
  - Variable Length Decoder
    - Video stream syntax parsing and decoding
    - Error detection and handling
  - Motion Prediction
    - Supports frame, field, 16 x 8 and dual prime motion compensation modes
    - Performs half-pel interpolation and bi-directional interpolation
  - Error detection, handling and mitigation
- **Video Postprocessor**
  - Filters for interpolation to ITU-R BT.601 and BT.656 format
  - Display Management
  - Automatic repetition of dropped field for 3:2 Pulldown (Telecine)
  - Horizontal and vertical scaling
  - Master mode D1/VMI output
  - Slave mode CCIR output
  - Letter-box, NTSC to PAL format conversion
  - OSD/OGD; 2-bit text, 2-,4-, or 8-bit graphics
- **Audio Processor**
  - Programmable, 24-bit, digital signal processor
  - Input/Output sampling rates: 32, 44.1, 48, or 96 kHz
  - Data resolution up to 24 bits/sample
  - Two channel audio encoding or decoding in either MPEG (all Layers) or Dolby Digital (AC-3)
  - 5.1 channels audio decoding (downmixed to two channels)
  - Additional audio encoding/decoding algorithms can be supported via firmware upgrades
- **System Processor**
  - System Multiplexor/Demultiplexor
  - Based on powerful embedded ARC core
  - Programmable, supports DVD, VCD, SVCD, encoding and decoding
  - Supports Transport, Program, and Elementary streams
  - Trick Play; fast and slow play forward, fast play backward
- **System Interfaces**
  - 16-bit bus that supports Intel and Motorola interfaces
  - 8-bit interface supports the Philips Trimedia TM1300 and other 8-bit microcontrollers with either separate or multiplexed address and data buses.
  - Gluless interface to Philips 7146 PCI bridge
  - Direct interface to NTSC/PAL industry standard NTSC/PAL video encoders/decoders (Philips, Harris)

- Glueless interface to industry standard SDRAM(s)
- Glueless interface to Data Flash and EPROM memories
- 8051 Protocol interface
- I^2S
- General Purposed I/O
- Glueless interface to USB controllers
- Programmable clock output for audio A/D and D/A converters.

• **Technology**
- 0.18um CMOS technology
- 272-pin PBGA package
- 3.3 and 1.8 Volts power supplies
- 5V I/O tolerance
- Internal pull-ups for SDRAM and HIU data buses
- 1 W typical average power consumption at 108 MHz

Ordering Information

Part Number	Package	Operating Temp Range
CS92288	272L-BGA	0^o ~ $+70^o$

Application Information

Figure 1shows a digital audio/video deck using the CS92288, a host microcontroller, a CD-R/W drive, and supporting commodity devices. A drive interface is supported by the controller CPU to transfer data between the CS92288 and the CD-R/W drive. The functionality of the CS92288 can be controlled either from the host microcontroller or from an optional Firmware EPROM. The OSD EPROM is also optional

Encoding

Analog video is demodulated and passed to the CS92288. The setup and control for the NTSC/PAL video decoder are handled by an external I^2C interface master. Input video can be overlayed with on-screen graphics and be passed back to the NTSC/PAL video encoder for video output loopback.

Analog audio is digitized by the A/D converter, and LPCM data is transfered to the CS92288 via the I^2S interface. Audio loopback is provided by a separate I^2S interface to the output audio D/A of the system. The CS92288 utilizes the SDRAM to process the input audio and video, producing an MPEG-compliant output to the Host CPU. The Host CPU directs the writing of the data to the media.

Decoding

The compressed audio and video data is read off the media device. The CS92288 demultiplexes and decompresses the audio and video data and transfers digital video to the NTSC/PAL video encoder and digital LPCM audio to the audio D/A converter. Furthermore, the output video data can be mixed with OSD or OGT (On-screen Graphics and Text) data before the final output. The NTSC/PAL video encoder is configured by an external I^2C master. The audio D/A interfaces with the CS92288 using the I^2S bus and associated interface circuitry.

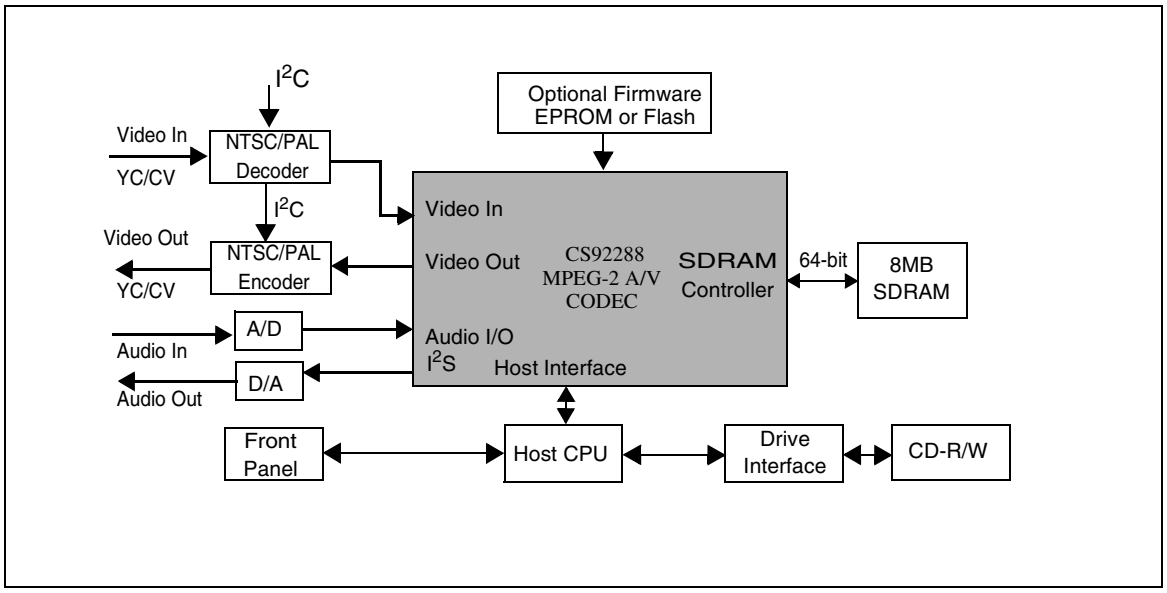

Figure 1: System diagram of an CS92288-based digital A/V Recorder/Player

Functional Descriptions

The CS92288 is organized as a process pipeline that implements the MPEG-2 audio and video encoding and decoding algorithms.

The CS92288 provides application program control over a large number of encoding parameters. For example, for video encoding one can control such parameters as I, P, B-picture cadence, GOP structure, bit rates, and decoder buffer sizes. For audio encoding, one can select coding format and average bit rate.

The algorithmic and architectural innovations of the CS92288 allow a unique degree of integration for the MPEG audio/video CODEC function. The CS92288 is also designed to provide a high degree of system integration and ease of system design. These combined benefits make it an ideal platform for a variety of MPEG-2-based digital audio/video applications

For communication applications, the CS92288 can match the output bit rate to the channel rate. This feature allows the host controller to make bit rate changes as needed to demonstrate better bandwidth utilization across multiple channels.

Internal rate control provides a high degree of flexibility in relation to the output bit rate, including the ability to generate variable bit rate compressed video stream in one pass. This makes it suitable for storage sensitive applications such as digital camcorders and digital versatile discs (DVDs).

The CS92288 also has features geared toward MPEG-2 publishing and authoring systems. These include the ability to specify the initial decoder buffer fullness.

Architecture

Figure 2 shows the major functional units of the CS92288.These units include:

- The RISC microcontroller (an ARC RISC core)
- The Video Interface Unit (VIO)
- The Audio Interface Unit (AIU)
- The Video Engine Unit (VEU)
- The Audio Engine (DSP)
- The Host Interface Unit (HIU), and
- The SDRAM Control Unit (DCU)

All blocks inter-communicate with two major data buses: a 64-bit wide data bus (D-Bus) and a 16-bit wide register bus (R-Bus). The PLL block is used to multiply (4X) the SYSCLK frequency to provide for all internal blocks and external memory clocking. A separate PLL is used to provide an output clock to external audio A/D and D/A converters.

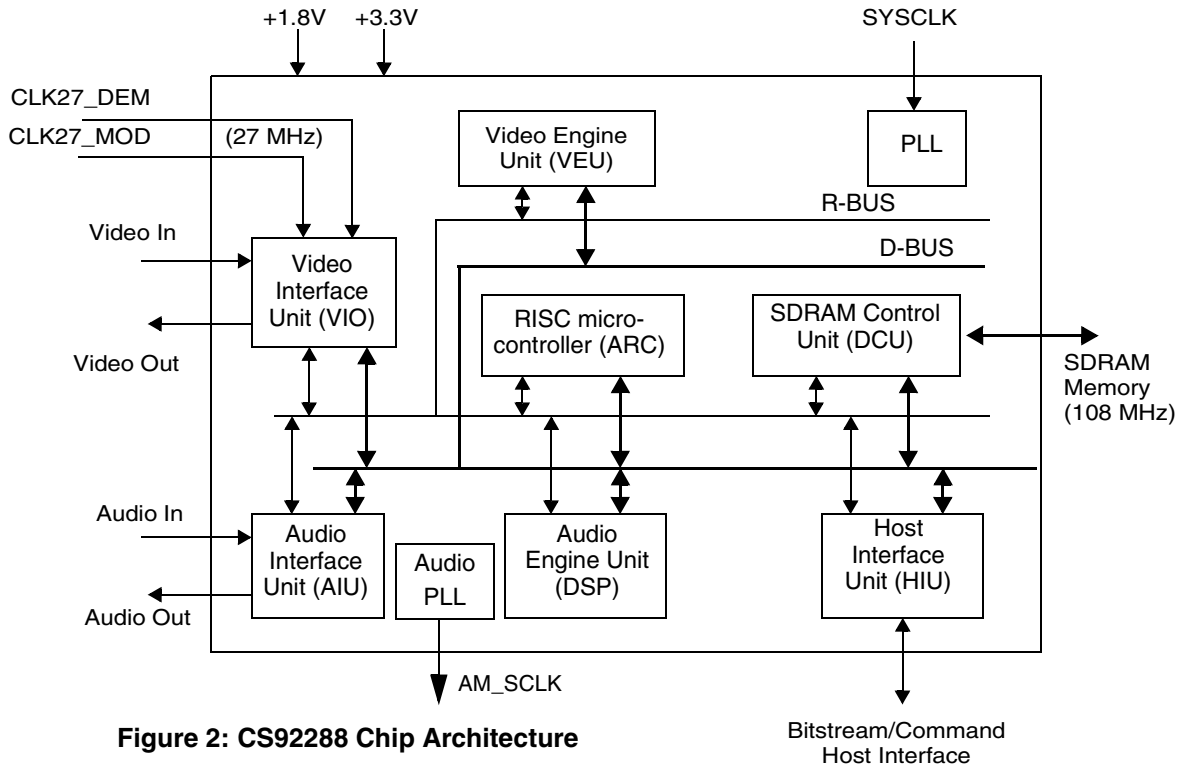

Figure 2: CS92288 Chip Architecture

The Video Interface Unit (VIO)

Figure 3 shows a block diagram of the VIO. It includes the Video Input Unit (VIU), the Video Output Unit (VOU), the Video Processing Unit (VPU), and the OSD Unit.

The VIU selects the input video active area and performs chroma conversion, inverse telecine, spatial and/or temporal prefilter-

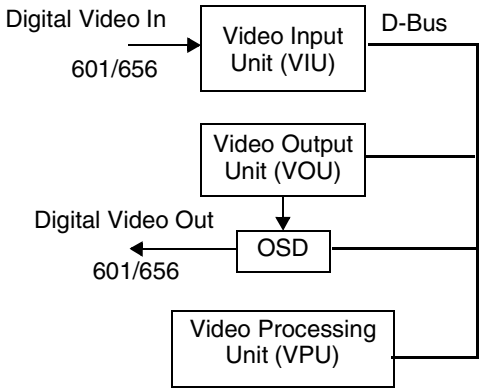

Figure 3: Block diagram of the Video Interface Unit

ing, and data arrangement to facilitate the subsequent encoding processes. It preprocesses the input data so that encoding can

be done in the most efficient way.

The VOU can perform a variety of postprocessing operations, including horizontal and vertical scaling, telecine, and video format conversion.

The OSD block mixes text and/or graphics from the OSD buffer (in SDRAM) with the output of the VOU and generates a correctly sequenced ITU-R BT.601 or 656 4:2:2 output video stream. The flexible architecture of the VIO unit allows it to operate in a number of different configurations.

Video Encoding - Normal Mode

Figure 4 shows the operation of the VIO unit under the normal encoding mode. Input video is captured by the VIU and is transferred to SDRAM. The buffered input is passed first to the VOU and then to the OSD unit, where it is mixed with text or graphics from the OSD buffers. The output of the OSD unit provides digital loopback of the input video, overlaid with on-screen text or graphics.

Video Encoding - Intermediate Mode

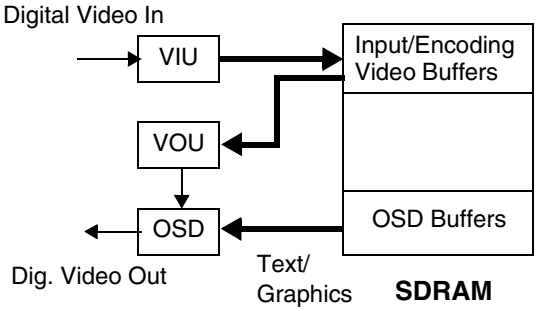

Figure 4: Video Encoding - Normal Mode

Figure 5 shows the flow of operations in the VIO unit under the intermediate encoding mode. As in the normal mode, this mode allows for digital video loopback of the input video with overlaid text or graphics. However, this mode also allows for additional preprocessing of the input video by the video processing unit (VPU). Among its functions, the VPU can initialize the video frame buffer with specific YCbCr values (e.g., blue screen generation), copy data from one video buffer to another, or scale data from one frame-buffer region to another frame-buffer region.

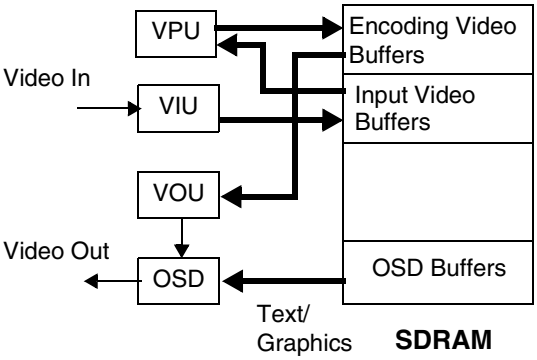

Figure 5: Video Encoding - Intermediate Mode

Video Encoding - Advanced Mode

Figure 6 shows the flow of operations when the VIO is used in advanced encoding mode. In this mode, input video is captured

directly by the OSD unit, where it can be mixed with OSD data. The output of the OSD unit is passed back to the VIU and then to SDRAM for video encoding. As in the previous mode, additional preprocessing of the video data by the VPU may also be enabled.

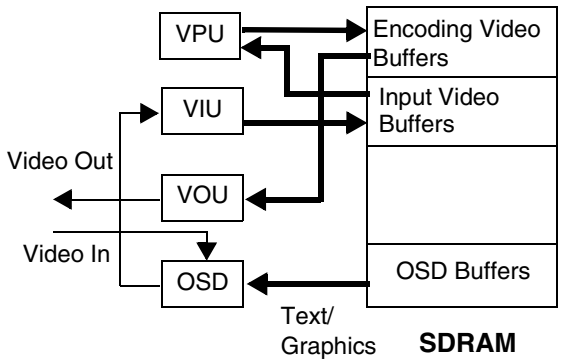

Figure 6: Video Encoding - Advanced Mode

Video Decoding

Figure 7 shows the flow of data in the VIO unit during video decoding. At minimum, decoded video data are transferred from the SDRAM to the VOU for chroma upconversion and other postprocessing. The output of the VOU is passed to the OSD unit where it can be mixed with text or graphics before it is transferred to the video output. Optionally, the VPU may also be enabled to process the decoded data before they are being transferred to the VOU.

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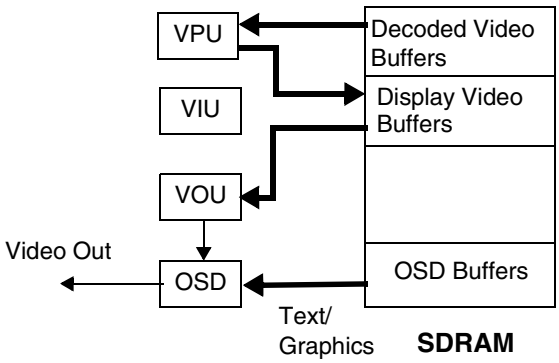

Figure 7: Video Decoding

The Audio Interface Unit (AIU)

The audio interface unit provides the interface between the CS92288 and external audio devices. Audio samples are transferred in and out of the CS92288 using I^2S signaling. The CS92288 also provides a user-configurable output clock for external audio A/D and D/As.

The RISC Microcontroller

This is an embedded, programmable,32-bit ARC RISC processor. It performs multiplexing and demultiplexing of MPEG program streams and acts as a central sequencer. Its microcode can be downloaded either from an external host, from external data Flash, or from an external EEPROM, through the Host Interface Unit.

The Video Engine Unit (VEU)

This is the core video processor for the CS92288. During encoding, it operates on the video data and generates an MPEG-compliant video elementary stream. It includes several dedicated processing units, such as the motion estimation and refinement units. Among its many functions, it performs motion estimation and compensation, DCT, quantization, rate control, and variable length coding. During decoding, it operates on a video elementary stream and generates decompressed video frames. It performs, variable length decoding, IDCT, and motion compensation. The IDCT output is fully compliant with the IEEE-1800 accuracy requirements.

The Audio Engine

The Audio Engine provides the core processing power for all audio-related functions. It consists of an embedded, 24-bit, general purpose, and programmable digital signal processor (DSP). The DSP operates from its own embedded program and data memories for the most efficient processing of audio data.

The Host Interface Unit

The CS92288 host interface is used for communication with the host controller and external EPROMS or flash memory. It is designed to support a variety of communication protocols. The host interface has a glue-less interface to USB controllers and it may also be used in PC-based host systems using a PCI bridge interface, such as the Philips 7146.

The SDRAM Control Unit (DCU)

The SDRAM control unit (DCU) provides a 64-bit interface from all functional units to the off-chip memory (SDRAM) storage. It is designed to sustain real-time audio and video encoding and decoding at 30 frames per second.

Related Documentation

Additional information about the CS92288 can be found in:

- The "*CS92288 Programming Guide*"
- "*CS92288 JTAG Operation and Programming Guide*"
- "*CS92288 - Data Book Addendum*"

available from Cirrus Logic.

Signal Descriptions

This section groups the signals according to the bus interface type. The convention for active-low signals is to apply an overscore to the signal name, e.g., active-low SIGNAL and active-high SIGNAL. Pin Types are defined as: I/O = Input and output; I = Input only; O = Output only; Ts = Tri-State.

Table 1: Host Interface

Pin Name	Type	Pin Number	Description
HAD[15:0]	I/O, Ts	J1,J3,H2,H1,H3,G2,G1,G3, F2,F1,F3,E2,E1,D2,E3,D3	16-bit Host Multiplexed Address/data (Pull-up Resistor Provided)
HA[7:0]	I	L3,M1,L2,L1,K3,K1,K2,J2	8-bit Address Bus
INTX16	I	R3	Bus Width Select. 0 = 8-bit bus; 1 = 16-bit bus
INTL_$\overline{\text{MOT}}$	I	T2	Interface Select. 0 = Motorola interface; 1 = Intel interface
$\overline{\text{AS\_ALE}}$	I	M2	Address Strobe (Motorola); Address Latch Enable (Intel) (Pull-up Resistor Provided). Both are low assertive
DMA_REQ	O	N1	DMA Request. Active-low or active-high is configurable. Default = active-high
$\overline{\text{DMA\_ACK}}$	I	N2	DMA Acknowledge, low assertive. Pull-up resistor is provided.
$\overline{\text{DTACK}}$_RDY	O	N3	Data Transfer Acknowledge - Low assertive(Motorola); Data Ready - High assertvie (Intel).
$\overline{\text{HSEL}}$	I	P1	Host Select, low assertive (Internal Resistor Pull-ups)
$\overline{\text{RWN\_SBHE}}$	I	P2	Read Write not (Motorola); System Byte High Enable (Intel). Both are low assertive
$\overline{\text{LDS\_RDN}}$	I	P3	Lower Data Strobe (Motorola); Read not (Intel). Both are low assertive
$\overline{\text{UDS\_WRN}}$	I	R1	Upper Data Strobe (Motorola); Write not (Intel). Both are low assertive
$\overline{\text{HIU\_INT}}$	O	R2	Host Interrupt, low assertive. Level triggered
SYS_RDY	O	T1	System Ready signal, high assertive
GPIO[5:0]	I/O	Y3,W3,Y2,Y1,V1,T3	6-bit General purpose I/O. Function is configurable by software. GPIO[0] is shared with the AM_WS signal of the audio interface
FLASH_SEL	I	U1	Flash memory indicator. If FLASH_SEL=1, then Flash memory is present.
ROM_SEL	I	U2	EPROM indicator. If ROM_SEL=1, read firmware from bootram EPROM
$\overline{\text{ROMDATA\_EN}}$	O	W1	If ROM_SEL=1, then chip enable for EPROM; active low.
SER_OUT	O	V2	If FLASH_SEL=1, serial output to data.
SCL	I/O	B9	Serial clock, normally configured as input
SDA	I/O	C9	Serial data bus, normally configured as input

Table 2: Video Interface

Pin Name	Type	Pin Number	Description
YIN[7:0]	I	B15,C15,A15,A16,B16,A17, C16,B17	8-bit Input video data
YOUT[7:0]	O, Ts	B12,A12,C13,B13,A13,A14, C14,B14	8-bit Output video data. Can be set into tristate mode by microcode
CLK27_DEM	I	C12	2x Input NTSC/PAL Decoder (Demodulator) Pixel-Clock (27MHz)
CLK27_MOD	I	B4	2x Input NTSC/PAL Encoder (Modulator) Pixel-Clock (27MHz)
HREF_DEM	I	A11	Horizontal Input Reference for ITU-R BT.601. High assertive

Table 2: Video Interface

HREF_MOD	I/O	B11	Horizontal Output Reference for ITU-R BT.601. Input in Slave mode; output in Master mode. High assertive
VSYNC_DEM	I	A10	Vertical Input Sync for ITU-R BT.601. Low assertive
VSYNC_MOD	I/O	C11	Vertical Output Sync for ITU-R BT.601. Input in Slave mode; output in Master mode. Low assertive
DREADY_DEM	I	B10	Data Ready signal, high assertive. Input in encode mode with field sync. Pull high with external resistor.
DREADY_MOD	O	A9	Data Ready signal, high assertive. Output in decode mode with vertical sync; Pull high with external resistor.
ENC_DEC	O	C10	Mode Select. 0 = Encode; 1 = Decode

Table 3: Audio Interface

Pin Name	Type	Pin Number	Description
WS_IN_ENC	I	C8	Input word select; value may be controlled by firmware. Defaults: WS_IN_ENC=0: Channel 1 (left), WS_IN_ENC=1: Channel 2 (right)
SD_IN_ENC	I	A7	Serial input audio data; used for audio encoding only
BCK_IN_ENC	I	B8	Serial data input bit clock for audio encoding
BCK_IN_DEC	I	A8	DAC input bit clock for audio data; used only for audio decoding in slave mode
BCK_OUT	O	B7	Serial data output bit clock; for decoding or loop-back during encoding
SD_OUT	O	A6	Serial output audio data; for decoding or loop-back during encoding
WS_OUT	O	C7	Output word select; value may be controlled by firmware. Defaults: WS_OUT=0: Channel 1 (left), WS_OUT=1: Channel 2 (right); for decoding or loop-back during encoding
AM_BCK	O	B3	Output Master bit clock from internal PLL for external audio A/D and D/A converters
AM_WS	O	T3	Output Master word select for slaves ADCs. This pin is shared with GPIO[0]
AM_SCLK	O	A3	Output Master system audio clock from internal PLL for external audio A/D and D/A converters.

Table 4: Memory Interface

Pin Name	Type	Pin Number	Function
MD[63:0]	I/O	V4,W4,V5,Y4,W5,Y5,W6,Y6,V7,W7,Y7,V8,W8,Y8,V9,W9, Y9,V10,W10,Y10,V11,W11,Y11,W12,Y12,W13,Y13,V13, W14,Y14,V14,W15,P19,P20,N19,M19,N20,M20,L19,L20, K19,K20,J18,J19,J20,H19,H20,H18,G19,G20,G18,F19, F18,C19,D18,B20,W17,V17,Y18,W18,Y19,Y20,V19,T18	64-bit SDRAM Data bus (Pull-up Resistor Provided)
MA[11:0]	O	U18,W20,U19,V20,R18,T19,U20,P18,T20,N18,R19,R20	12-bit SDRAM Address bus
DQMU	O	Y15	SDRAM Upper Byte I/O Mask
DQML	O	V15	SDRAM Lower Byte I/O Mask
WE	O	V16	SDRAM Write Enable, low assertive
CS	O	Y16	SDRAM Chip Select, low assertive
RAS	O	W16	SDRAM RAS, low assertive
CAS	O	Y17	SDRAM CAS, low assertive
CLKOUT[1:0]	O	A19,C17	SDRAM output Clocks (108MHz)

Table 5: Global Interface

Pin Name	Type	Pin Number	Function
SYSCLK	I	C4	System Clock (27 MHz)
HARD_RESET	I	U3	Chip Reset, low assertive (Pull-up Resistor Provided)
PLL_RESET	I	E19	PLL Reset, low assertive. Pull high for normal operation.
APLL_RESET	I	C1	Audio PLL Reset, low assertive. Pull high for normal operation.
CS_IN	I	C5	Chip Select Input, low assertive. When set to high, it tristates all output and bidirectional drivers. Set to low for normal operation
VDD	+1.8V	D9,D10,D13,G4,G17,H17,K4,L4,N17,U6,U10, U11,V6	1.8V core power supply
VDDD	+3.3V	D6,D7,D11,D14,F4,J4,J17,K17,M4,M17,P4,P17, R4,R17,U7,U8,U12,U14,U15,V12	3.3V I/O power supply
VSS	GND	D4,D17,J9-J12,K9-K12,L9-L12,M9-M12,U4,U17	VDD ground
VSSD	GND	B2,B19,C3,C18,D5,D8,D12,D15,D16,E4,E17, F17,H4,K18,L17,L18,M3,M18,N4,T4,T17,U5, U9,U13,U16,V3,V18,W2,W19	VDDD ground
PLL_VDD	+1.8V	F20	1.8V Video PLL power supply
PLL_VDDA	+1.8V	D20	1.8V Analog video PLL power supply
PLL_VSSA	GND	C20	Analog video PLL ground
PLL_VSS	GND	E20	Video PLL ground
APLL_VDD	+1.8V	D1	1.8V Audio PLL power supply
APLL_VDDA	+1.8V	B1	1.8V Analog Audio PLL power supply
APLL_VSSA	GND	A2	Analog Audio PLL ground
APLL_VSS	GND	C2	Audio PLL ground
TCK	I	B6	JTAG Input Clock
TDI	I	C6	JTAG Input Data
TMS	I	B5	JTAG Control Input
TDO	O	A5	JTAG Output Data
TEST_MODE	I	A20	For chip test only; ground for normal operation
GLOBAL_PD	I	E18	For chip test only; ground for normal operation
SE	I	A18	For chip test only; ground for normal operation
PLL_BP	I	A1	For chip test only; ground for normal operation
BIDI_IN	I	D19	Forces all bidirectional drivers to input-only mode. For chip test only; ground for normal operation
MBIST_EN	I	B18	For chip test only; ground for normal operation
ND_TREE	O	A4	For board test only; floating for normal operation

System Interfaces

The system interfaces consists of Host, Video, Audio, Memory, and Global interfaces; their definitions are detailed as follows:

Host Interface

The Host Interface Unit (HIU) port of the CS92288 provides an interface between the CS92288 on-chip CPU and components of an off-chip host system, such as boot ROM, Flash memory, or a host microcontroller. One of the main functions of the HIU module is to provide a communication link between a host and the CS92288 core modules so that encoding and decoding parameters can be properly set. Specifically, the HIU relays requests from the CS92288 on-chip CPU to the off-chip host system, and vice versa. Such requests include starting, loading of control parameters, stopping, loading of microcode, user status query and so forth.

The other function of the HIU is to serve as an interface for compressed bitstreams. During encoding, compressed audio/video bitstreams (Program Stream or Elementary Audio and Video Streams) output from the HIU to an application- specific host system. During decoding, compressed bit streams input from a host system to the CS92288 SDRAM via HIU.

CS92288 External Pins and Interfaces

Figures 8-10 shows typical connections of the CS92288 with external hosts.

Host Interface Signal Descriptions

HAD[15:0] are bidirectional multiplexed address/data pins. 8-bit or 16-bit operation is selectable by signal INTX16. Internal pull-up resistors are provided. In 8-bit demultiplexed mode, the higher 8 bits are used as data and the lower 8 bits are used as address (see Figure 10).

HA[7:0] is an 8-bit input address bus. It is used in demultiplexed or 8-bit mode.

INTX16 is an input pin defining the data bus width, 16-bit (set HIGH) and 8-bit (set LOW).

INTL_MOT is an input pin which can be selected in either Intel/ISA mode (set HIGH) or Motorola-68K mode (set LOW).

AS_ALE is a dual-purpose input pin. For Intel mode (when INTL_MOT=1), it is an active-low Address Latch Enable signal. For Motorola mode (when INTL_MOT=0), it is an active-low Address Strobe. This signal toggles only when a new address phase is presented. An internal pull-up resistor is provided.

DMA_REQ is an active-high output signal which can be asserted by CS92288 to an external processor to request an operand transfer. This pin can be configured as active-high (default upon power up) or active-low.

DMA_ACK, an active-low input signal, is asserted by an external processor to indicate an operand being transferred in response to a previous transfer request. An internal pull-up resistor is provided.

DTACK_RDY is a dual-purpose output pin. For Intel mode (when INTL_MOT=1), it is an active-high Ready signal. For Motorola mode (when INTL_MOT=0), it is an active-low Data Transfer Acknowledge.

HSEL is an active-low Chip-Select input pin, set LOW for normal operation. An internal pull-up resistor is provided.

RWN_SBHE is a dual-purpose input pin. For Intel mode (when INTL_MOT=1), it is an active-low System Byte High Enable signal. For Motorola mode (when INTL_MOT=0), it is an active-low Read/Write-not signal.

LDS_RDN is a dual-purpose input pin. For Intel mode (when INTL_MOT=1), it is an active-low Read signal. For Motorola mode (when INTL_MOT=0), it is an active-low Lower Data Strobe.

UDS_WRN is a dual-purpose input pin; for Intel mode (when INTL_MOT=1), it is an active-low Write signal. For Motorola mode (when INTL_MOT=0), it is an active-low Upper Data Strobe.

HIU_INT is an active-low level-triggered output pin which can be asserted by CS92288 to an external processor to request an interrupt. This pin is nonmaskable.

SYS_RDY is an active-high output System Ready signal to indicate HIU power-up properly and is ready for software download.

GPIO[5:0] is an 6-bit bidirectional bus for general purpose I/O. After reset, these pins are configured as input only. Afterwards, their function is programmable by microcode.

FLASH_SEL is an input pin which when set to high (FLASH_SEL=1) indicates the presense of Flash memory.

ROM_SEL is an input pin which when set to high (ROM_SEL=1) indicates the presence of an EPROM for downloading firmware.

$\overline{\text{ROMDATA\_EN}}$ is an active-low output pin. When ROM_SEL=1, this pin is being used as a chip select for the boot EPROM.

SER_OUT is an output serial signal bus for Flash memory (used when FLASH_SEL=1).

SCL is a bidirectional clock pin. When active, a clock is outputted from this pin. When inactive, it is configured as an input pin to allow other activities on this pin. This pin is used for the EPROM and Data Flash interface.

SDA is a bidirectional serial data pin. This pin outputs for write mode and inputs for read mode. When inactive, it is configured as an input pin to allow other activities on this pin. This pin is used for the EPROM and Data Flash interface.

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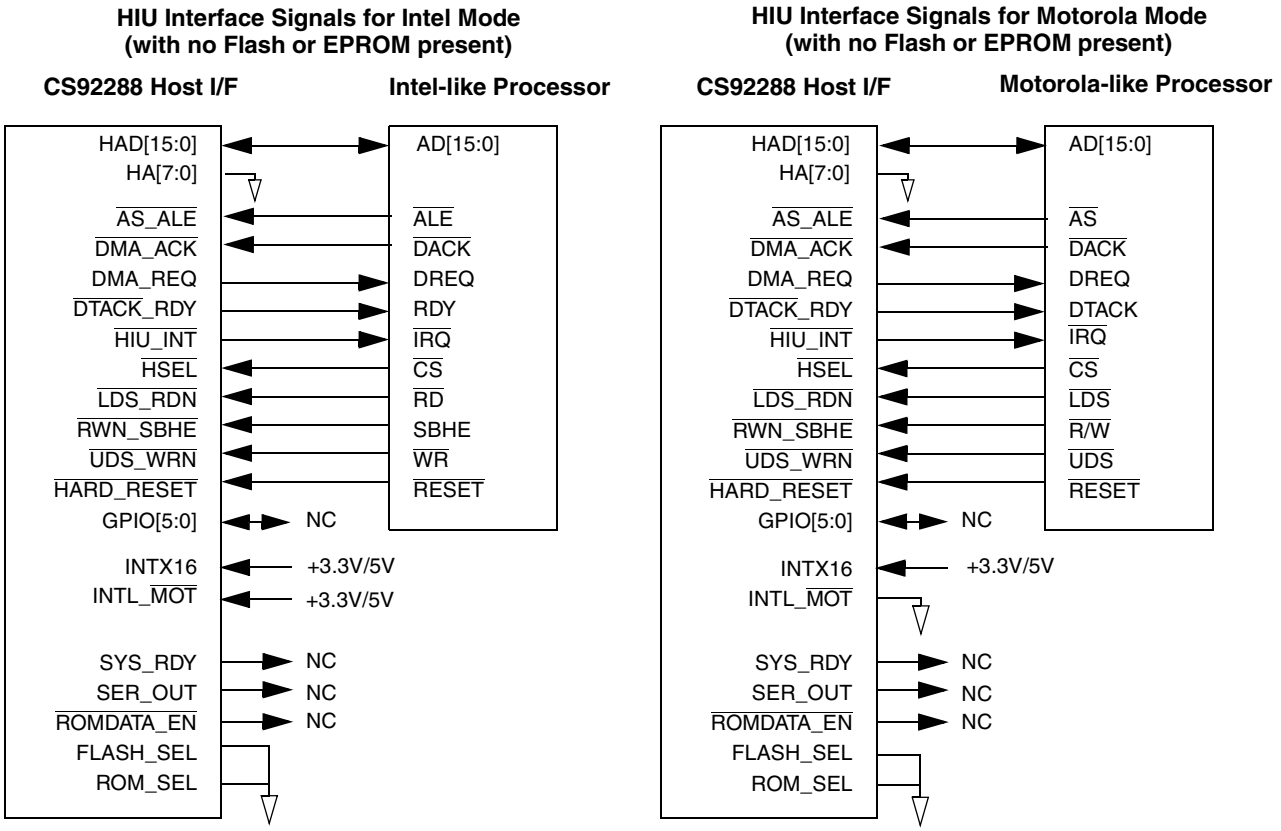


Figure 8: HIU Interface signals for 16-bit host processors

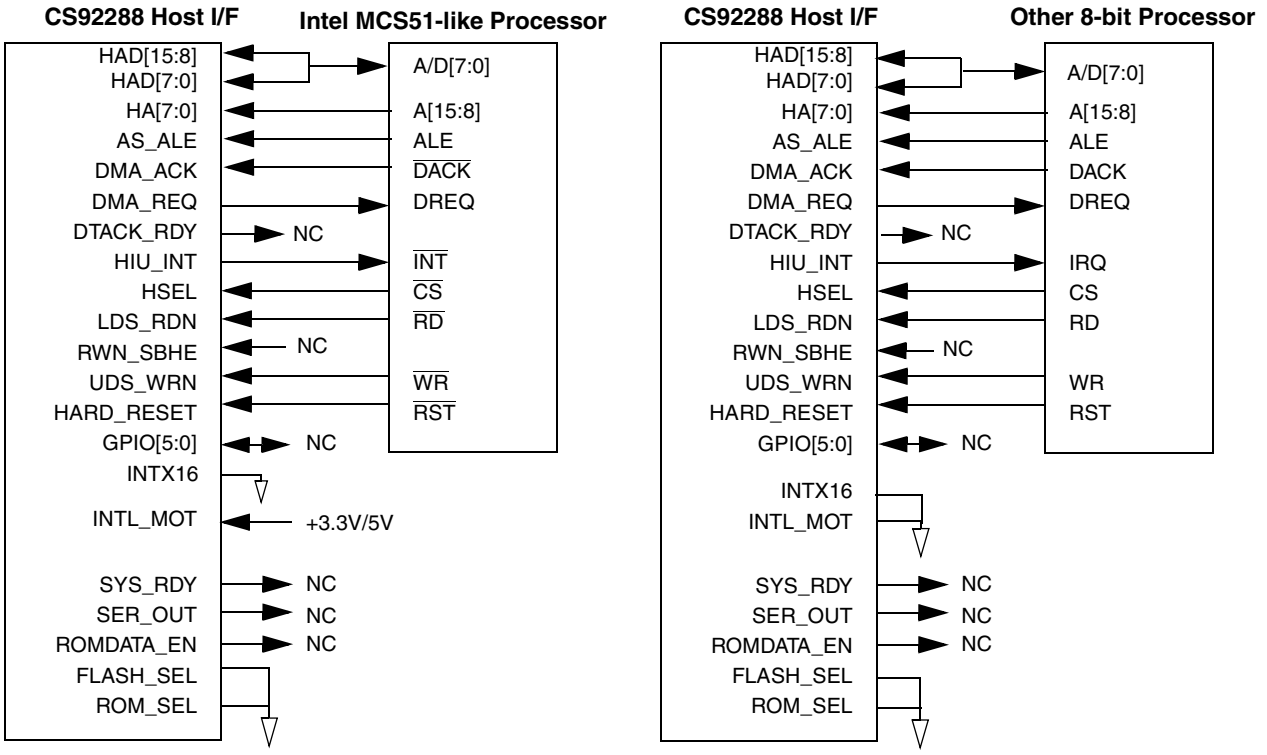


Figure 9: HIU Interface Signals for 8-bit Hosts with multiplexed address and data buses

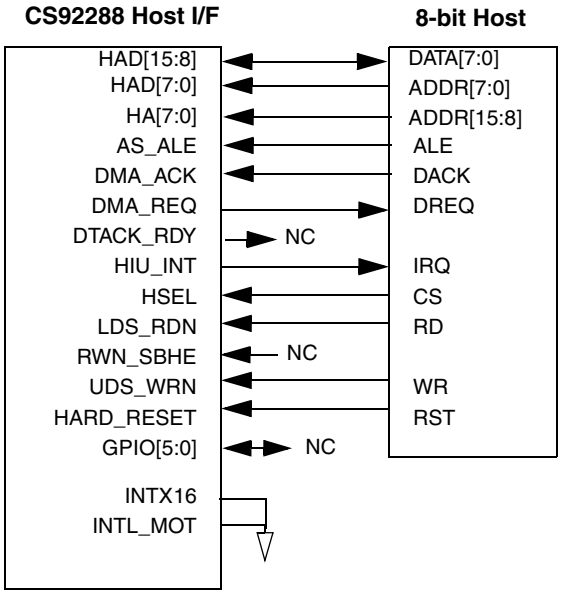


Figure 10: HIU Interface Signals for 8-bit Hosts with separate address and data buses

Description

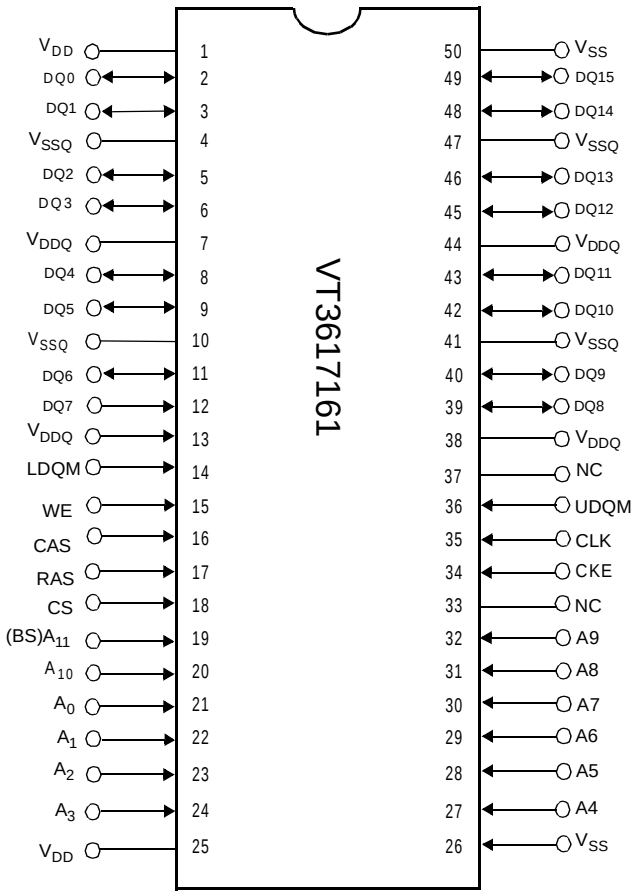
The VT3617161 is CMOS Synchronous Dynamic RAM organized as 524,288-word X 16-bit X 2-bank. It is fabricated with an advanced submicron CMOS technology and designed to operate from a single 3.3V power supply. This SDRAM is delicately designed with performance concern for current high-speed application. Programmable CAS Latency and Burst Length make it possible to be used in widely various domains. It is packaged by using JEDEC standard pinouts and standard plastic 50-pin TSOP II.

Features

- Single 3.3V +/- 0.3V power supply
- Clock Frequency: 166MHz, 143MHz, 125MHz, 100MHz
- Fully synchronous with all signals referenced to a positive clock edge
- Programmable CAS latency (2,3)
- Programmable burst length (1,2,4,8,& Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- Dual internal banks controlled by A11(Bank select)
- Simultaneous and independent two bank operation
- I/O level : LVTTL interface
- Random column access in every cycle
- X16 organization
- Byte control by LDQM and UDQM
- 2048 refresh cycles/32ms
- Burst termination by burst stop and precharge command

Pin Configuration

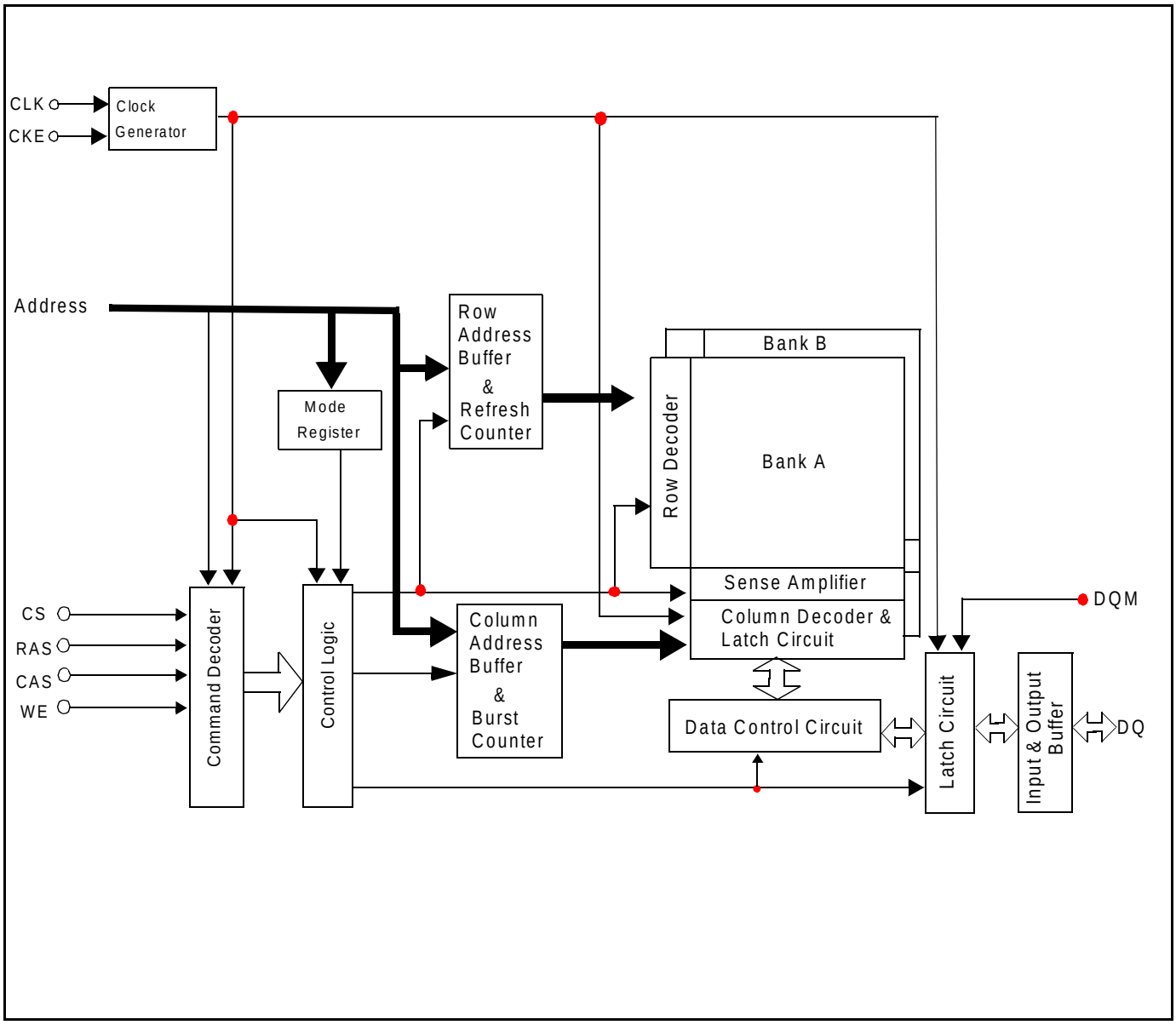
50-Pin Plastic TSOP(II)(400 mil)



Pin Description
(VT3617161)

Pin Name	Function	Pin Name	Function
A0-A11	Address inputs - Row address A0-A10 - Column address A0-A8 A11: Bank select	LDQM, UDQM	Lower DQ mask enable and Upper DQ mark enable
DQ0~DQ15	Data-in/data-out	CLK	Clock input
RAS	Row address strobe	CKE	Clock enable
CAS	Column address strobe	CS	Chip select
WE	Write enable	V_{DDQ}	Supply voltage for DQ
V_{SS}	Ground	V_{SSQ}	Ground for DQ
V_{DD}	Power		

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1.0 to +4.6	V
Supply voltage relative to Vss	V_{DD},V_{DDQ}	-1.0 to +4.6	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPT}	0 to + 70	℃
Storage temperature	T_{STG}	-55 to + 125	℃

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage, all inputs	V_{IH}	2.0	—	V_{DD}+0.3	V	1
Input Low Voltage, all inputs	V_{IL}	-0.3	—	0.8	V	2

Note 1.Overshoot limit : $V_{IH(MAX.)}$=V_{DDQ}+2.0V with a pulse width < 3ns
2.Undershoot limit : V_{IL}=V_{SSQ}-2.0V with a pulse < 3ns and -1.5V with a pulse < 5ns

Capacitance
(Ta=25°C,f=1MHZ)

Parameter	Symbol	Typ	Max	Unit
Input capacitance(CLK)	C_{11}	2.5	4	pF
Input capacitance(all input pins except data pins)	C_{12}	2.5	5	pF
Data input/output capacitance	$C_{I/O}$	4.0	6.5	pF

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI-data slicer and high performance scaler SAA7114H

CONTENTS

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI-data slicer and high performance scaler

SAA7114H

1 FEATURES

1.1 Video decoder

- Six analog inputs, internal analog source selectors, e.g. 6 × CVBS or (2 × Y/C and 2 × CVBS) or (1 × Y/C and 4 × CVBS)
- Two analog preprocessing channels in differential CMOS style inclusive built-in analog anti-alias filters
- Fully programmable static gain or Automatic Gain Control (AGC) for the selected CVBS or Y/C channel
- Automatic Clamp Control (ACC) for CVBS, Y and C
- Switchable white peak control
- Two 9-bit video CMOS Analog-to-Digital Converters (ADCs), digitized CVBS or Y/C signals are available on the expansion port
- On-chip line-locked clock generation according *“ITU 601”*
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources e.g. consumer grade VTR
- Requires only one crystal (32.11 or 24.576 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGDHIN, combination PAL N, PAL M, NTSC M, NTSC-Japan, NTSC 4.43 and SECAM
- Adaptive 2/4-line comb filter for two dimensional chrominance/luminance separation
  - Increased luminance and chrominance bandwidth for all PAL and NTSC standards
  - Reduced cross colour and cross luminance artefacts
- PAL delay line for correcting PAL phase errors
- Independent Brightness Contrast Saturation (BCS) adjustment for decoder part
- User programmable sharpness control
- Independent gain and offset adjustment for raw data path.

1.2 Video scaler

- Horizontal and vertical down-scaling and up-scaling to randomly sized windows
- Horizontal and vertical scaling range: variable zoom to $^{1}/_{64}$ (icon); it should be noted that the H and V zoom are restricted by the transfer data rates
- Anti-alias and accumulating filter for horizontal scaling
- Vertical scaling with linear phase interpolation and accumulating filter for anti-aliasing (6-bit phase accuracy)
- Horizontal phase correct up and down scaling for improved signal quality of scaled data, especially for compression and video phone applications, with 6-bit phase accuracy (1.2 ns step width)
- Two independent programming sets for scaler part, to define two ‘ranges’ per field or sequences over frames
- Fieldwise switching between decoder part and expansion port (X-port) input
- Brightness, contrast and saturation controls for scaled outputs.

1.3 Vertical Blanking Interval (VBI) data decoder and slicer

- Versatile VBI-data decoder, slicer, clock regeneration and byte synchronization e.g. for World Standard Teletext (WST), North-American Broadcast Text System (NABTS), close caption, Wide Screen Signalling (WSS) etc.

1.4 Audio clock generation

- Generation of a field locked audio master clock to support a constant number of audio clocks per video field
- Generation of an audio serial and left/right (channel) clock signal.

1.5 Digital I/O interfaces

- Real-time signal port (R port), inclusive continuous line-locked reference clock and real-time status information supporting RTC level 3.1 (refer to external document *"RTC Functional Specification"* for details)
- Bi-directional expansion port (X-port) with half duplex functionality (D1), 8-bit YUV
  - Output from decoder part, real-time and unscaled
  - Input to scaler part, e.g. video from MPEG decoder (extension to 16-bit possible)
- Video image port (I-port) configurable for 8-bit data (extension to 16-bit possible) in master mode (own clock), or slave mode (external clock), with auxiliary timing and hand shake signals
- Discontinuous data streams supported
- 32-word × 4-byte FIFO register for video output data
- 28-word × 4-byte FIFO register for decoded VBI output data
- Scaled 4 : 2 : 2, 4 : 1 : 1, 4 : 2 : 0, 4 : 1 : 0 YUV output
- Scaled 8-bit luminance only and raw CVBS data output
- Sliced, decoded VBI-data output.

1.6 Miscellaneous

- Power-on control
- 5 V tolerant digital inputs and I/O ports
- Software controlled power saving standby modes supported
- Programming via serial I^2C-bus, full read-back ability by an external controller, bit rate up to 400 kbits/s
- Boundary scan test circuit complies with the *"IEEE Std. 1149.b1 - 1994"*.

2 APPLICATIONS

- Desktop video
- Multimedia
- Digital television
- Image processing
- Video phone applications.

3 GENERAL DESCRIPTION

The SAA7114H is a video capture device for applications at the image port of VGA controllers.

The SAA7114H is a combination of a two-channel analog preprocessing circuit including source selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multi-standard decoder containing two-dimensional chrominance/luminance separation by an adaptive comb filter and a high performance scaler, including variable horizontal and vertical up and down scaling and a brightness, contrast and saturation control circuit.

It is a highly integrated circuit for desktop video applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into ITU 601 compatible colour component values. The SAA7114H accepts as analog inputs CVBS or S-video (Y/C) from TV or VCR sources, including weak and distorted signals. An expansion port (X-port) for digital video (bi-directional half duplex, D1 compatible) is also supported to connect to MPEG or video phone codec. At the so called image port (I-port) the SAA7114H supports 8 or 16-bit wide output data with auxiliary reference data for interfacing to VGA controllers.

The target application for SAA7114H is to capture and scale video images, to be provided as digital video stream through the image port of a VGA controller, for display via VGA's frame buffer, or for capture to system memory.

In parallel SAA7114H incorporates also provisions for capturing the serially coded data in the vertical blanking interval (VBI-data). Two principal functions are available:

1. To capture raw video samples, after interpolation to the required output data rate, via the scaler
2. A versatile data slicer (data recovery) unit.

SAA7114H incorporates also a field locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a field, or a set of fields. This prevents the loss of synchronization between video and audio, during capture or playback.

The circuit is I^2C-bus controlled (full write/read capability for all programming registers, bit rate up to 400 kbits/s).

6 BLOCK DIAGRAM

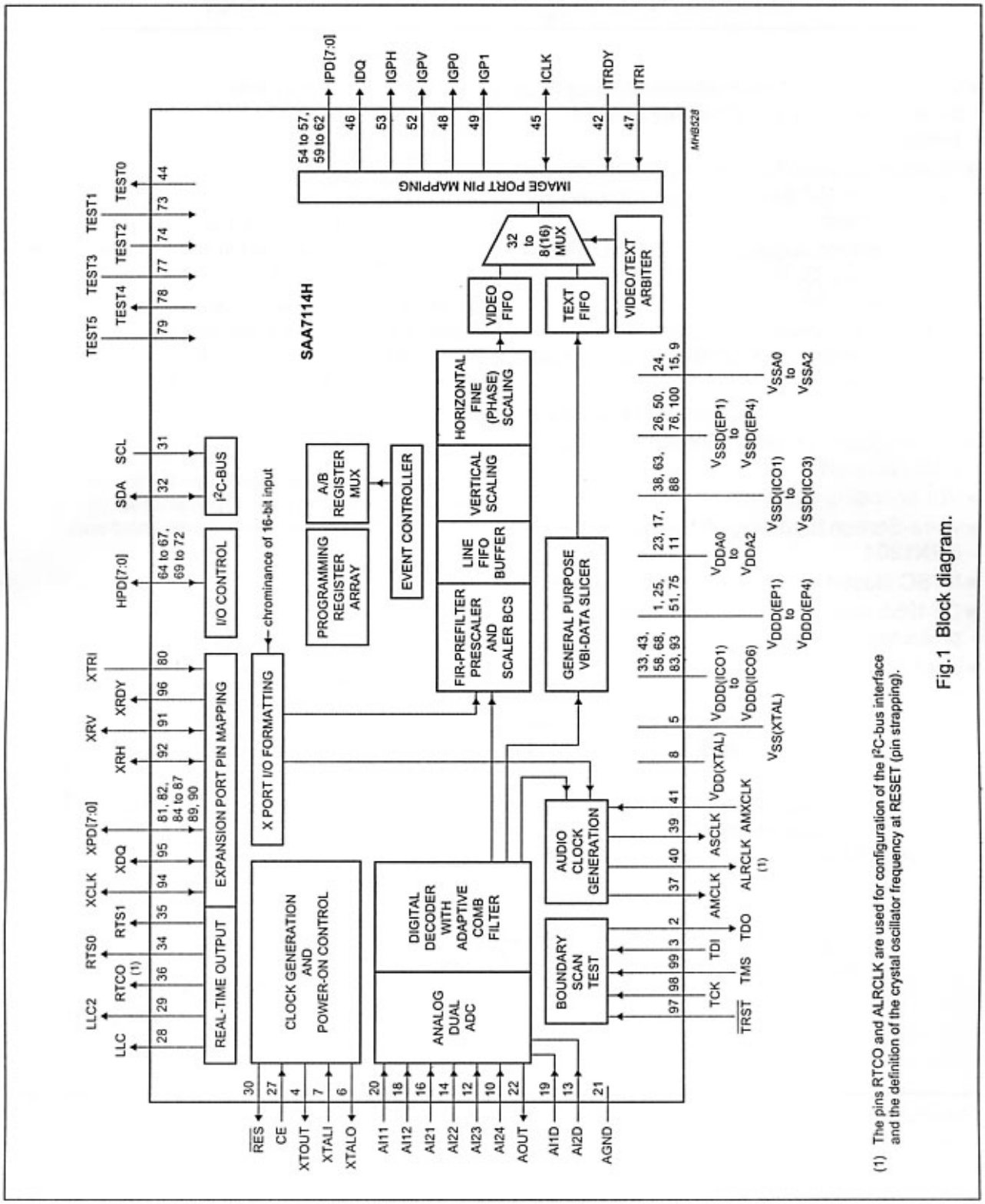


Fig.1 Block diagram.

(1) The pins RTCO and ALRCLK are used for configuration of the I²C-bus interface and the definition of the crystal oscillator frequency at RESET (pin strapping).

7 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
$V_{DDD(EP1)}$	1	P	external digital pad supply voltage 1 (+3.3 V)
TDO	2	O	test data output for boundary scan test; note 1
TDI	3	I	test data input for boundary scan test; note 1
XTOUT	4	O	crystal oscillator output signal; auxiliary signal
$V_{SS(XTAL)}$	5	P	ground for crystal oscillator
XTALO	6	O	24.576 MHz (32.11 MHz) crystal oscillator output; not connected if TTL clock input of XTALI is used
XTALI	7	I	input terminal for 24.576 MHz (32.11 MHz) crystal oscillator or connection of external oscillator with TTL compatible square wave clock signal
$V_{DD(XTAL)}$	8	P	supply voltage for crystal oscillator
V_{SSA2}	9	P	ground for analog inputs AI2n
AI24	10	I	analog input 24
V_{DDA2}	11	P	analog supply voltage for analog inputs AI2n (+3.3 V)
AI23	12	I	analog input 23
AI2D	13	I	differential input for ADC channel 2 (pins AI24, AI23, AI22 and AI21)
AI22	14	I	analog input 22
V_{SSA1}	15	P	ground for analog inputs AI1n
AI21	16	I	analog input 21
V_{DDA1}	17	P	analog supply voltage for analog inputs AI1n (+3.3 V)
AI12	18	I	analog input 12
AI1D	19	I	differential input for ADC channel 1 (pins AI12 and AI11)
AI11	20	I	analog input 11
AGND	21	P	analog ground connection
AOUT	22	O	do not connect; analog test output
V_{DDA0}	23	P	analog supply voltage (+3.3 V) for internal Clock Generation Circuit (CGC)
V_{SSA0}	24	P	ground for internal clock generation circuit
$V_{DDD(EP2)}$	25	P	external digital pad supply voltage 2 (+3.3 V)
$V_{SSD(EP1)}$	26	P	external digital pad supply ground 1
CE	27	I	chip enable or reset input (with internal pull-up)
LLC	28	O	line-locked system clock output (27 MHz nominal)
LLC2	29	O	line-locked ½ clock output (13.5 MHz nominal)
$\overline{RES}$	30	O	reset output (active LOW)
SCL	31	I(/O)	serial clock input (I^2C-bus) with inactive output path
SDA	32	I/O	serial data input/output (I^2C-bus)
$V_{DDD(ICO1)}$	33	P	internal digital core supply voltage 1 (+3.3 V)
RTS0	34	O	real-time status or sync information, controlled by subaddresses 11H and 12H; see Section 15.2.18, 15.2.19 and 15.2.20
RTS1	35	O	

SYMBOL	PIN	TYPE	DESCRIPTION
RTCO	36	(I/)O	real-time control output; contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier frequency and phase and PAL sequence (see external document *"RTC Functional Description"*, available on request); the RTCO pin is enabled via I^2C-bus bit RTCE; see notes 2, 3 and Table 34
AMCLK	37	O	audio master clock output, up to 50% of crystal clock
$V_{SSD(ICO1)}$	38	P	internal digital core supply ground 1
ASCLK	39	O	audio serial clock output
ALRCLK	40	(I/)O	audio left/right clock output; can be strapped to supply via a 3.3 kΩ resistor to indicate that the default 24.576 MHz crystal (ALRCLK = 0; internal pull-down) has been replaced by a 32.110 MHz crystal (ALRCLK = 1); see notes 2 and 4
AMXCLK	41	I	audio master external clock input
ITRDY	42	I	target ready input, image port (with internal pull-up)
$V_{DDD(ICO2)}$	43	P	internal digital core supply voltage 2 (+3.3 V)
TEST0	44	O	do not connect; reserved for future extensions and for testing: scan output
ICLK	45	I/O	clock output signal for image port, or optional asynchronous back-end clock input
IDQ	46	O	output data qualifier for image port (optional: gated clock output)
ITRI	47	I(/O)	image port output control signal, effects all input port pins inclusive ICLK, enable and active polarity is under software control (bits IPE in subaddress 87H); output path used for testing: scan output
IGP0	48	O	general purpose output signal 0; image port (controlled by subaddresses 84H and 85H)
IGP1	49	O	general purpose output signal 1; image port (controlled by subaddresses 84H and 85H)
$V_{SSD(EP2)}$	50	P	external digital pad supply ground 2
$V_{DDD(EP3)}$	51	P	external digital pad supply voltage 3 (+3.3 V)
IGPV	52	O	multi purpose vertical reference output signal; image port (controlled by subaddresses 84H and 85H)
IGPH	53	O	multi purpose horizontal reference output signal; image port (controlled by subaddresses 84H and 85H)
IPD7 to IPD4	54 to 57	O	image port data outputs
$V_{DDD(ICO3)}$	58	P	internal digital core supply voltage 3 (+3.3 V)
IPD3 to IPD0	59 to 62	O	image port data output
$V_{SSD(ICO2)}$	63	P	internal digital core supply ground 2
HPD7 to HPD4	64 to 67	I/O	host port data I/O, carries UV chrominance information in 16-bit video I/O modes
$V_{DDD(ICO4)}$	68	P	internal digital core supply voltage 4 (+3.3 V)
HPD3 to HPD0	69 to 72	I/O	host port data I/O, carries UV chrominance information in 16-bit video I/O modes
TEST1	73	I	do not connect; reserved for future extensions and for testing: scan input
TEST2	74	I	do not connect; reserved for future extensions and for testing: scan input
$V_{DDD(EP4)}$	75	P	external digital pad supply voltage 4 (+3.3 V)
$V_{SSD(EP3)}$	76	P	external digital pad supply ground 3
TEST3	77	I	do not connect; reserved for future extensions and for testing: scan input

SYMBOL	PIN	TYPE	DESCRIPTION
TEST4	78	O	do not connect; reserved for future extensions and for testing: scan output
TEST5	79	I	do not connect; reserved for future extensions and for testing: scan input
XTRI	80	I	X-port output control signal, affects all X-port pins (XPD7 to XPD0, XRH, XRV, XDQ and XCLK), enable and active polarity is under software control (bits XPE in subaddress 83H)
XPD7	81	I/O	expansion port data
XPD6	82	I/O	expansion port data
$V_{DDD(ICO5)}$	83	P	internal digital core supply voltage 5 (+3.3 V)
XPD5 to XPD2	84 to 87	I/O	expansion port data
$V_{SSD(ICO3)}$	88	P	internal digital core supply ground 3
XPD1	89	I/O	expansion port data
XPD0	90	I/O	expansion port data
XRV	91	I/O	vertical reference I/O expansion port
XRH	92	I/O	horizontal reference I/O expansion port
$V_{DDD(ICO6)}$	93	P	internal digital core supply voltage 6 (+3.3 V)
XCLK	94	I/O	clock I/O expansion port
XDQ	95	I/O	data qualifier I/O expansion port
XRDY	96	O	task flag or ready signal from scaler, controlled by XRQT
TRST	97	I	test reset input (active LOW), for boundary scan test (with internal pull-up); notes 5 and 6
TCK	98	I	test clock for boundary scan test; note 1
TMS	99	I	test mode select input for boundary scan test or scan test; note 1
$V_{SSD(EP4)}$	100	P	external digital pad supply ground 4

Notes

1. In accordance with the *"IEEE1149.1"* standard the pads TDI, TMS, TCK and $\overline{\text{TRST}}$ are input pads with an internal pull-up transistor and TDO is a 3-state output pad.
2. Pin strapping is done by connecting the pin to supply via a 3.3 kΩ resistor. During the power-up reset sequence the corresponding pins are switched to input mode to read the strapping level. For the default setting no strapping resistor is necessary (internal pull-down).
3. Pin RTCO: operates as I^2C-bus slave address pin; RTCO = 0 slave address 42H/43H (default); RTCO = 1 slave address 40H/41H.
4. Pin ALRCLK: 0 = 24.576 MHz crystal (default); 1 = 32.110 MHz crystal.
5. For board design without boundary scan implementation connect the $\overline{\text{TRST}}$ pin to ground.
6. This pin provides easy initialization of the Boundary Scan Test (BST) circuit. $\overline{\text{TRST}}$ can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.

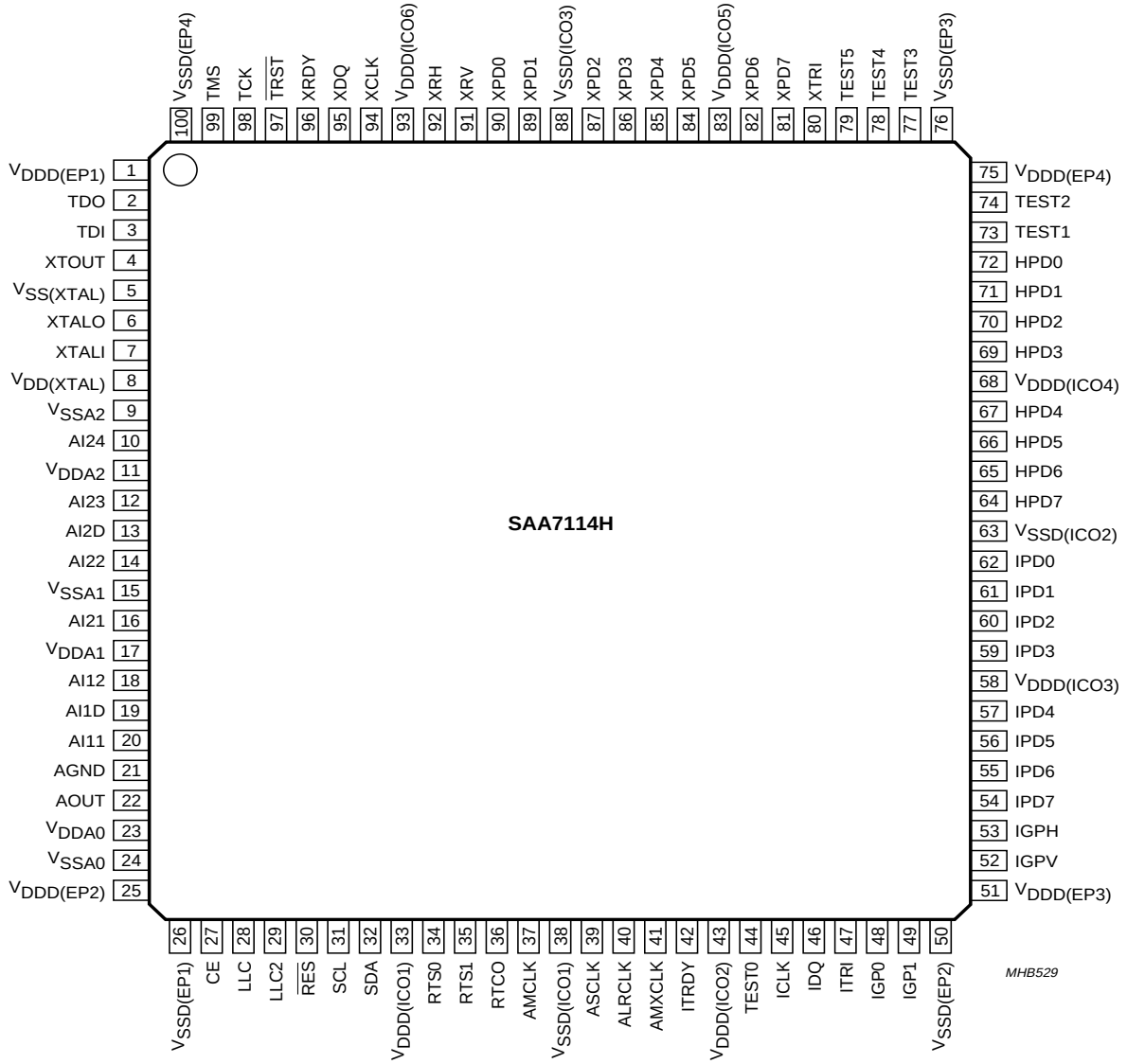


Fig.2 Pin configuration.

8-Pin, Stereo A/D Converter for Digital Audio

Features

- Single +5 V Power Supply
- 18-Bit Resolution
- 94 dB Dynamic Range
- Linear Phase Digital Anti-Alias Filtering
  0.05dB Passband Ripple
  80dB Stopband Rejection
- Low Power Dissipation: 150 mW
  Power-Down Mode for Portable Applications
- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz

General Description

The CS5330A / 31A is a complete stereo analog-to-digital converter which performs anti-alias filtering, sampling and analog-to-digital conversion generating 18-bit values for both left and right inputs in serial form. The output sample rate can be infinitely adjusted between 2 and 50 kHz.

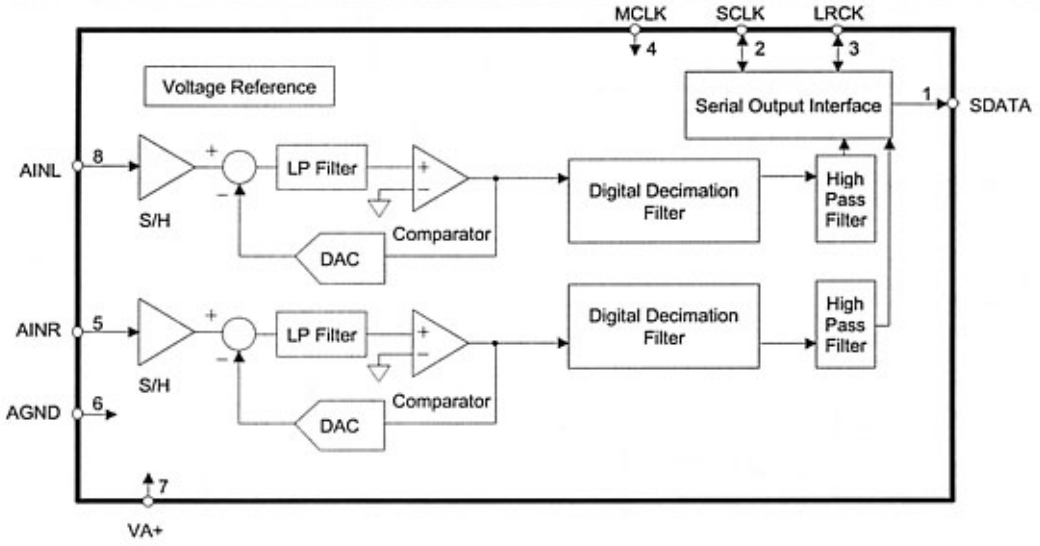
The CS5330A / 31A operates from a single +5V supply and requires only 150 mW for normal operation, making it ideal for battery-powered applications.

The ADC uses delta-sigma modulation with 128X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The linear-phase digital filter has a passband to 21.7 kHz, 0.05 dB passband ripple and >80 dB stopband rejection. The device also contains a high pass filter to remove DC offsets.

The device is available in a 0.208" wide, 8-pin surface mount package.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS5330A-KS	-10° to 70°C	8-pin plastic SOIC
CS5331A-KS	-10° to 70°C	8-pin plastic SOIC
CS5330A-BS	-40° to +85°C	8-pin plastic SOIC
CS5331A-BS	-40° to +85°C	8-pin plastic SOIC



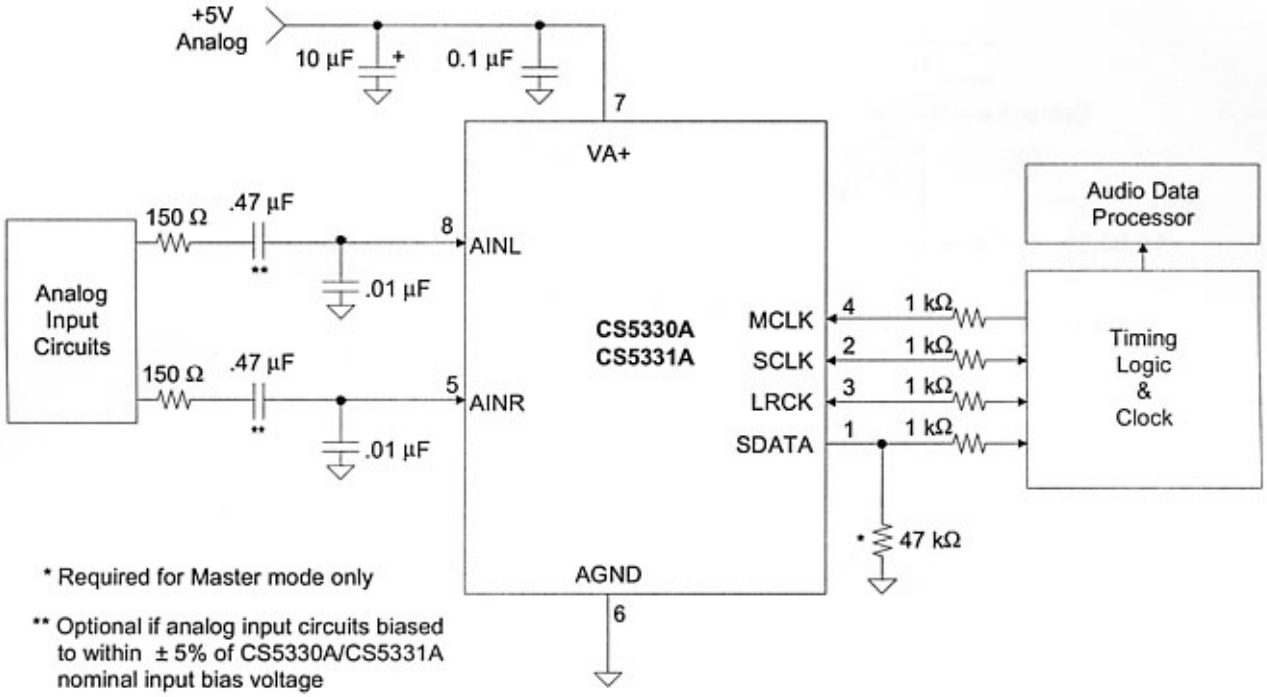


Figure 1. Typical Connection Diagram

1. General description

The PCF8563 is a CMOS real time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage-low detector are also provided. All address and data are transferred serially via a two-line bidirectional I^2C-bus. Maximum bus speed is 400 kbit/s. The built-in word address register is incremented automatically after each written or read data byte.

2. Features

- Provides year, month, day, weekday, hours, minutes and seconds based on 32.768 kHz quartz crystal
- Century flag
- Clock operating voltage: 1.8 to 5.5 V
- Low backup current; typical 0.25 μA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 400 kHz two-wire I^2C-bus interface (at V_{DD} = 1.8 to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz and 1 Hz)
- Alarm and timer functions
- Integrated oscillator capacitor
- Internal power-on reset
- I^2C-bus slave address: read A3H and write A2H
- Open-drain interrupt pin.

3. Applications

- Mobile telephones
- Portable instruments
- Fax machines
- Battery powered products.

Block diagram

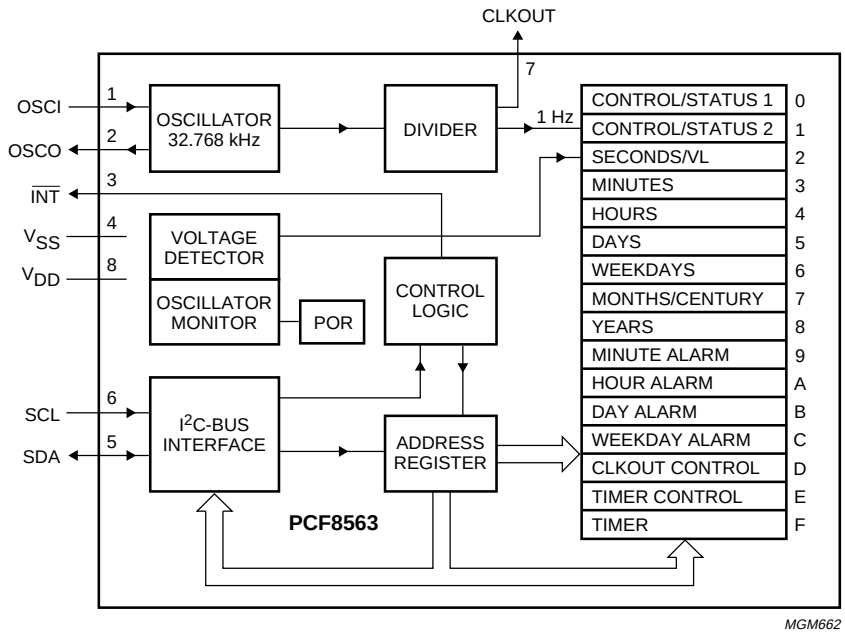


Fig 1. Block diagram.

Pinning information

Pinning

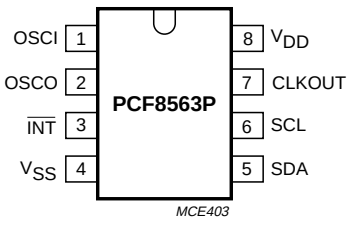


Fig 2. Pin configuration DIP8.

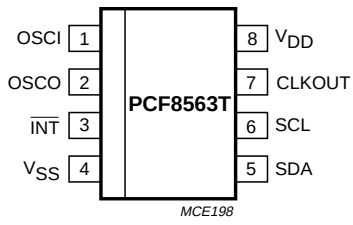


Fig 3. Pin configuration SO8.

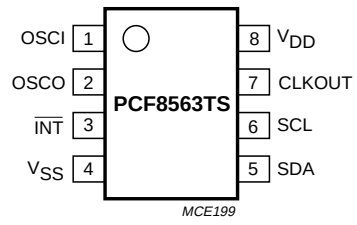


Fig 4. Pin configuration TSSOP8.

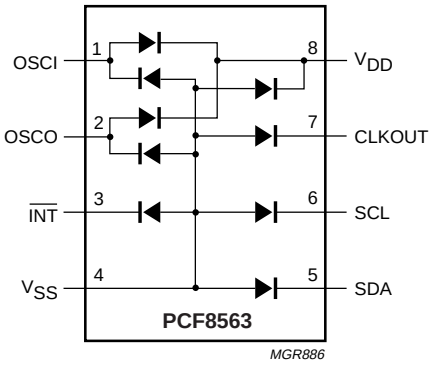


Fig 5. Device diode protection diagram.

Pin description

Table 3: Pin description

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
$\overline{INT}$	3	interrupt output (open-drain; active LOW)
V_{SS}	4	ground
SDA	5	serial data input and output
SCL	6	serial clock input
CLKOUT	7	clock output, open-drain
V_{DD}	8	positive supply voltage

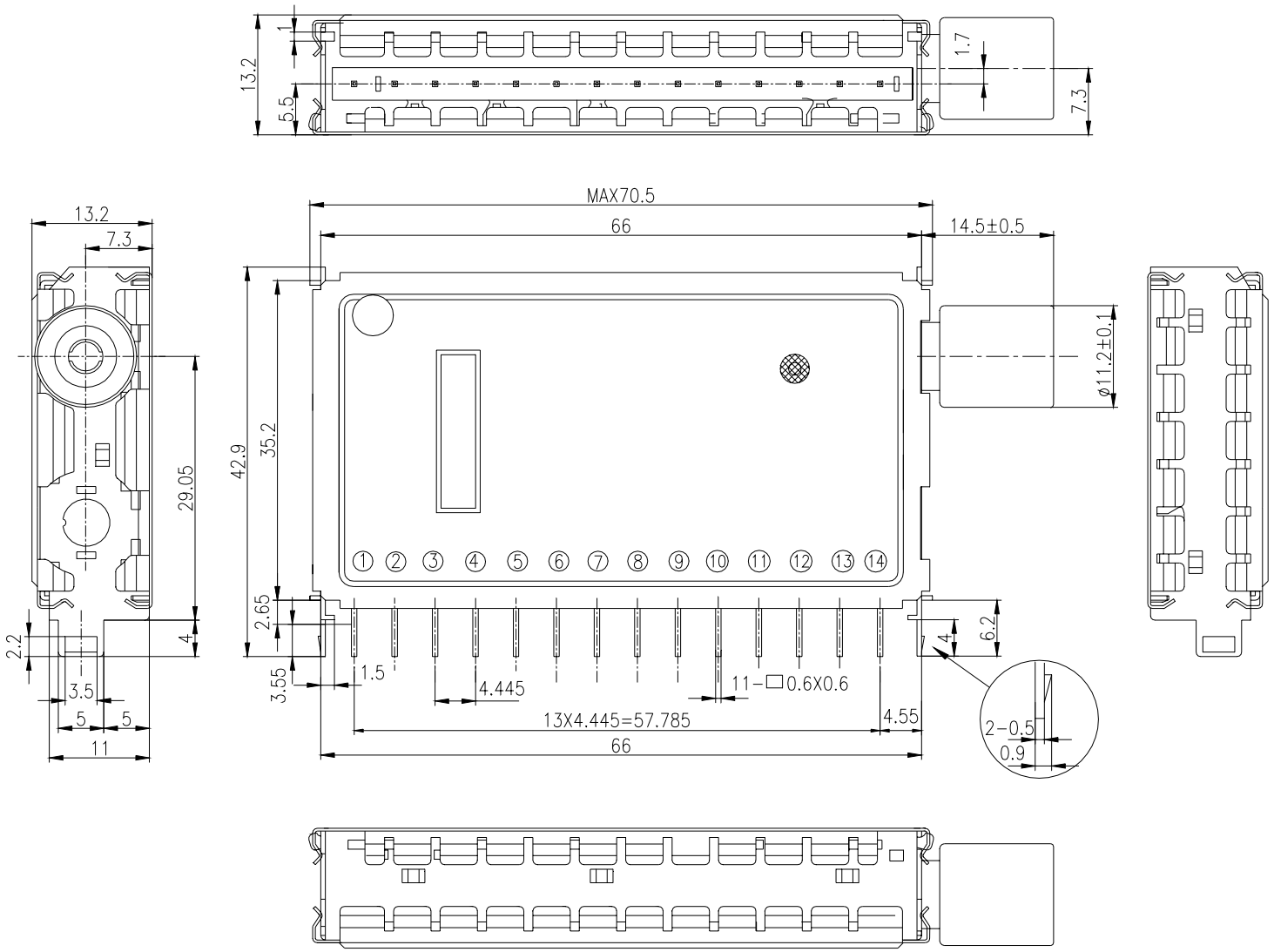
Functional description

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the Real Time Clock/calender (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C-bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00H and 01H) are used as control and/or status registers. The memory addresses 02H through 08H are used as counters for the clock function (seconds up to years counters). Address locations 09H through 0CH contain alarm registers which define the conditions for an alarm. Address 0DH controls the CLKOUT output frequency. 0EH and 0FH are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.


13.2
1
5.5
1.7
7.3
MAX70.5
66
14.5±0.5
13.2
7.3
29.05
42.9
35.2
ø11.2±0.1
2.65
2.2
4
3.5
5
5
11
3.55
1.5
4.445
11-□0.6X0.6
13X4.445=57.785
4.55
66
6.2
4
2-0.5
0.9
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪ ⑫ ⑬ ⑭

DESCRIPTION

PT6312 is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/4 to 1/11 duty factor. Eleven segment output lines, 6 grid output lines, 5 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6312 via a three-line serial interface. It is housed in a 44-pin plastic QFP or LQFP Package and is functionally compatible with µpD16312.

FEATURES

- ❒ CMOS Technology
- ❒ Low Power Consumption
- ❒ Key Scanning (6 x 4 matrix)
- ❒ Multiple Display Modes: (11 segments, 11 digits to 16 segments, 6 digits)
- ❒ 8-Step Dimming Circuitry
- ❒ LED Ports Provided (4 channels, 20 mA max.)
- ❒ 4- Bits General Purpose Input Ports Provided
- ❒ Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- ❒ No External Resistors Needed for Driver Outputs
- ❒ Functional Compatibility with µpD16312
- ❒ Available in 44-pin, QFP or LQFP Package

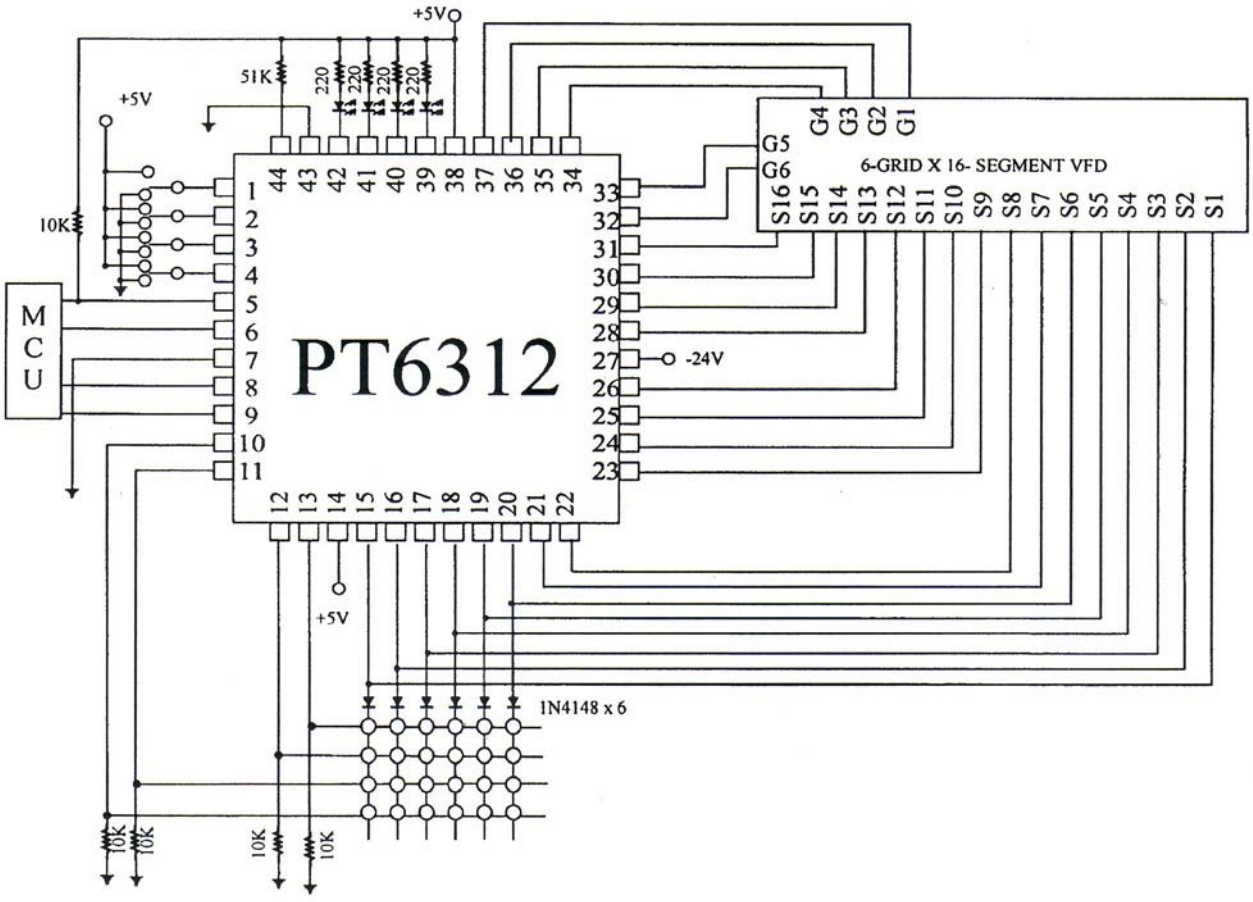
APPLICATION

- ❒ Micro-computer Peripheral Device

ORDER INFORMATION

Valid Part Number	Package Type
PT6312	44 pins, QFP Package
PT6312LQ	44 pins, LQFP Package

6-GRID X 16-SEGMENT VFD APPLICATION CIRCUIT



U201
MT1388E

Subsystem Configuration

Dual Drive Support

Two drives may be accessed via a common interface cable, using the same range of I/O addresses. The drives have a jumper configuration as device 0 or 1 (Master/Slave), and are selected by the drive select bit in the Device/Head register of the task file.

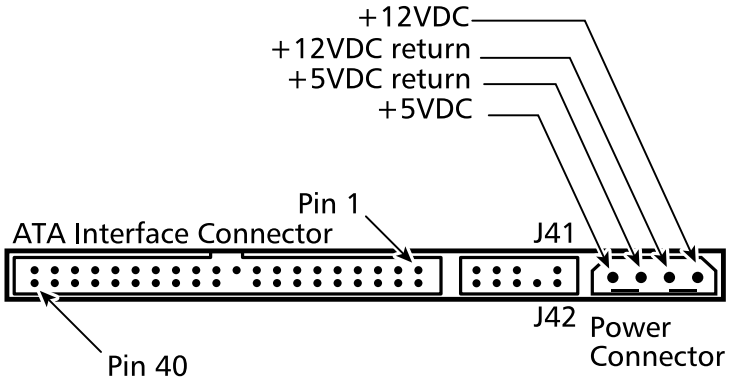
All Task File registers are written in parallel to both drives. The interface processor on each drive decides whether a command written to it should be executed; this depends on the type of command and which drive is selected. Only the drive selected executes the command and activates the data bus in response to host I/O reads; the drive not selected remains inactive.

A master/slave relationship exists between the two drives: device 0 is the master and device 1 the slave. When the Master is closed (factory default, figure 2-1), the drive assumes the role of master; when open, the drive acts as a slave. In single drive configurations, the Master jumper must be closed.

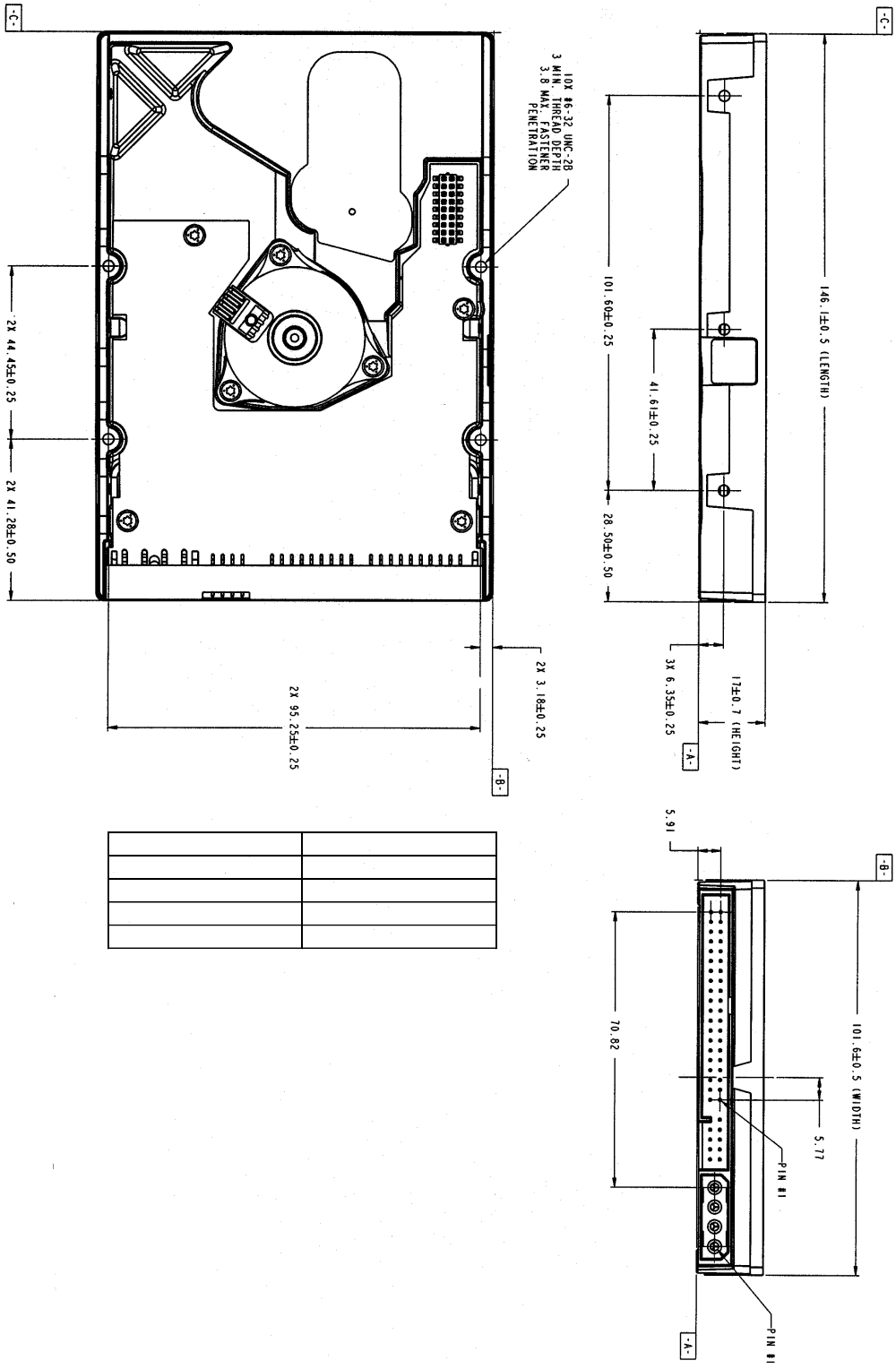
Cable Select Option

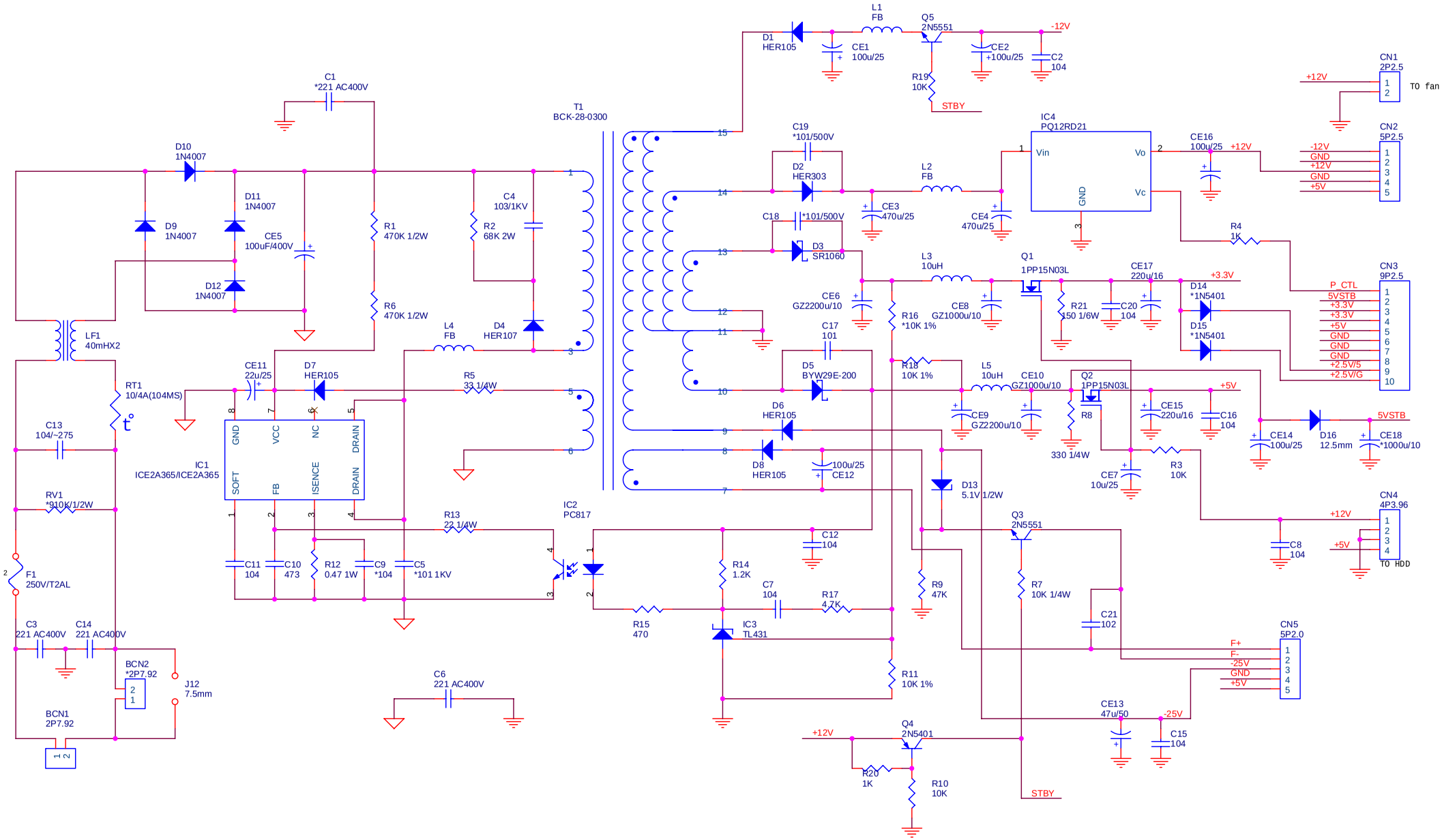
CSEL (cable select) is an optional feature per ANSI ATA specification. Drives configured in a multiple drive system are identified by CSEL's value:

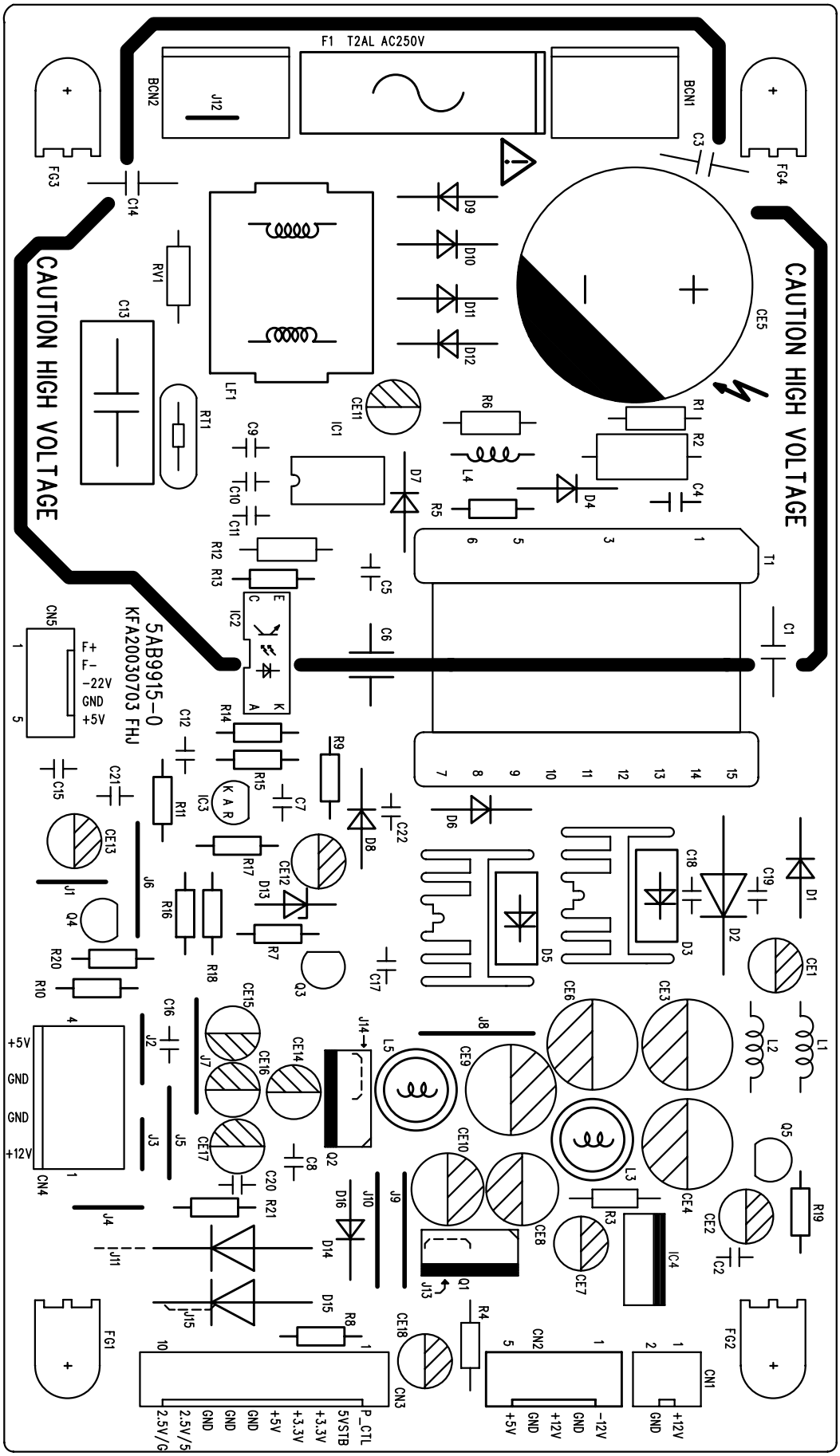
– If CSEL is grounded, then the drive address is 0.
– If CSEL is open, then the drive address is 1.

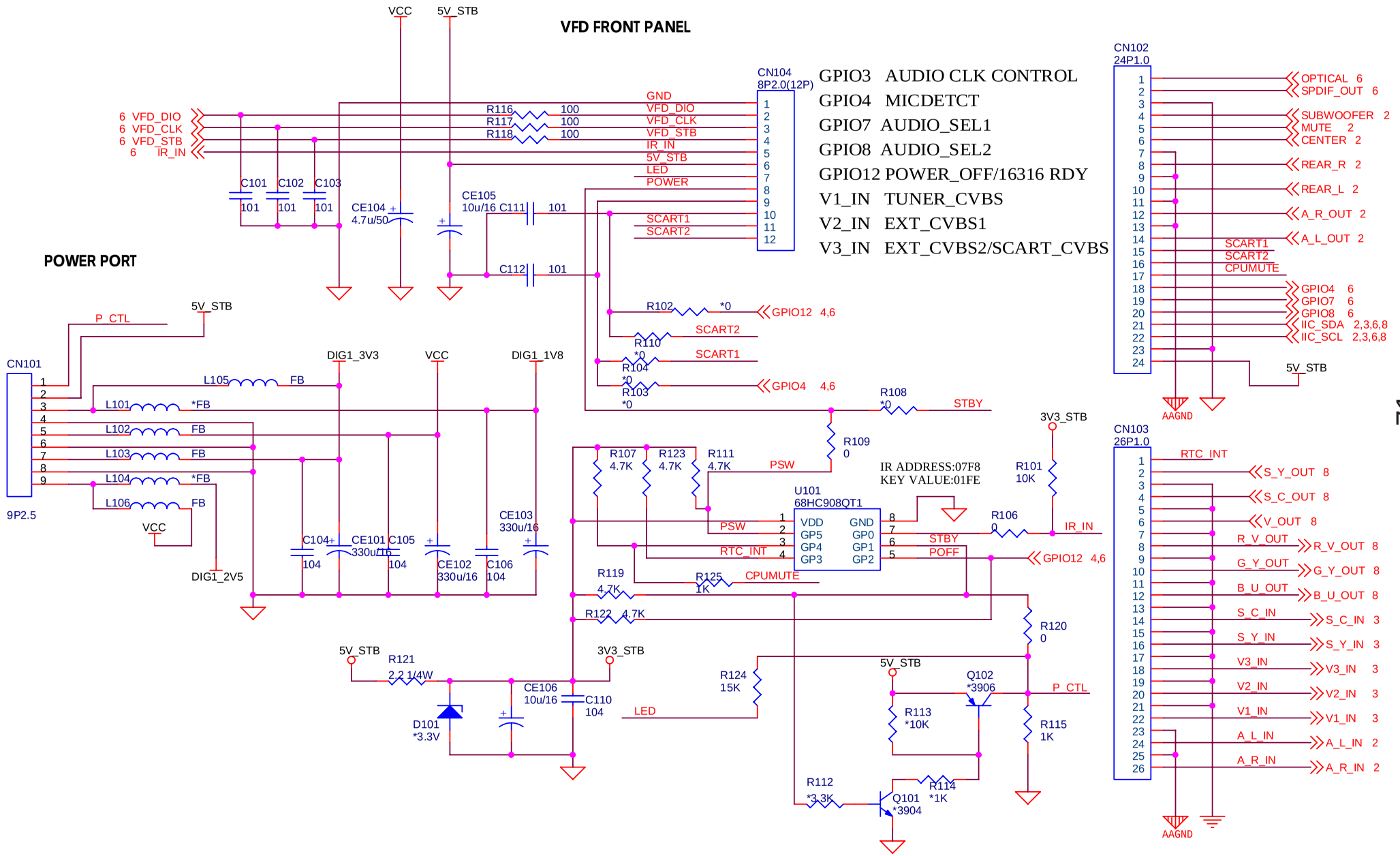


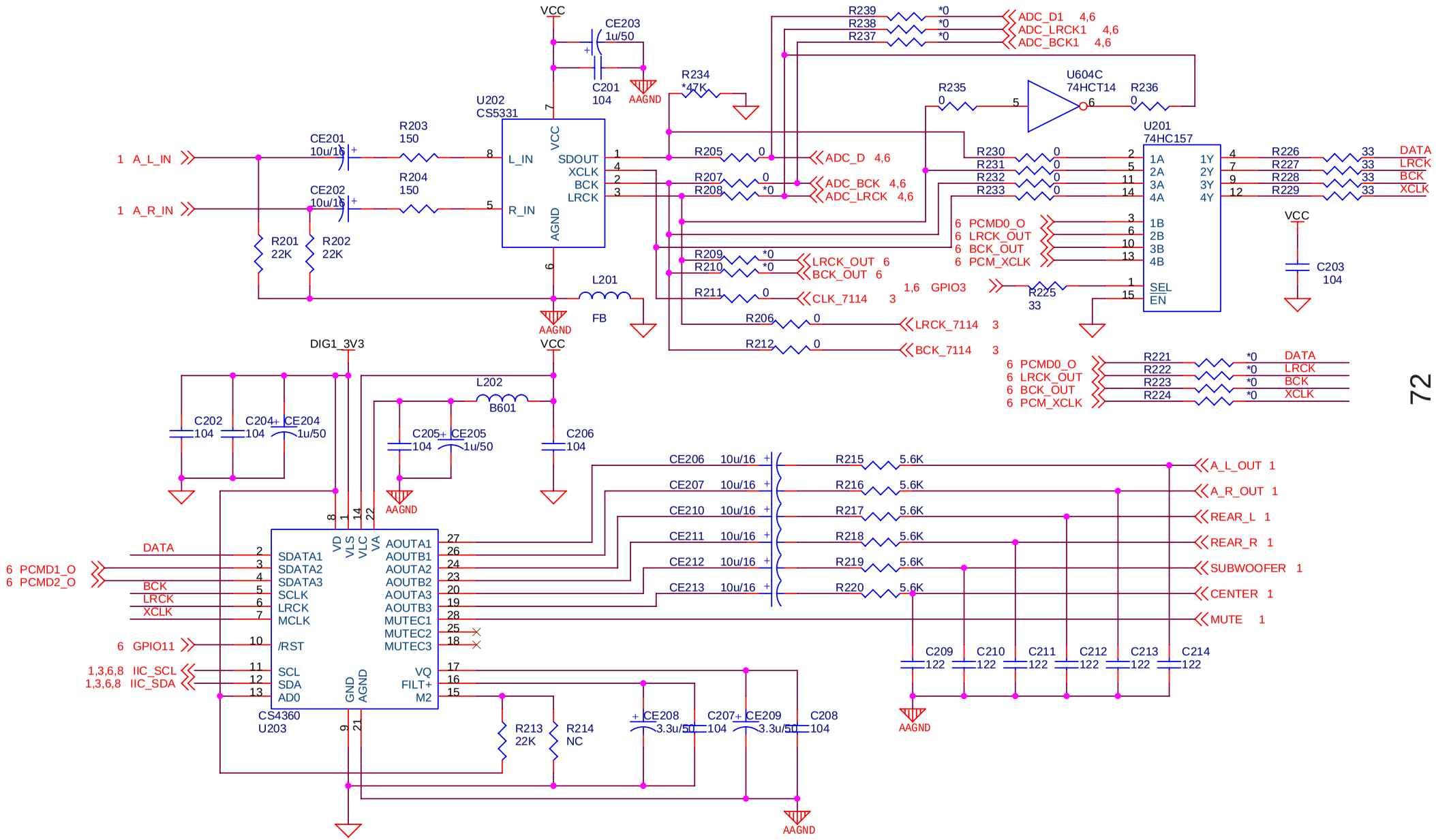
PCBA Jumper Location and Configuration

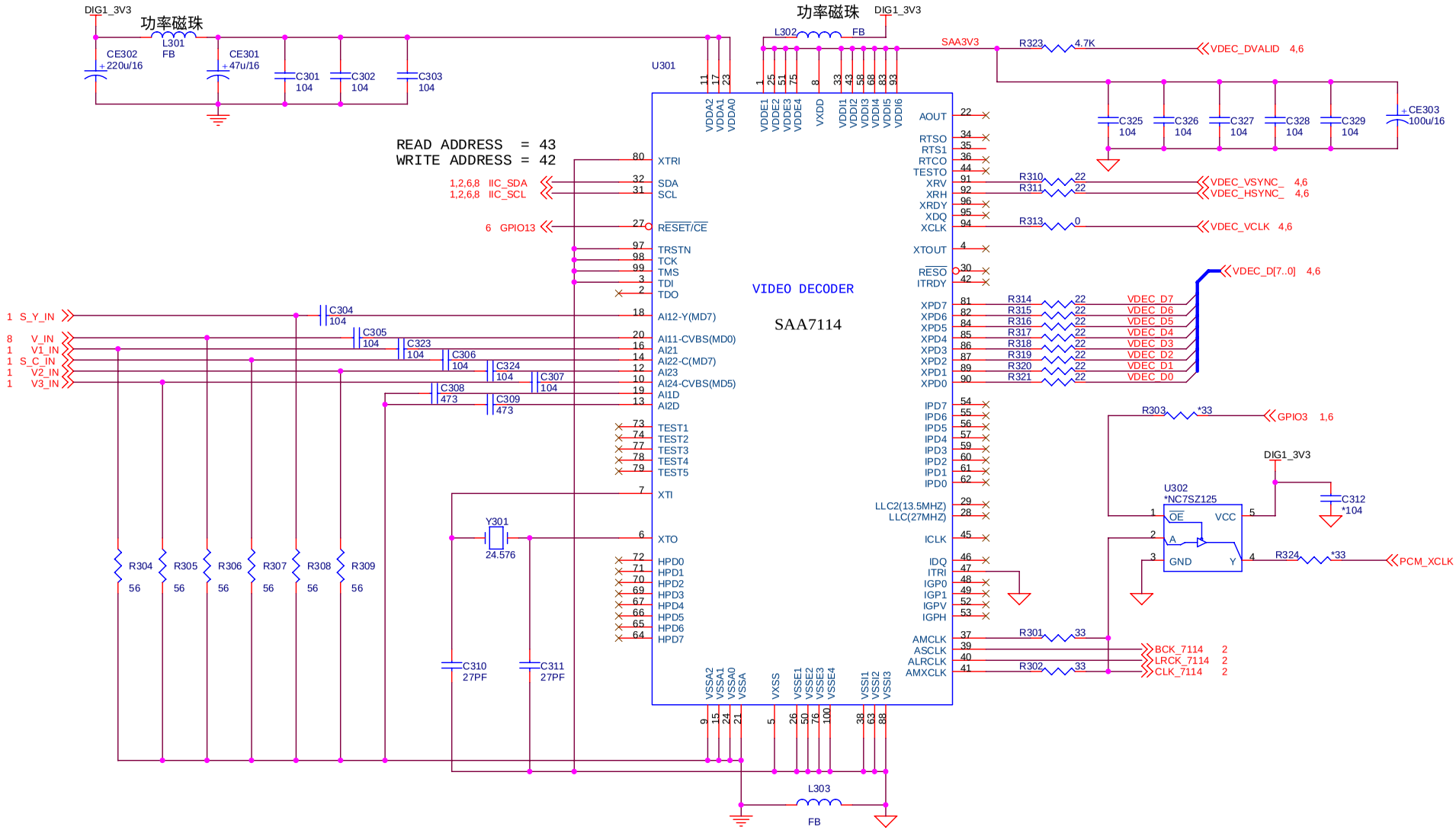

-C-
10X #6-32 UNC-2B
3 MIN. THREAD DEPTH
3.8 MAX. FASTENER
PENETRATION
2X 44.45±0.25
2X 41.28±0.50
2X 95.25±0.25
2X 3.18±0.25
-B-
101.60±0.25
41.61±0.25
28.50±0.50
146.1±0.5 (LENGTH)
3X 6.35±0.25
17±0.7 (HEIGHT)
-A-
5.91
70.82
101.6±0.5 (WIDTH)
5.77
PIN #1
PIN #1

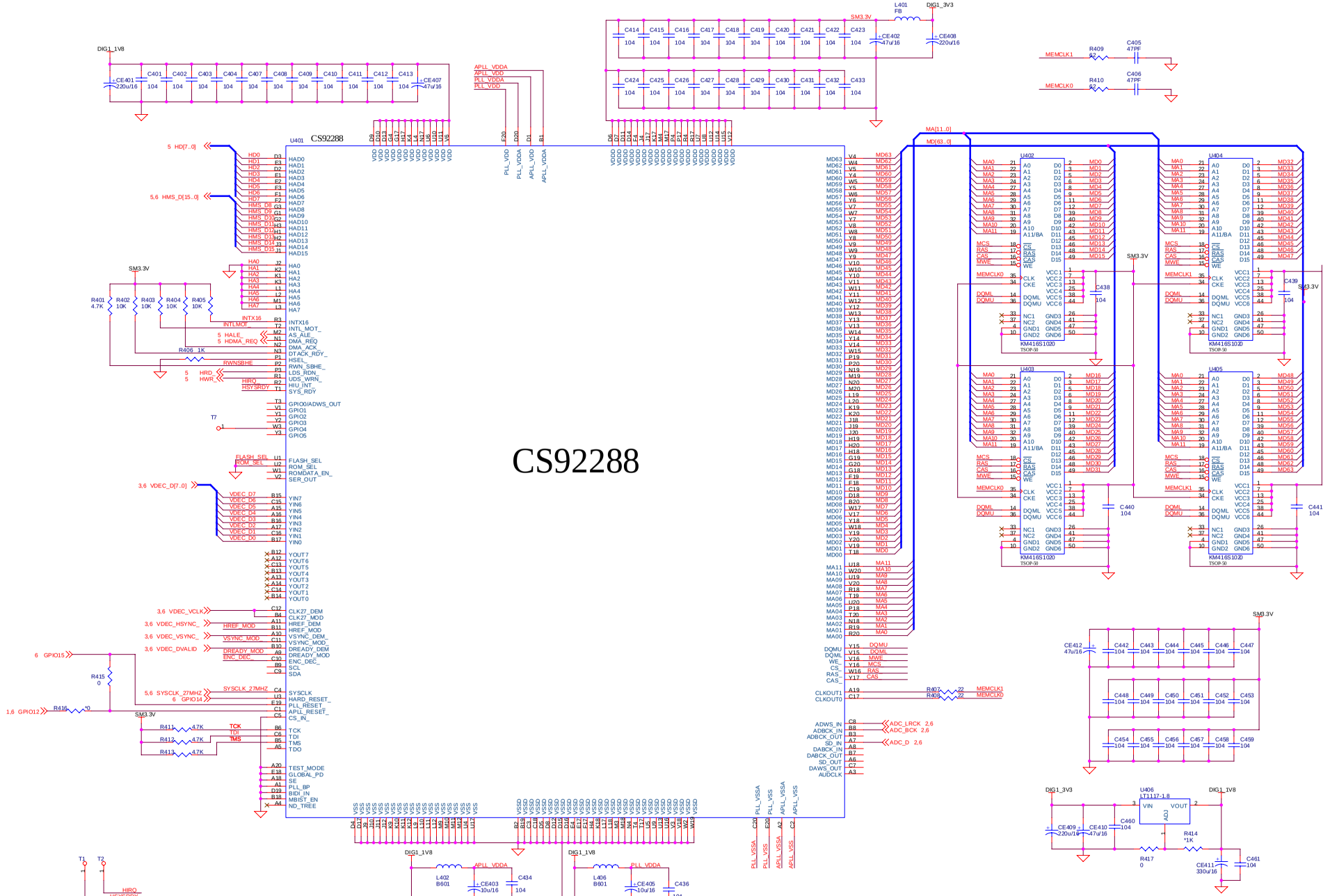

C1
*221 AC400V
T1
BCK-28-0300
L1
FB
D1
HER105
CE1
100u/25
Q5
2N5551
-12V
CE2
+100u/25
C2
104
R19
10K
STBY
CN1
2P2.5
+12V
TO fan
CN2
5P2.5
-12V
GND
+12V
GND
+5V
D10
1N4007
D11
1N4007
D9
1N4007
CE5
100uF/400V
D12
1N4007
R1
470K 1/2W
R6
470K 1/2W
R2
68K 2W
C4
103/1KV
D4
HER107
L4
FB
LF1
40mHX2
RT1
10/4A(104MS)
CE11
22u/25
D7
HER105
R5
33 1/4W
C13
104/~275
IC1
ICE2A365/ICE2A365
GND
VCC
NC
DRAIN
SOFT
FB
ISENCE
DRAIN
RV1
*910K/1/2W
F1
250V/T2AL
C3
221 AC400V
C14
221 AC400V
BCN2
*2P7.92
J12
7.5mm
BCN1
2P7.92
C11
104
C10
473
R12
0.47 1W
C9
*104
C5
*101 1KV
R13
22 1/4W
C6
221 AC400V
IC2
PC817
R15
470
C19
*101/500V
D2
HER303
C18
*101/500V
D3
SR1060
CE3
470u/25
L2
FB
CE4
470u/25
IC4
PQ12RD21
Vin
Vo
GND
Vc
CE16
100u/25
+12V
R4
1K
L3
10uH
Q1
1PP15N03L
CE17
220u/16
+3.3V
CE6
GZ2200u/10
R16
*10K 1%
CE8
GZ1000u/10
R21
150 1/6W
C20
104
D14
*1N5401
D15
*1N5401
CN3
9P2.5
P_CTL
5VSTB
+3.3V
+3.3V
+5V
GND
GND
GND
+2.5V/5
+2.5V/G
C17
101
D5
BYW29E-200
R18
10K 1%
L5
10uH
CE10
GZ1000u/10
Q2
1PP15N03L
+5V
D6
HER105
CE9
GZ2200u/10
R8
330 1/4W
CE15
220u/16
C16
104
CE14
100u/25
D16
12.5mm
5VSTB
CE18
*1000u/10
D8
HER105
100u/25
CE12
CE7
10u/25
R3
10K
D13
5.1V 1/2W
CN4
4P3.96
+12V
+5V
TO HDD
C8
104
C12
104
Q3
2N5551
R14
1.2K
C7
104
R17
4.7K
R9
47K
R7
10K 1/4W
C21
102
IC3
TL431
R11
10K 1%
CN5
5P2.0
F+
F-
-25V
GND
+5V
CE13
47u/50
-25V
C15
104
+12V
Q4
2N5401
R20
1K
R10
10K
STBY

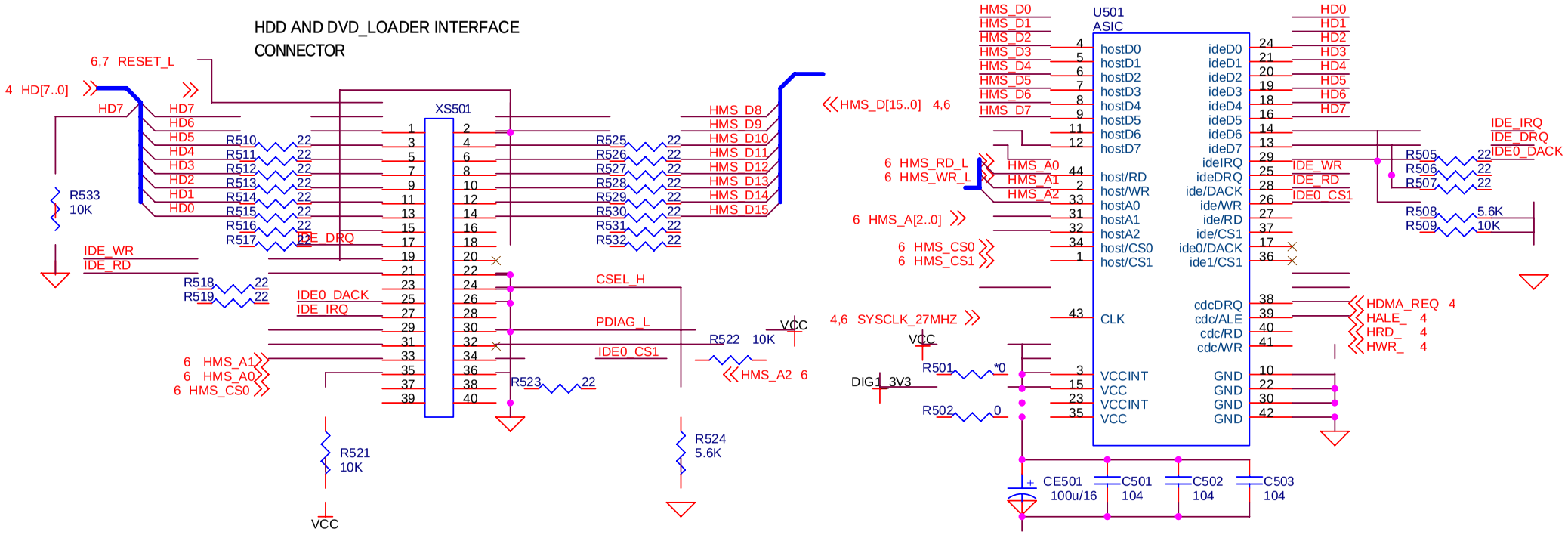

F1 T2AL AC250V
CAUTION HIGH VOLTAGE
CAUTION HIGH VOLTAGE
5AB9915-0
KFA20030703 FHJ
CN5
F+
F-
-22V
GND
+5V
CN4
+5V
GND
GND
+12V
CN2
+12V
GND
-12V
CN1
+12V
GND
CN3
P_CTL
5VSTB
+3.3V
+3.3V
+5V
GND
GND
GND
2.5V/5
2.5V/G
T1
IC1
IC2
IC3
IC4
LF1
RT1
RV1
Q1
Q2
Q3
Q4
Q5
BCN1
BCN2
FG1
FG2
FG3
FG4

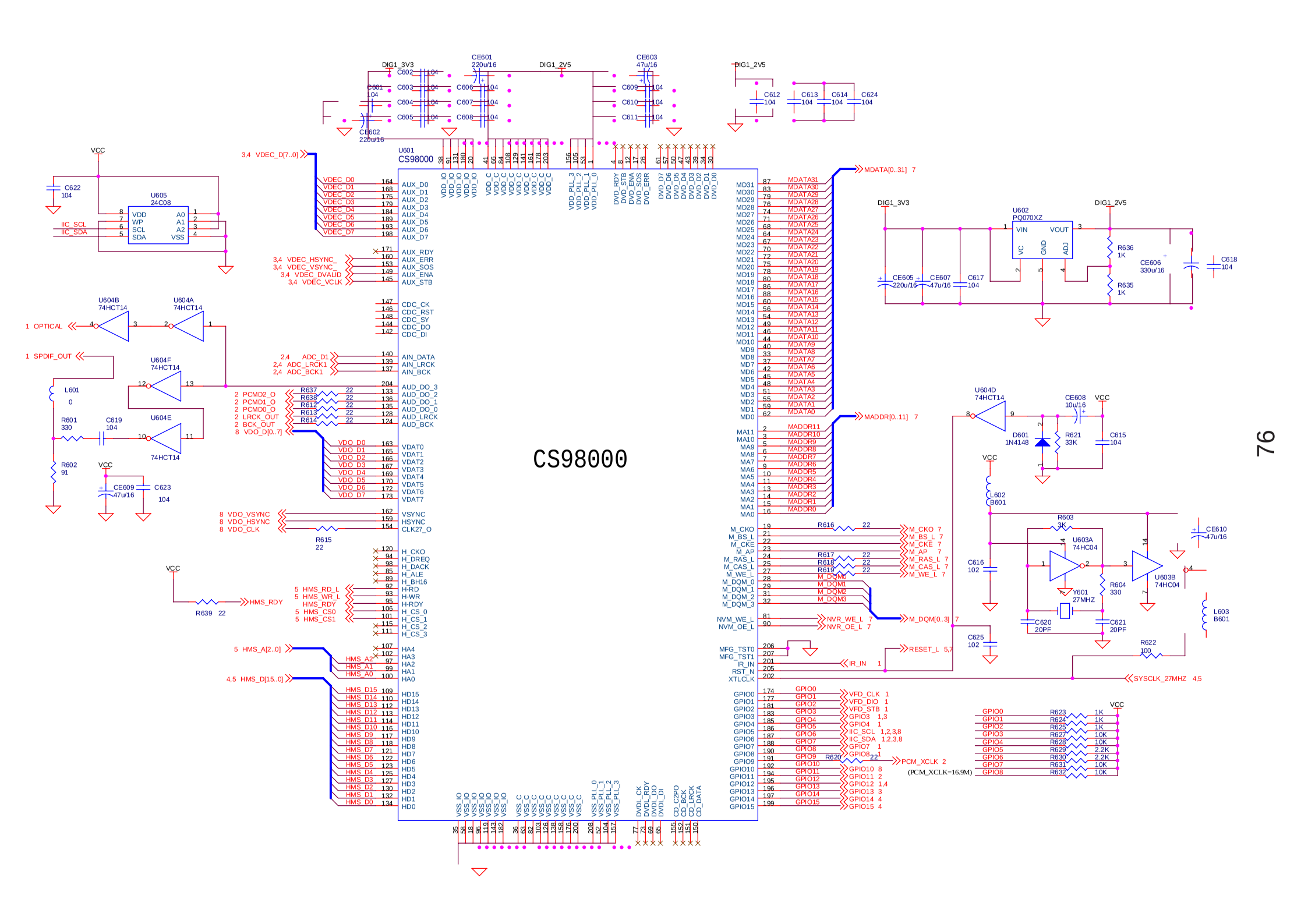

VFD FRONT PANEL
POWER PORT
GPIO3 AUDIO CLK CONTROL
GPIO4 MICDETCT
GPIO7 AUDIO_SEL1
GPIO8 AUDIO_SEL2
GPIO12 POWER_OFF/16316 RDY
V1_IN TUNER_CVBS
V2_IN EXT_CVBS1
V3_IN EXT_CVBS2/SCART_CVBS
IR ADDRESS:07F8
KEY VALUE:01FE
CN101
CN102 24P1.0
CN103 26P1.0
CN104 8P2.0(12P)
U101 68HC908QT1
VCC
5V_STB
3V3_STB
DIG1_3V3
DIG1_1V8
DIG1_2V5
AAGND
VFD_DIO
VFD_CLK
VFD_STB
IR_IN
LED
POWER
SCART1
SCART2
CPUMUTE
STBY
PSW
RTC_INT
POFF
P_CTL
OPTICAL 6
SPDIF_OUT 6
SUBWOOFER 2
MUTE 2
CENTER 2
REAR_R 2
REAR_L 2
A_R_OUT 2
A_L_OUT 2
GPIO4 6
GPIO7 6
GPIO8 6
IIC_SDA 2,3,6,8
IIC_SCL 2,3,6,8
S_Y_OUT 8
S_C_OUT 8
V_OUT 8
R_V_OUT 8
G_Y_OUT 8
B_U_OUT 8
S_C_IN 3
S_Y_IN 3
V3_IN 3
V2_IN 3
V1_IN 3
A_L_IN 2
A_R_IN 2
R101 10K
R102 *0
R103 *0
R104 *0
R106 0
R107 4.7K
R108 *0
R109 0
R110 *0
R111 4.7K
R112 *3.3K
R113 *10K
R114 *1K
R115 1K
R119 4.7K
R120 0
R121 2.2 1/4W
R122 4.7K
R123 4.7K
R124 15K
R125 1K
Q101 *3904
Q102 *3906
D101 *3.3V
C101 101
C102 101
C103 101
C104 104
C105 104
C106 104
C110 104
C111 101
C112 101
CE101 330u/16
CE102 330u/16
CE103 330u/16
CE104 4.7u/50
CE105 10u/16
CE106 10u/16
L101 *FB
L102 FB
L103 FB
L104 *FB
L105 FB
L106 FB
9P2.5

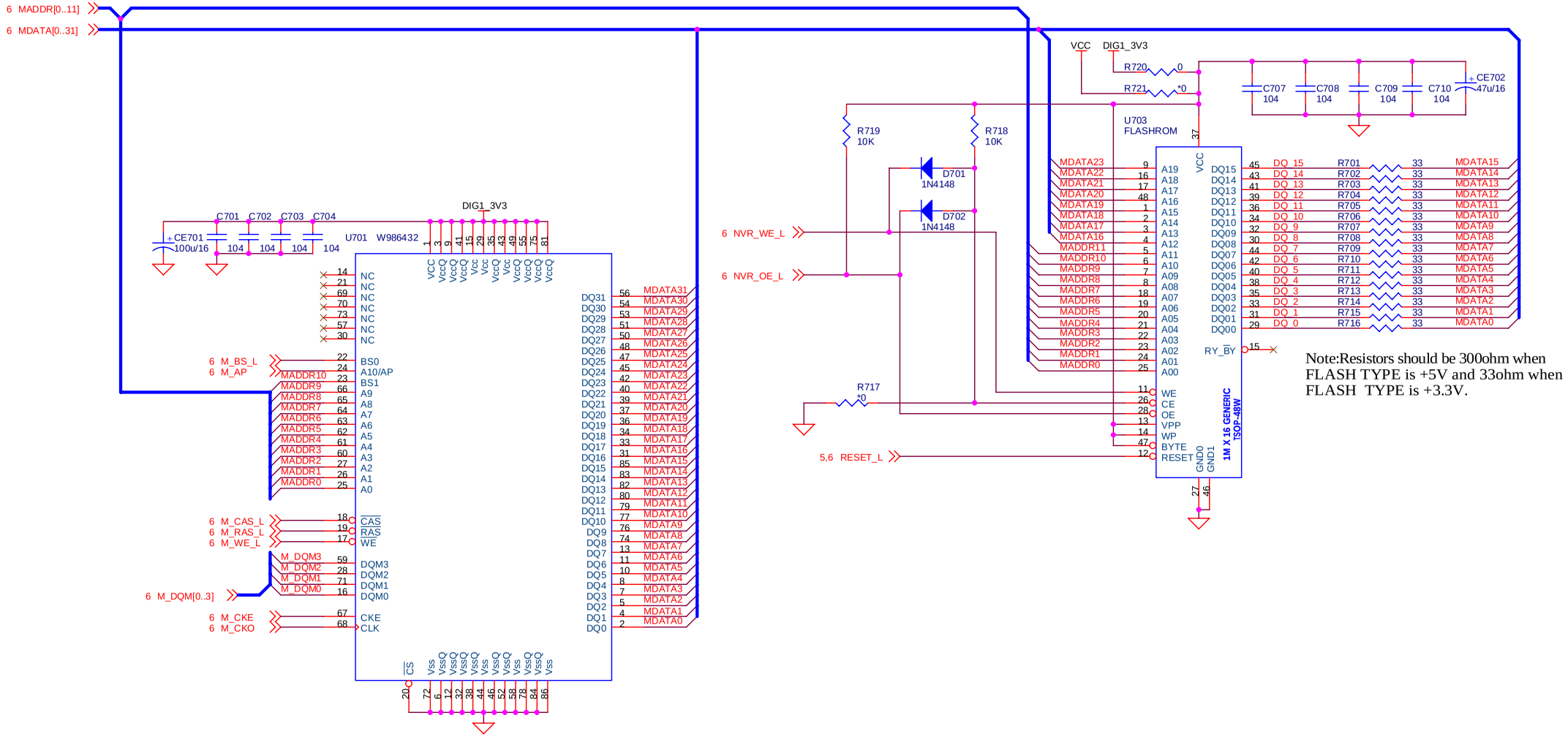

VCC
CE203 1u/50
C201 104
AAGND
U202 CS5331
R234 *47K
R239 *0
R238 *0
R237 *0
ADC_D1 4,6
ADC_LRCK1 4,6
ADC_BCK1 4,6
U604C 74HCT14
R235 0
R236 0
U201 74HC157
1 A_L_IN
1 A_R_IN
CE201 10u/16
CE202 10u/16
R203 150
R204 150
L_IN
R_IN
SDOUT
XCLK
BCK
LRCK
VCC
AGND
R201 22K
R202 22K
R205 0
R207 0
R208 *0
ADC_D 4,6
ADC_BCK 4,6
ADC_LRCK 4,6
R230 0
R231 0
R232 0
R233 0
R226 33
R227 33
R228 33
R229 33
DATA
LRCK
BCK
XCLK
6 PCMD0_O
6 LRCK_OUT
6 BCK_OUT
6 PCM_XCLK
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
SEL
EN
R209 *0
R210 *0
LRCK_OUT 6
BCK_OUT 6
R211 0
CLK_7114 3
1,6 GPIO3
R225 33
C203 104
L201
FB
R206 0
LRCK_7114 3
R212 0
BCK_7114 3
R221 *0
R222 *0
R223 *0
R224 *0
DIG1_3V3
L202
B601
C202 104
C204 104
CE204 1u/50
C205 104
CE205 1u/50
C206 104
CE206 10u/16
CE207 10u/16
CE210 10u/16
CE211 10u/16
CE212 10u/16
CE213 10u/16
R215 5.6K
R216 5.6K
R217 5.6K
R218 5.6K
R219 5.6K
R220 5.6K
A_L_OUT 1
A_R_OUT 1
REAR_L 1
REAR_R 1
SUBWOOFER 1
CENTER 1
MUTE 1
C209 122
C210 122
C211 122
C212 122
C213 122
C214 122
DATA
6 PCMD1_O
6 PCMD2_O
BCK
LRCK
XCLK
6 GPIO11
1,3,6,8 IIC_SCL
1,3,6,8 IIC_SDA
SDATA1
SDATA2
SDATA3
SCLK
LRCK
MCLK
/RST
SCL
SDA
AD0
VD
VLS
VLC
VA
GND
AGND
AOUTA1
AOUTB1
AOUTA2
AOUTB2
AOUTA3
AOUTB3
MUTEC1
MUTEC2
MUTEC3
VQ
FILT+
M2
CS4360
U203
R213 22K
R214 NC
CE208 3.3u/50
C207 104
CE209 3.3u/50
C208 104


DIG1_3V3
功率磁珠
L301
FB
CE302
220u/16
CE301
47u/16
C301
104
C302
104
C303
104
功率磁珠
DIG1_3V3
L302
FB
SAA3V3
R323
4.7K
VDEC_DVALID 4,6
C325
104
C326
104
C327
104
C328
104
C329
104
CE303
100u/16
U301
READ ADDRESS = 43
WRITE ADDRESS = 42
VIDEO DECODER
SAA7114
1,2,6,8 IIC_SDA
1,2,6,8 IIC_SCL
6 GPIO13
R310
R311
R313
VDEC_VSYNC_ 4,6
VDEC_HSYNC_ 4,6
VDEC_VCLK 4,6
VDEC_D[7..0] 4,6
1 S_Y_IN
8 V_IN
1 V1_IN
1 S_C_IN
1 V2_IN
1 V3_IN
C304
C305
C323
C306
C324
C307
C308
C309
R304
R305
R306
R307
R308
R309
56
Y301
24.576
C310
27PF
C311
27PF
R314
R315
R316
R317
R318
R319
R320
R321
VDEC_D7
VDEC_D6
VDEC_D5
VDEC_D4
VDEC_D3
VDEC_D2
VDEC_D1
VDEC_D0
R303
*33
GPIO3 1,6
DIG1_3V3
U302
*NC7SZ125
C312
*104
R324
*33
PCM_XCLK
R301
R302
BCK_7114 2
LRCK_7114 2
CLK_7114 2
L303
FB

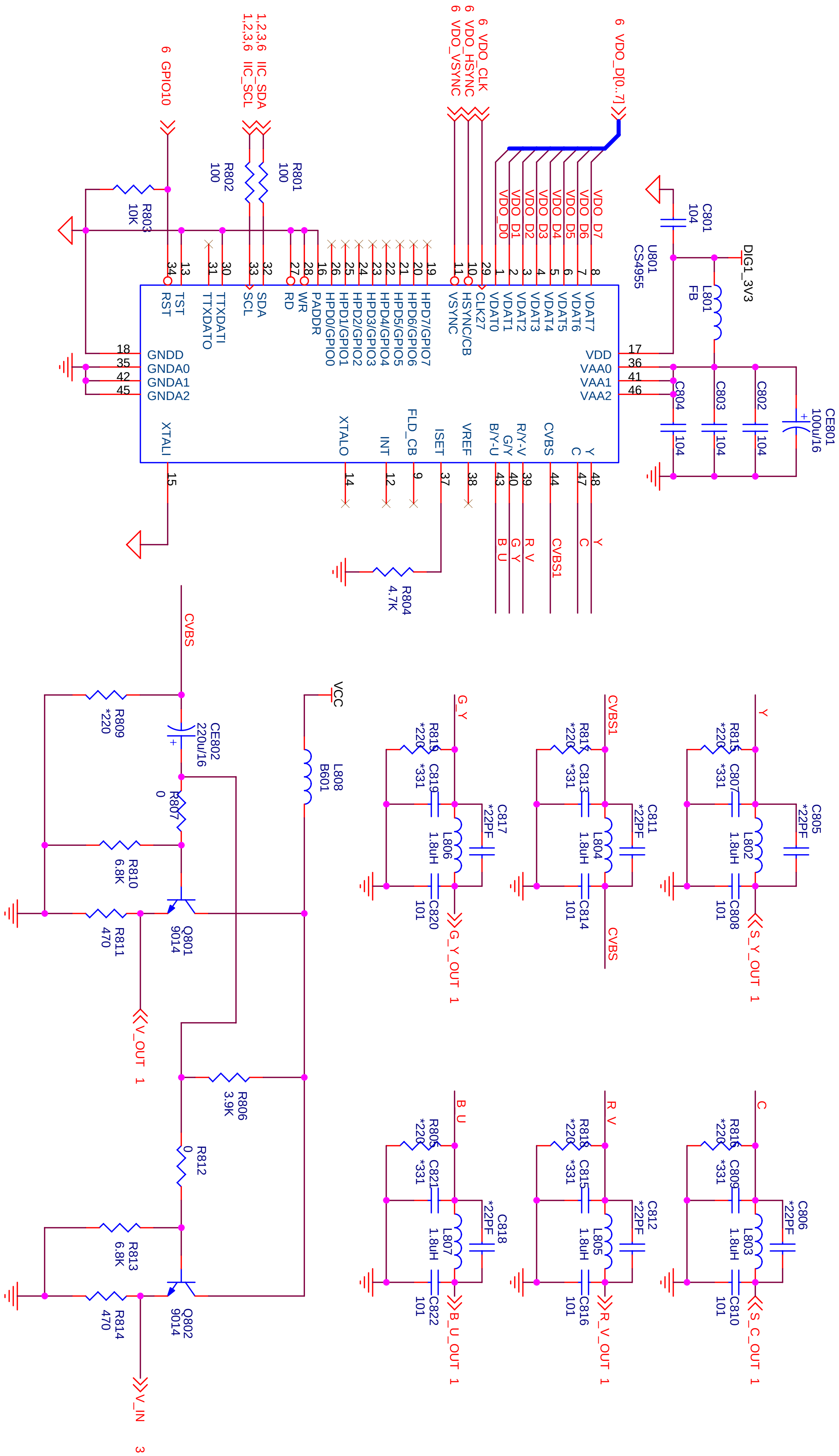

CS92288
U401
DIG1_1V8
DIG1_3V3
SM3.3V
APLL_VDDA
APLL_VDD
PLL_VDD
PLL_VDDA
APLL_VSSA
PLL_VSSA
APLL_VSS
PLL_VSS
MA[11..0]
MD[63..0]
MEMCLK1
MEMCLK0
U402
U403
U404
U405
KM416S1020
TSOP-50
U406
LT1117-1.8
5 HD[7..0]
5,6 HMS_D[15..0]
3,6 VDEC_D[7..0]
3,6 VDEC_VCLK
3,6 VDEC_HSYNC_
3,6 VDEC_VSYNC_
3,6 VDEC_DVALID
5,6 SYSCLK_27MHZ
6 GPIO15
6 GPIO14
1,6 GPIO12
5 HALE_
5 HDMA_REQ
5 HRD_
5 HWR_
HIRQ
HSYSRDY
FLASH_SEL
ROM_SEL
RWNSBHE
INTX16
INTLMOT
HREF_MOD
VSYNC_MOD
DREADY_MOD
ENC_DEC_
TCK
TDI
TMS
ADC_LRCK 2,6
ADC_BCK 2,6
ADC_D 2,6
CS92288
74

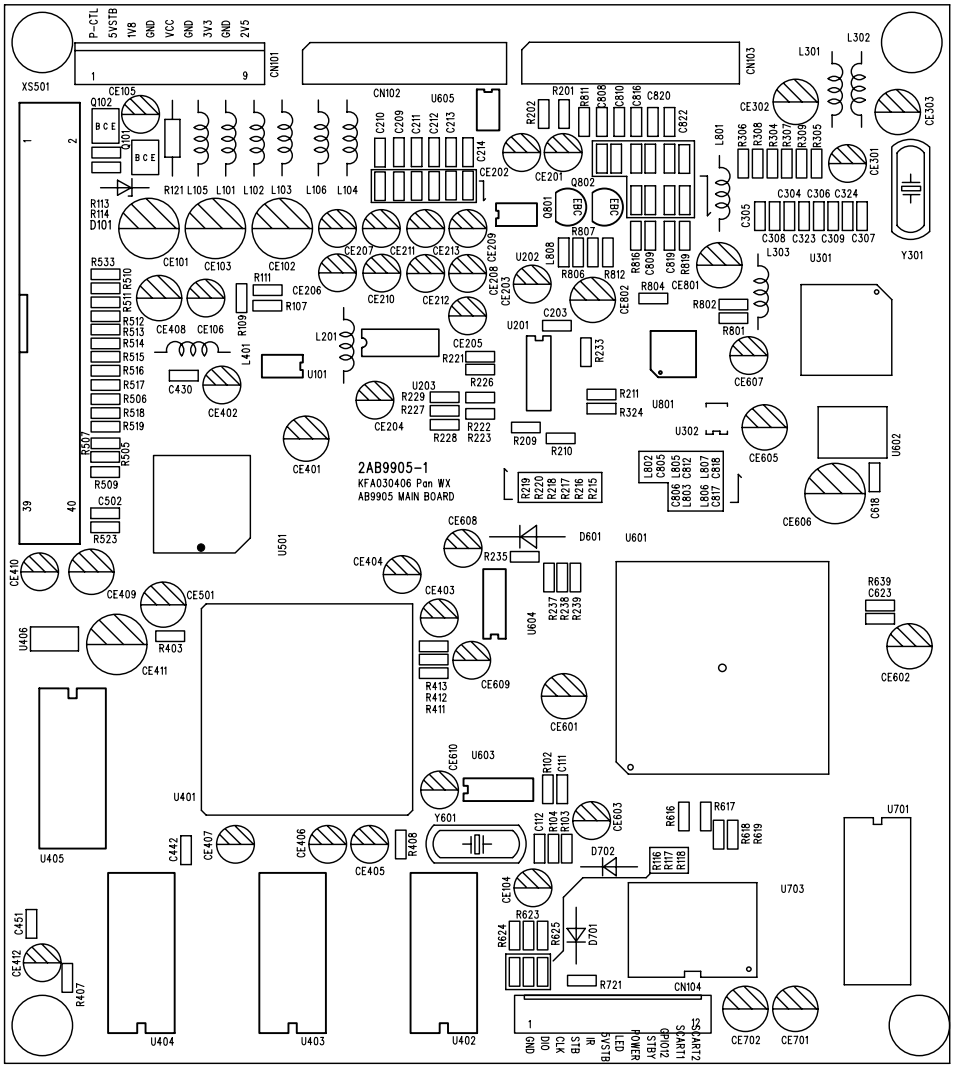

HDD AND DVD_LOADER INTERFACE
CONNECTOR
6,7 RESET_L
4 HD[7..0]
HD7
HD6
HD5
HD4
HD3
HD2
HD1
HD0
R533
10K
IDE_WR
IDE_RD
R510 22
R511 22
R512 22
R513 22
R514 22
R515 22
R516 22
R517 22
IDE_DRQ
R518 22
R519 22
IDE0_DACK
IDE_IRQ
6 HMS_A1
6 HMS_A0
6 HMS_CS0
XS501
R521
10K
VCC
R525 22
R526 22
R527 22
R528 22
R529 22
R530 22
R531 22
R532 22
HMS_D8
HMS_D9
HMS_D10
HMS_D11
HMS_D12
HMS_D13
HMS_D14
HMS_D15
CSEL_H
PDIAG_L
IDE0_CS1
R523 22
R522 10K
VCC
HMS_A2 6
R524
5.6K
HMS_D[15..0] 4,6
U501
ASIC
HMS_D0
HMS_D1
HMS_D2
HMS_D3
HMS_D4
HMS_D5
HMS_D6
HMS_D7
hostD0
hostD1
hostD2
hostD3
hostD4
hostD5
hostD6
hostD7
6 HMS_RD_L
6 HMS_WR_L
HMS_A0
HMS_A1
HMS_A2
host/RD
host/WR
hostA0
hostA1
hostA2
6 HMS_A[2..0]
6 HMS_CS0
6 HMS_CS1
host/CS0
host/CS1
4,6 SYSCLK_27MHZ
CLK
VCC
R501 *0
DIG1_3V3
R502 0
VCCINT
VCC
VCCINT
VCC
ideD0
ideD1
ideD2
ideD3
ideD4
ideD5
ideD6
ideD7
ideIRQ
ideDRQ
ide/DACK
ide/WR
ide/RD
ide/CS1
ide0/DACK
ide1/CS1
cdcDRQ
cdc/ALE
cdc/RD
cdc/WR
GND
GND
GND
GND
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
IDE_WR
IDE_RD
IDE0_CS1
IDE_IRQ
IDE_DRQ
IDE0_DACK
R505 22
R506 22
R507 22
R508 5.6K
R509 10K
HDMA_REQ 4
HALE_ 4
HRD_ 4
HWR_ 4
CE501
100u/16
C501
104
C502
104
C503
104

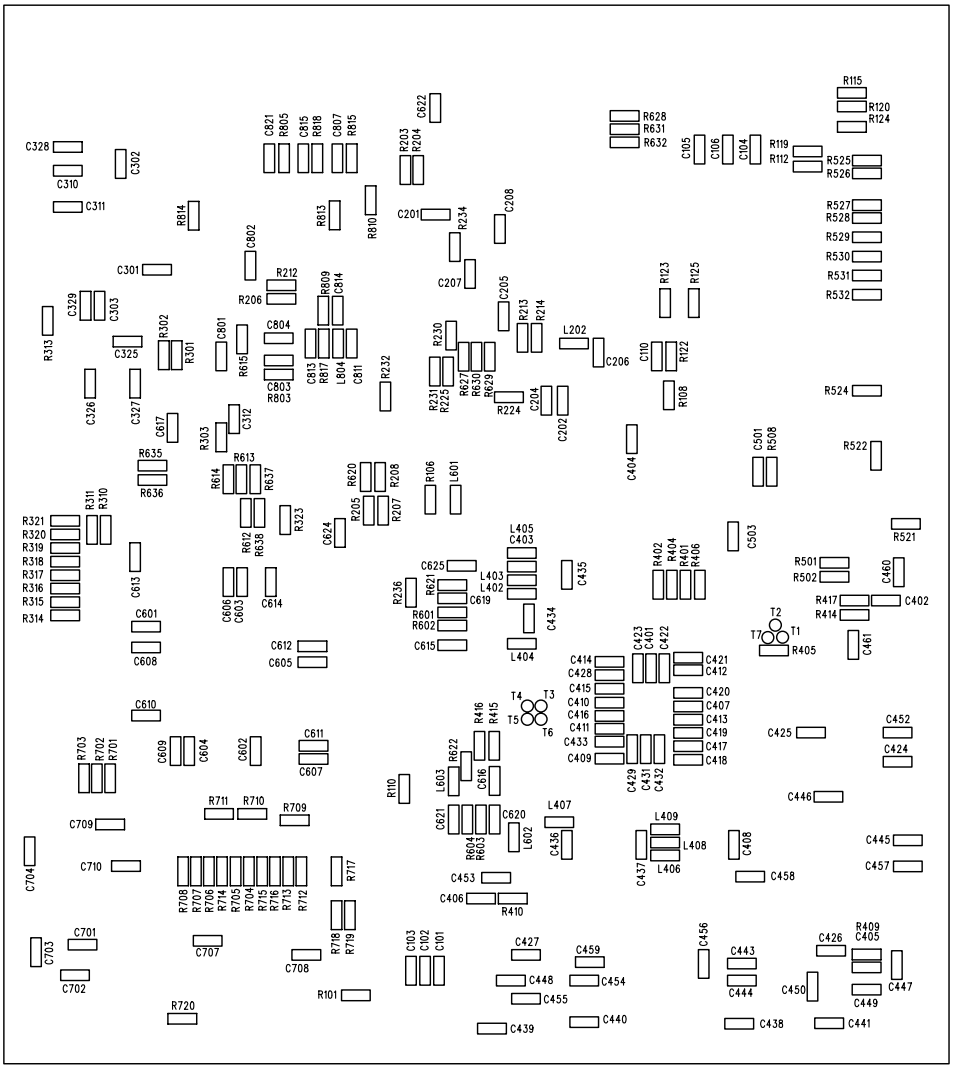

CS98000
U601
DIG1_3V3
DIG1_2V5
CE601 220u/16
CE602 220u/16
CE603 47u/16
C602 104
C603 104
C604 104
C605 104
C606 104
C607 104
C608 104
C609 104
C610 104
C611 104
C612 104
C613 104
C614 104
C624 104
C601 104
VCC
C622 104
U605 24C08
IIC_SCL
IIC_SDA
3,4 VDEC_D[7..0]
VDEC_D0
VDEC_D1
VDEC_D2
VDEC_D3
VDEC_D4
VDEC_D5
VDEC_D6
VDEC_D7
3,4 VDEC_HSYNC_
3,4 VDEC_VSYNC_
3,4 VDEC_DVALID
3,4 VDEC_VCLK
U604B 74HCT14
U604A 74HCT14
1 OPTICAL
1 SPDIF_OUT
U604F 74HCT14
U604E 74HCT14
L601 0
R601 330
C619 104
R602 91
CE609 47u/16
C623 104
2,4 ADC_D1
2,4 ADC_LRCK1
2,4 ADC_BCK1
2 PCMD2_O
2 PCMD1_O
2 PCMD0_O
2 LRCK_OUT
2 BCK_OUT
8 VDO_D[0..7]
R637 22
R638 22
R612 22
R613 22
R614 22
VDO_D0
VDO_D1
VDO_D2
VDO_D3
VDO_D4
VDO_D5
VDO_D6
VDO_D7
8 VDO_VSYNC
8 VDO_HSYNC
8 VDO_CLK
R615 22
R639 22
HMS_RDY
5 HMS_RD_L
5 HMS_WR_L
HMS_RDY
5 HMS_CS0
5 HMS_CS1
5 HMS_A[2..0]
HMS_A2
HMS_A1
HMS_A0
4,5 HMS_D[15..0]
HMS_D15
HMS_D14
HMS_D13
HMS_D12
HMS_D11
HMS_D10
HMS_D9
HMS_D8
HMS_D7
HMS_D6
HMS_D5
HMS_D4
HMS_D3
HMS_D2
HMS_D1
HMS_D0
AUX_D0
AUX_D1
AUX_D2
AUX_D3
AUX_D4
AUX_D5
AUX_D6
AUX_D7
AUX_RDY
AUX_ERR
AUX_SOS
AUX_ENA
AUX_STB
CDC_CK
CDC_RST
CDC_SY
CDC_DO
CDC_DI
AIN_DATA
AIN_LRCK
AIN_BCK
AUD_DO_3
AUD_DO_2
AUD_DO_1
AUD_DO_0
AUD_LRCK
AUD_BCK
VDAT0
VDAT1
VDAT2
VDAT3
VDAT4
VDAT5
VDAT6
VDAT7
VSYNC
HSYNC
CLK27_O
H_CKO
H_DREQ
H_DACK
H_ALE
H_BH16
H-RD
H-WR
H-RDY
H_CS_0
H_CS_1
H_CS_2
H_CS_3
HA4
HA3
HA2
HA1
HA0
HD15
HD14
HD13
HD12
HD11
HD10
HD9
HD8
HD7
HD6
HD5
HD4
HD3
HD2
HD1
HD0
MDATA[0..31] 7
MADDR[0..11] 7
M_DQM[0..3] 7
M_CKO 7
M_BS_L 7
M_CKE 7
M_AP 7
M_RAS_L 7
M_CAS_L 7
M_WE_L 7
M_DQM0
M_DQM1
M_DQM2
M_DQM3
NVR_WE_L 7
NVR_OE_L 7
RESET_L 5,7
IR_IN 1
SYSCLK_27MHZ 4,5
R616 22
R617 22
R618 22
R619 22
U602 PQ070XZ
VIN
VOUT
VC
GND
ADJ
R636 1K
R635 1K
CE606 330u/16
C618 104
CE605 220u/16
CE607 47u/16
C617 104
U604D 74HCT14
D601 1N4148
R621 33K
CE608 10u/16
C615 104
L602 B601
R603 3K
U603A 74HC04
U603B 74HC04
Y601 27MHZ
C620 20PF
C621 20PF
CE610 47u/16
L603 B601
C616 102
C625 102
R622 100
R604 330
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
VFD_CLK 1
VFD_DIO 1
VFD_STB 1
GPIO3 1,3
GPIO4 1
IIC_SCL 1,2,3,8
IIC_SDA 1,2,3,8
GPIO7 1
GPIO8 1
R620 22
PCM_XCLK 2
(PCM_XCLK=16.9M)
R623 1K
R624 1K
R625 1K
R627 10K
R628 10K
R629 2.2K
R630 2.2K
R631 10K
R632 10K

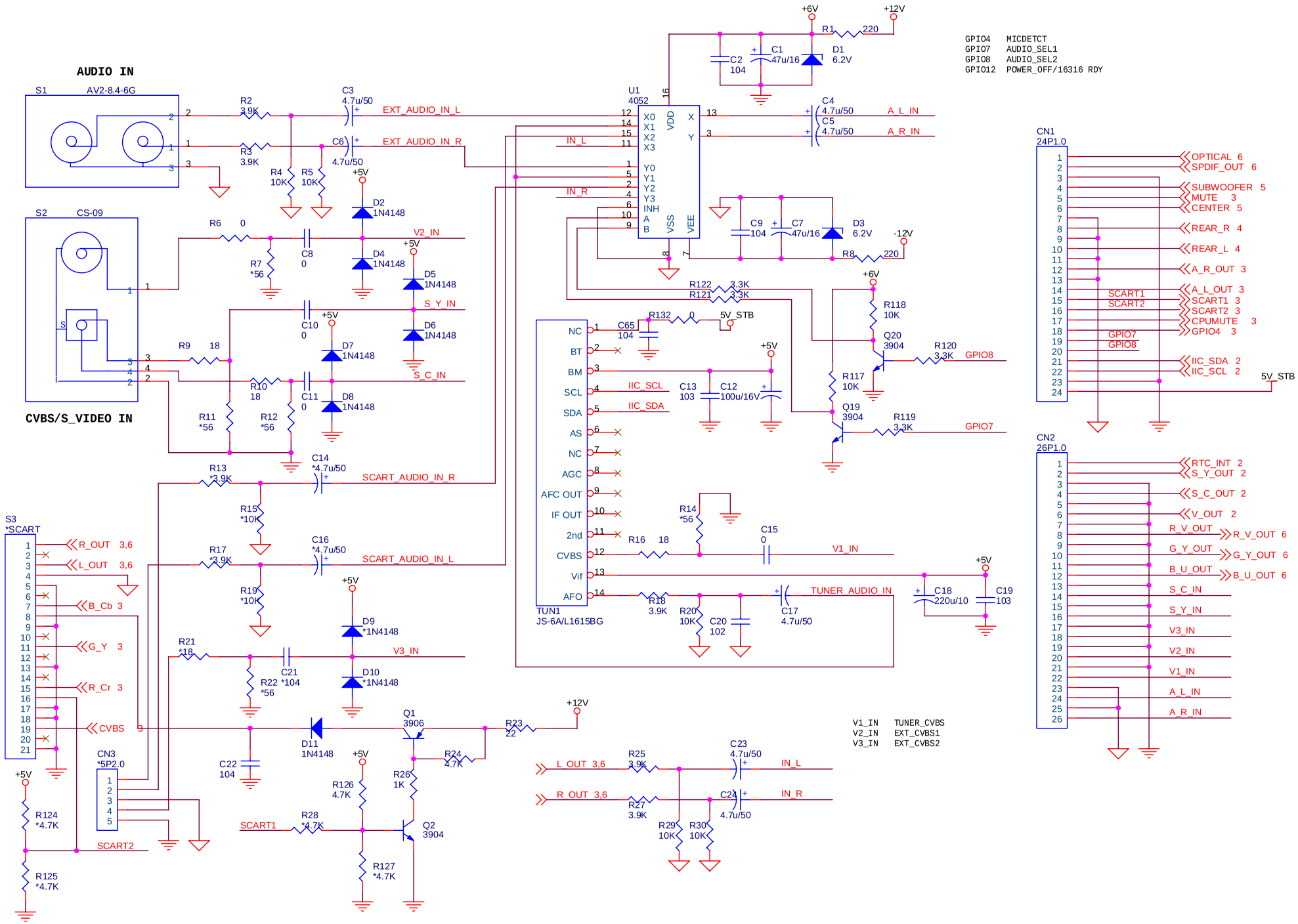


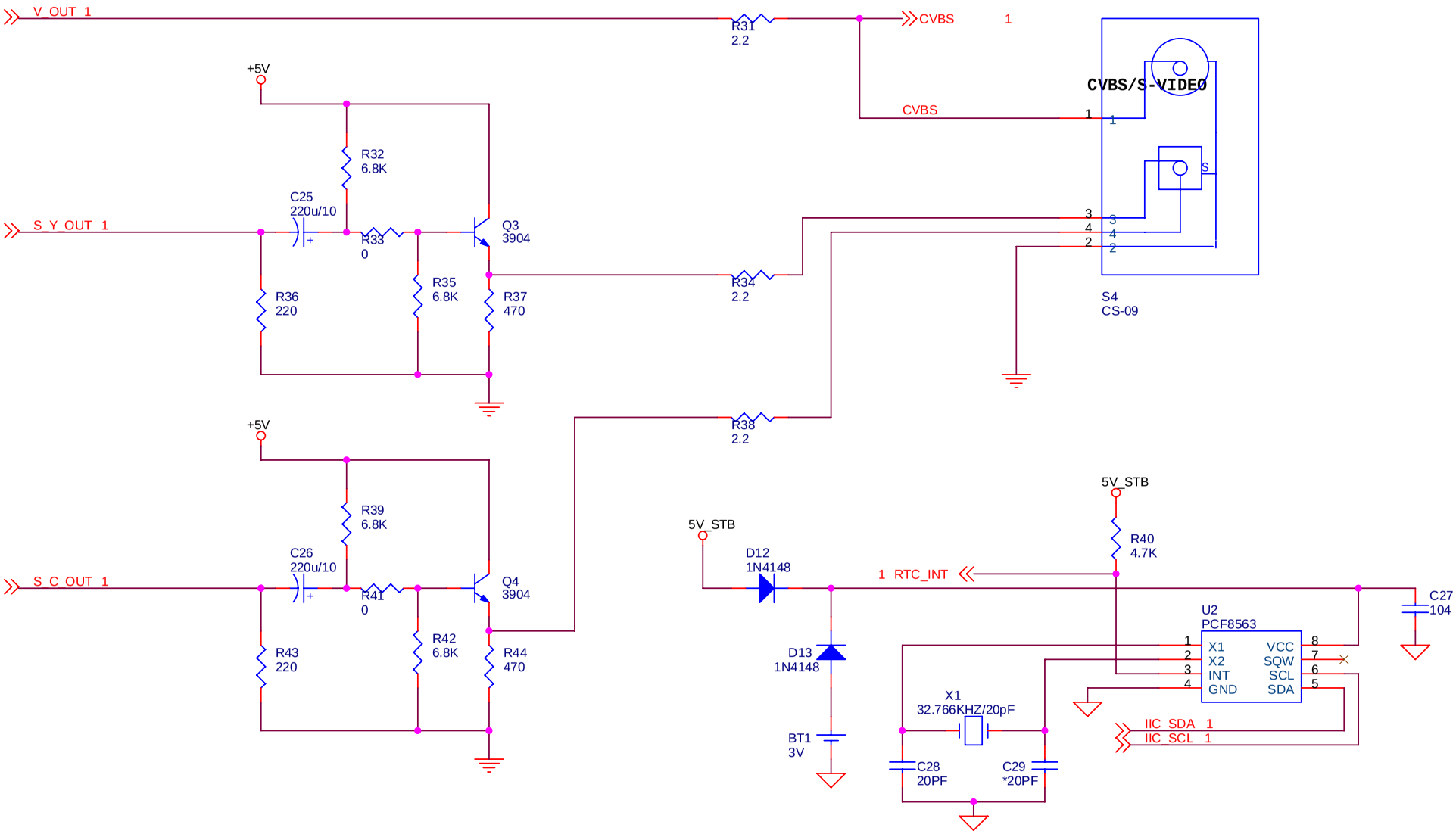
Note:Resistors should be 300ohm when FLASH TYPE is +5V and 33ohm when FLASH TYPE is +3.3V.

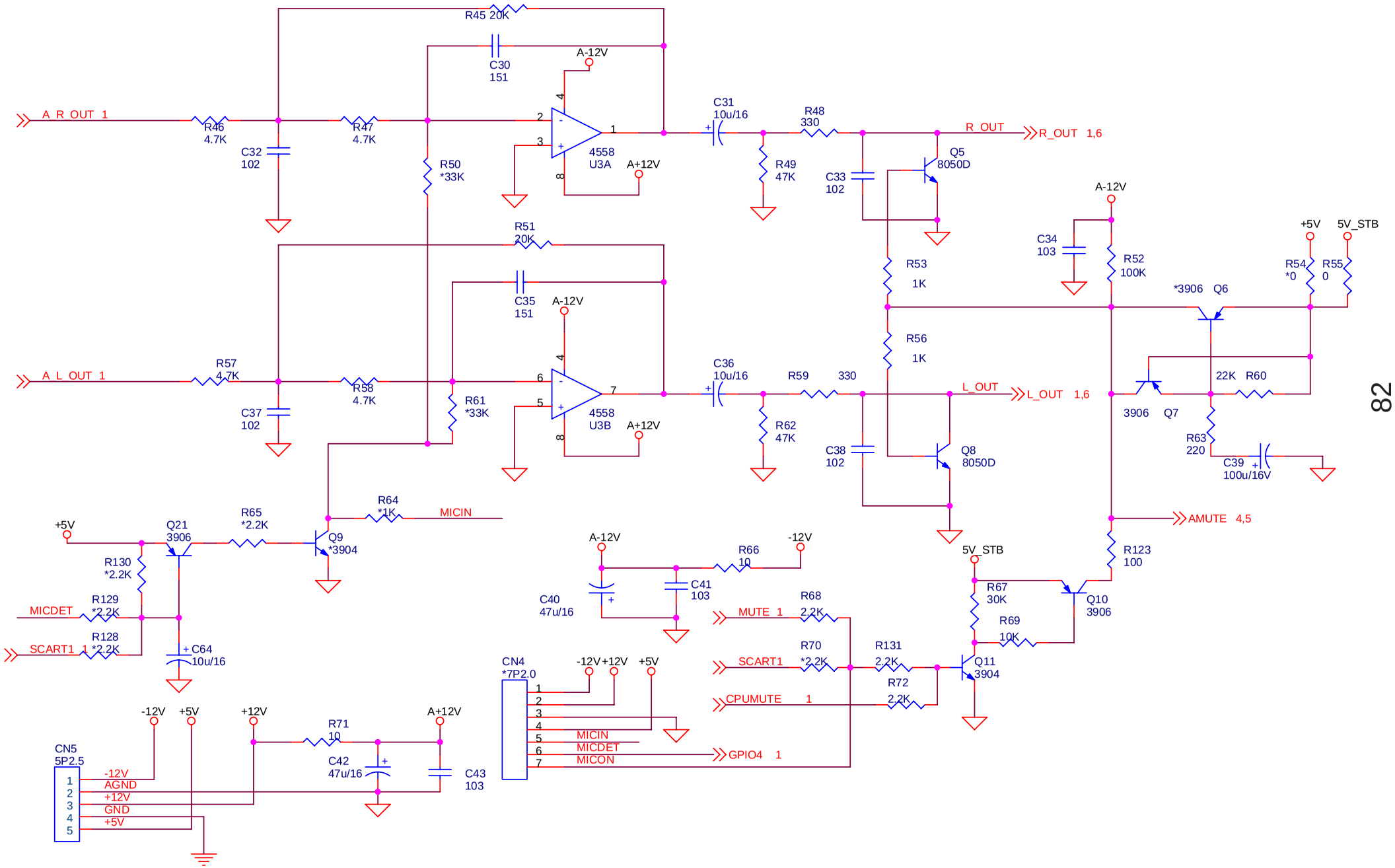

U801
CS4955
DIG1_3V3
L801
FB
C801
104
CE801
100u/16
C802
104
C803
104
C804
104
VDD
VAA0
VAA1
VAA2
GNDD
GNDA0
GNDA1
GNDA2
VDAT7
VDAT6
VDAT5
VDAT4
VDAT3
VDAT2
VDAT1
VDAT0
CLK27
HSYNC/CB
VSYNC
HPD7/GPIO7
HPD6/GPIO6
HPD5/GPIO5
HPD4/GPIO4
HPD3/GPIO3
HPD2/GPIO2
HPD1/GPIO1
HPD0/GPIO0
PADDR
WR
RD
SDA
SCL
TTXDATI
TTXDATO
TST
RST
XTALI
XTALO
INT
FLD_CB
ISET
VREF
B/Y-U
G/Y
R/Y-V
CVBS
C
Y
6 VDO_D[0..7]
VDO_D7
VDO_D6
VDO_D5
VDO_D4
VDO_D3
VDO_D2
VDO_D1
VDO_D0
6 VDO_CLK
6 VDO_HSYNC
6 VDO_VSYNC
1,2,3,6 IIC_SDA
1,2,3,6 IIC_SCL
6 GPIO10
R801
100
R802
100
R803
10K
R804
4.7K
Y
C
CVBS1
R V
G Y
B U
CVBS
CE802
220u/16
R809
*220
R807
0
R810
6.8K
Q801
9014
R811
470
V_OUT 1
VCC
L808
B601
R806
3.9K
R812
0
R813
6.8K
Q802
9014
R814
470
V_IN 3
R815
*220
C807
*331
L802
1.8uH
C805
*22PF
C808
101
S_Y_OUT 1
R817
*220
C813
*331
L804
1.8uH
C811
*22PF
C814
101
R819
*220
C819
*331
L806
1.8uH
C817
*22PF
C820
101
G_Y_OUT 1
R816
*220
C809
*331
L803
1.8uH
C806
*22PF
C810
101
S_C_OUT 1
R818
*220
C815
*331
L805
1.8uH
C812
*22PF
C816
101
R_V_OUT 1
R805
*220
C821
*331
L807
1.8uH
C818
*22PF
C822
101
B_U_OUT 1

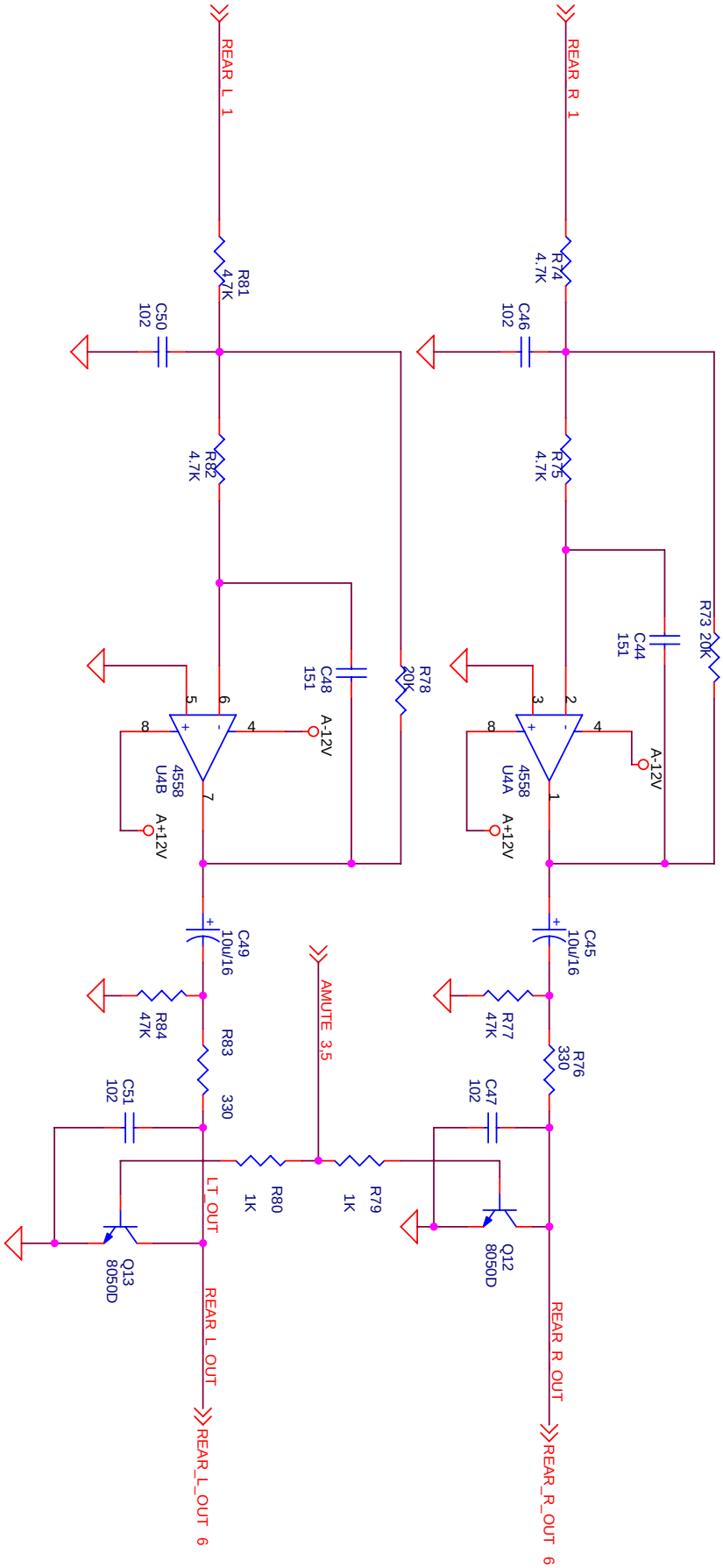

2AB9905-1
KFA030406 Pan WX
AB9905 MAIN BOARD

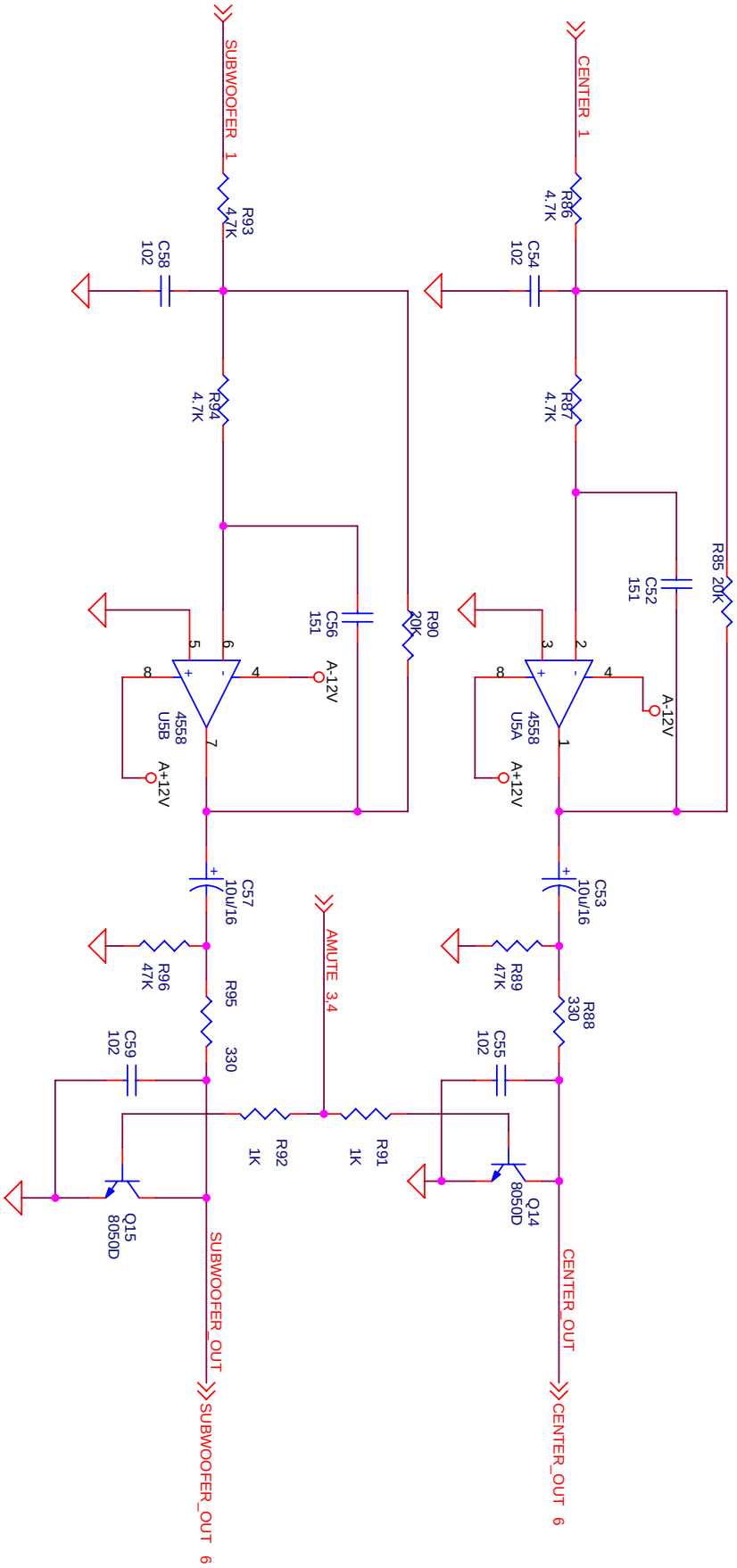


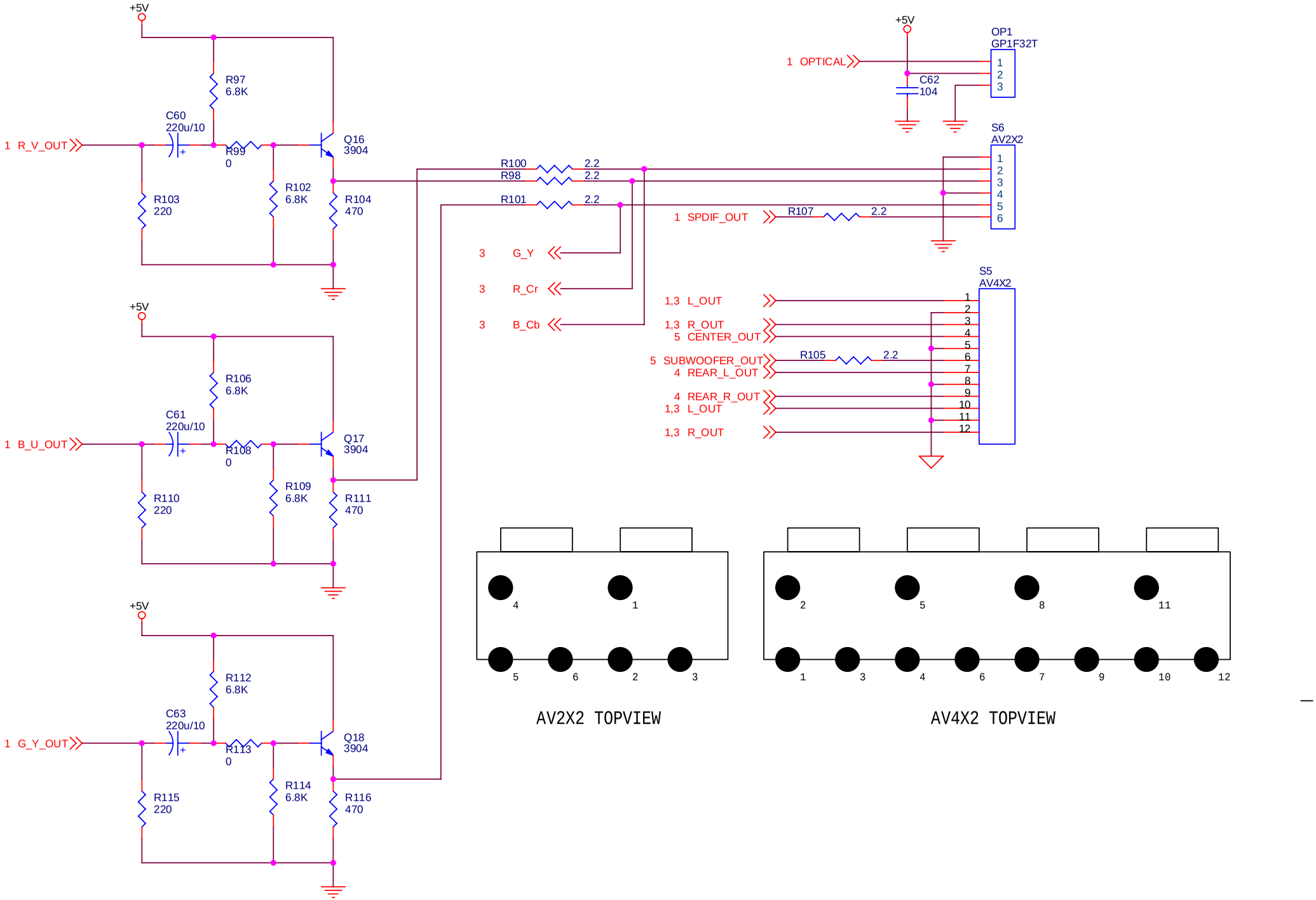

AUDIO IN
S1 AV2-8.4-6G
S2 CS-09
CVBS/S_VIDEO IN
S3 *SCART
U1 4052
TUN1 JS-6A/L1615BG
CN1 24P1.0
CN2 26P1.0
CN3 *5P2.0
GPIO4 MICDETCT
GPIO7 AUDIO_SEL1
GPIO8 AUDIO_SEL2
GPIO12 POWER_OFF/16316 RDY
V1_IN TUNER_CVBS
V2_IN EXT_CVBS1
V3_IN EXT_CVBS2
EXT_AUDIO_IN_L
EXT_AUDIO_IN_R
SCART_AUDIO_IN_R
SCART_AUDIO_IN_L
TUNER_AUDIO_IN
V2_IN
S_Y_IN
S_C_IN
V3_IN
V1_IN
IN_L
IN_R
A_L_IN
A_R_IN
IIC_SCL
IIC_SDA
5V_STB
SCART1
SCART2
GPIO7
GPIO8
OPTICAL 6
SPDIF_OUT 6
SUBWOOFER 5
MUTE 3
CENTER 5
REAR_R 4
REAR_L 4
A_R_OUT 3
A_L_OUT 3
SCART1 3
SCART2 3
CPUMUTE 3
GPIO4 3
IIC_SDA 2
IIC_SCL 2
RTC_INT 2
S_Y_OUT 2
S_C_OUT 2
V_OUT 2
R_V_OUT
G_Y_OUT
B_U_OUT
R_V_OUT 6
G_Y_OUT 6
B_U_OUT 6
S_C_IN
S_Y_IN
V3_IN
V2_IN
V1_IN
A_L_IN
A_R_IN
R_OUT 3,6
L_OUT 3,6
B_Cb 3
G_Y 3
R_Cr 3
CVBS 3
+6V
+12V
-12V
+5V

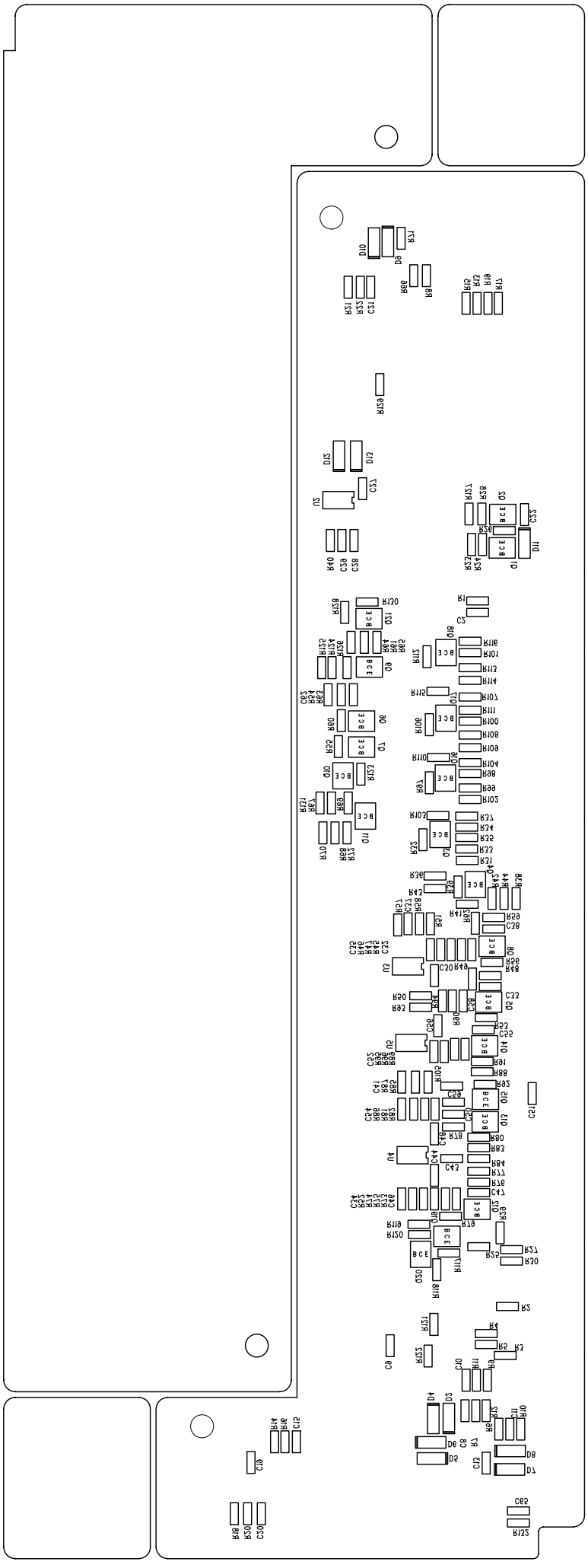

V_OUT 1
R31
2.2
CVBS 1
CVBS
CVBS/S-VIDEO
S
S4
CS-09
+5V
R32
6.8K
C25
220u/10
S_Y_OUT 1
R33
0
Q3
3904
R35
6.8K
R36
220
R37
470
R34
2.2
+5V
R39
6.8K
C26
220u/10
S_C_OUT 1
R41
0
Q4
3904
R42
6.8K
R43
220
R44
470
R38
2.2
5V_STB
D12
1N4148
1 RTC_INT
R40
4.7K
C27
104
U2
PCF8563
X1
X2
INT
GND
VCC
SQW
SCL
SDA
D13
1N4148
BT1
3V
X1
32.766KHZ/20pF
C28
20PF
C29
*20PF
IIC_SDA 1
IIC_SCL 1

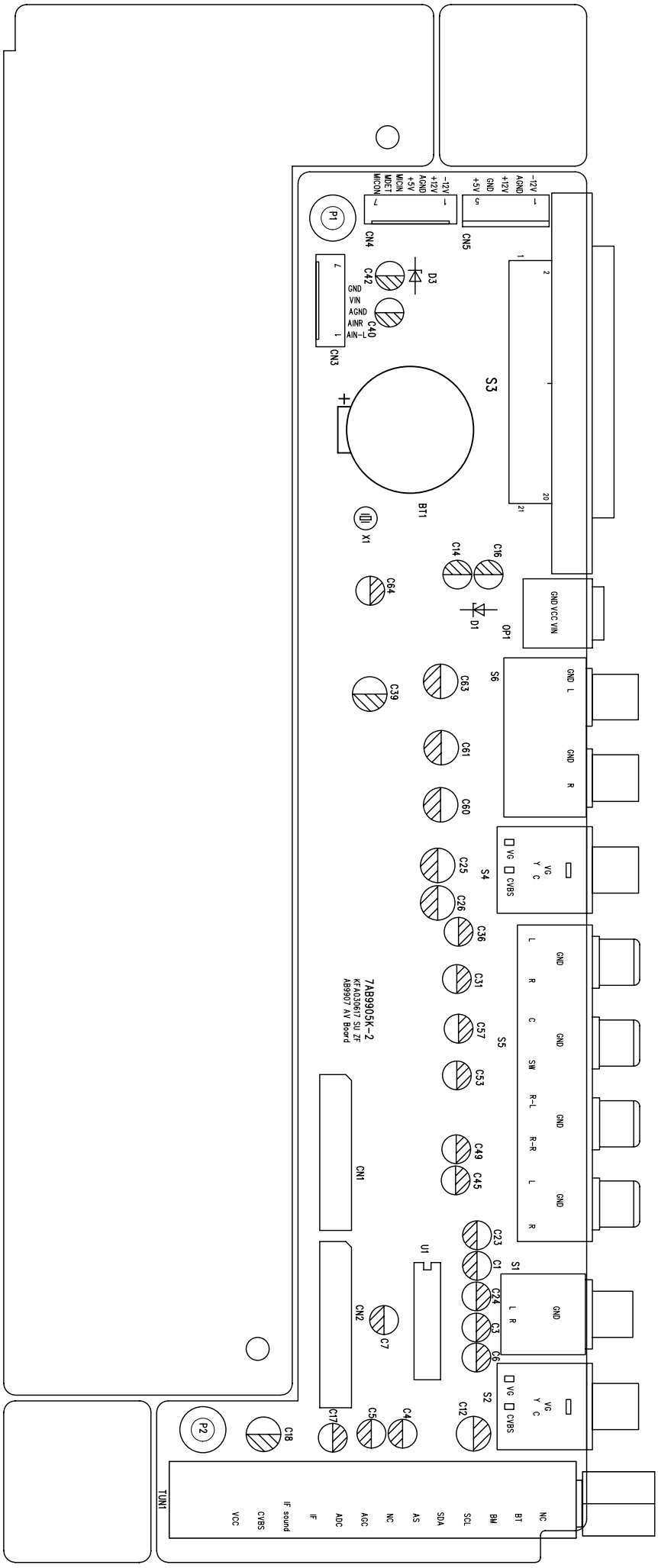

A_R_OUT 1
R46 4.7K
R47 4.7K
R45 20K
C30 151
C32 102
R50 *33K
A-12V
4558 U3A
A+12V
C31 10u/16
R48 330
R49 47K
C33 102
R_OUT
R_OUT 1,6
Q5 8050D
A_L_OUT 1
R57 4.7K
R58 4.7K
R51 20K
C35 151
C37 102
R61 *33K
4558 U3B
C36 10u/16
R59 330
R62 47K
C38 102
L_OUT
L_OUT 1,6
Q8 8050D
R53 1K
R56 1K
C34 103
R52 100K
A-12V
+5V
5V_STB
R54 *0
R55 0
*3906 Q6
3906 Q7
22K R60
R63 220
C39 100u/16V
AMUTE 4,5
R123 100
Q10 3906
5V_STB
R67 30K
R69 10K
R64 *1K
MICIN
R65 *2.2K
Q9 *3904
Q21 3906
+5V
R130 *2.2K
R129 *2.2K
R128 *2.2K
MICDET
SCART1 1
C64 10u/16
A-12V
R66 10
-12V
C40 47u/16
C41 103
MUTE 1
R68 2.2K
SCART1
R70 *2.2K
R131 2.2K
R72 2.2K
CPUMUTE 1
Q11 3904
CN4 *7P2.0
-12V +12V +5V
MICIN
MICDET
MICON
GPIO4 1
CN5 5P2.5
-12V
AGND
+12V
GND
+5V
R71 10
C42 47u/16
C43 103
A+12V

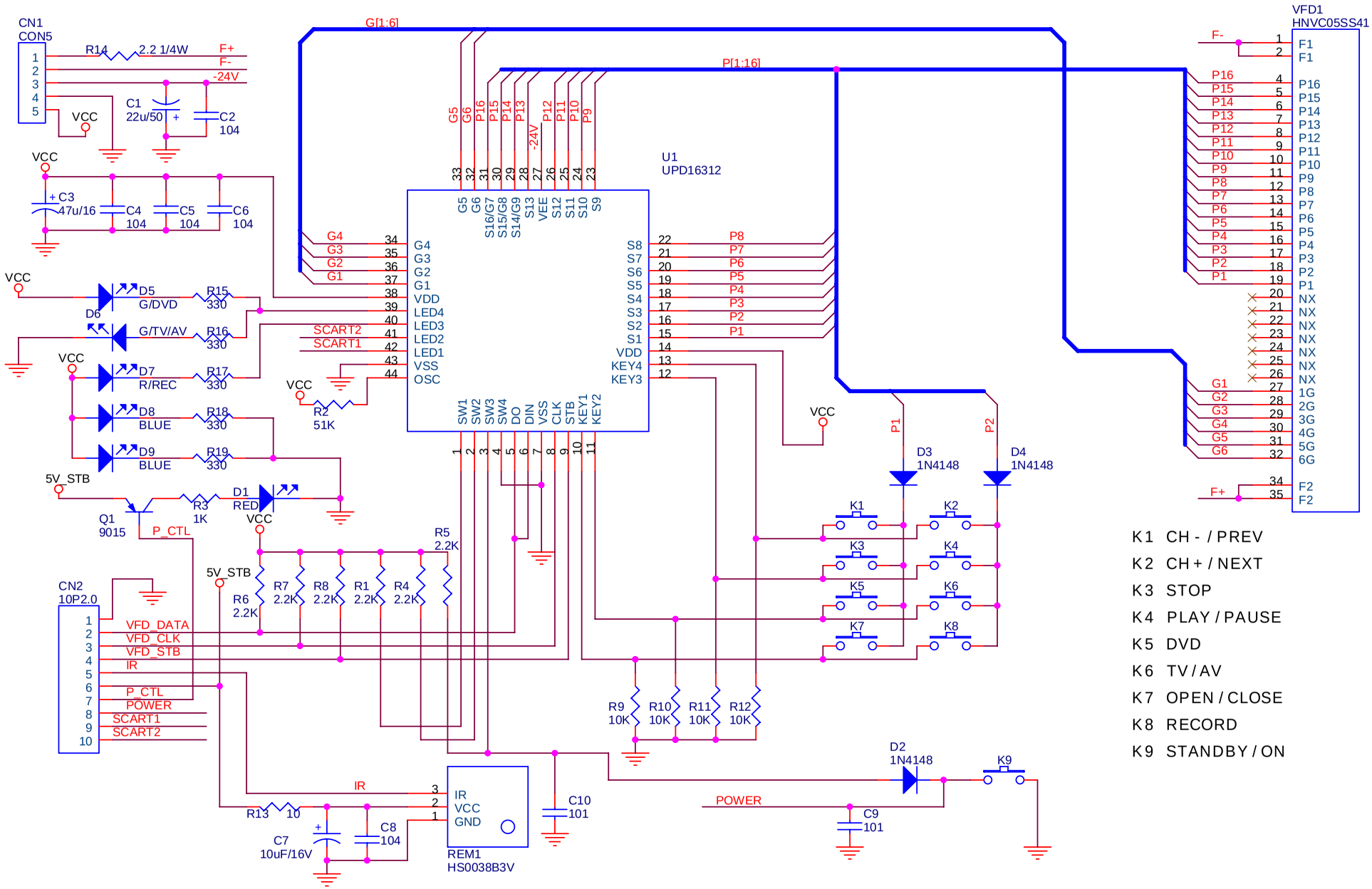

REAR_R_1
R74
4.7K
C46
102
R75
4.7K
C44
151
R73 20K
A-12V
4558
U4A
A+12V
C45
10u/16
R77
47K
R76
330
C47
102
Q12
8050D
REAR_R_OUT
REAR_R_OUT 6
REAR_L_1
R81
4.7K
C50
102
R82
4.7K
C48
151
R78
20K
A-12V
4558
U4B
A+12V
C49
10u/16
R84
47K
R83
330
C51
102
AMUTE 3,5
R80
1K
R79
1K
LT_OUT
Q13
8050D
REAR_L_OUT
REAR_L_OUT 6


CENTER_1
SUBWOOFER_1
R86
4.7K
R87
4.7K
R93
4.7K
R94
4.7K
C54
102
C58
102
R85 20K
C52
151
R90
20K
C56
151
A-12V
4558
U5A
U5B
A+12V
C53
10u/16
C57
10u/16
R89
47K
R96
47K
R88
330
R95
330
C55
102
C59
102
AMUTE_3,4
R91
1K
R92
1K
Q14
8050D
Q15
8050D
CENTER_OUT
SUBWOOFER_OUT
CENTER_OUT_6
SUBWOOFER_OUT_6

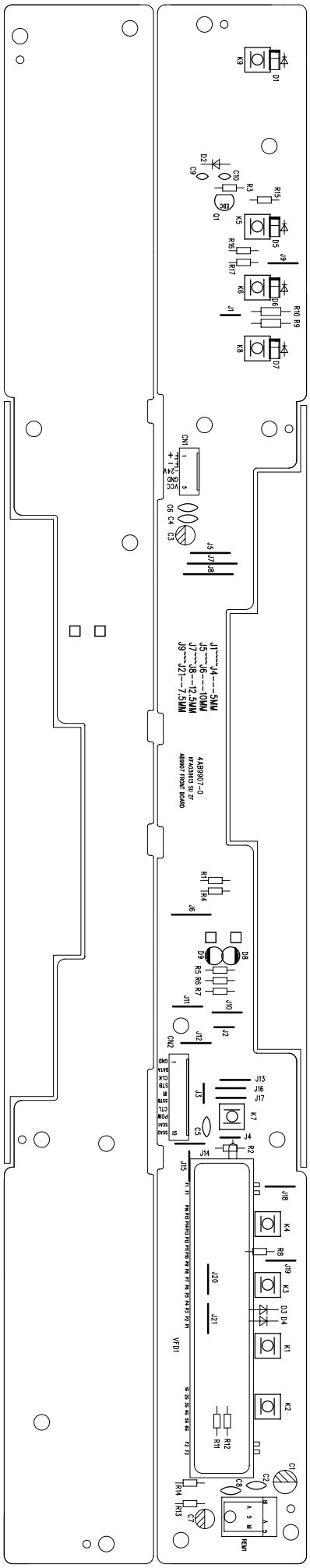

+5V
R97
6.8K
C60
220u/10
1 R_V_OUT
R99
0
Q16
3904
R103
220
R102
6.8K
R104
470
R100
R98
R101
2.2
3 G_Y
3 R_Cr
3 B_Cb
1 SPDIF_OUT
R107
S6
AV2X2
1 OPTICAL
C62
104
OP1
GP1F32T
S5
AV4X2
1,3 L_OUT
1,3 R_OUT
5 CENTER_OUT
5 SUBWOOFER_OUT
4 REAR_L_OUT
4 REAR_R_OUT
1,3 L_OUT
1,3 R_OUT
R105
R106
6.8K
C61
220u/10
1 B_U_OUT
R108
0
Q17
3904
R110
220
R109
6.8K
R111
470
R112
6.8K
C63
220u/10
1 G_Y_OUT
R113
0
Q18
3904
R115
220
R114
6.8K
R116
470
AV2X2 TOPVIEW
AV4X2 TOPVIEW




7AB9905K-2
KFAD3617 SU ZF
AB9907 AV Board
CN1
CN2
CN3
CN4
CN5
P1
P2
S1
S2
S3
S4
S5
S6
BT1
X1
OP1
U1
TUN1
C1
C3
C4
C5
C6
C7
C12
C14
C16
C17
C18
C23
C24
C25
C26
C31
C36
C39
C40
C42
C45
C49
C53
C57
C60
C61
C63
C64
D1
D3
GND VCC VIN
GND L
GND R
VG Y C
CVBS
GND L R C SW R-L R-R L GND R
GND L R
GND VIN AGND AINR AIN-L
-12V AGND +12V GND +5V
MICIN MDET MICON +5V AGND +12V -12V
NC BT BM SCL SDA AS NC AGC ADC IF IF sound CVBS VCC



K1 CH - / PREV
K2 CH + / NEXT
K3 STOP
K4 PLAY / PAUSE
K5 DVD
K6 TV / AV
K7 OPEN / CLOSE
K8 RECORD
K9 STANDBY / ON


J1~~~J4----5MM
J5~~~J6----10MM
J7~~~J8--12.5MM
J9~~~J21--7.5MM
4AB3907-0
KF4A03903 SU_3F
AB3907 FRONT BOARD
VFD1
REM1

PARTS LIST main board

ITEM	DESCRIPTION		QTY	LOCATION
1	Carbon film Resistor	1/4W2.2Ω ±5%	1	R121
2	RESISTOR	1/16W 0Ω ±5%	25	R104, R106, R109, R110, R120, R205~R207, R211, R212, R230~R233, R235, 236, R313, R415, R417, R502, L601, R720, R807, R812, R604
3	RESISTOR	1/16W 22Ω ±5%	46	R310, R311, R314~R321, R407, R408, R505, R506, R507, R510~R519, R523, R525~R532, R612~R620, R637, R638, R639
4	RESISTOR	1/16W 33Ω ±5%	23	R225~R229, R301, R302, R701~R716
5	RESISTOR	1/16W 56Ω ±5%	6	R304~R309
6	RESISTOR	1/16W 220Ω ±5%	1	R809
7	RESISTOR	1/16W 330Ω ±5%	1	R601
8	RESISTOR	1/16W 470Ω ±5%	2	R811, R814
9	RESISTOR	1/16W 1K ±5%	8	R115, R125, R406, R623, R624, R625, R635, R636
10	RESISTOR	1/16W 2.2K ±5%	2	R629, R630
11	RESISTOR	1/16W 4.7K ±5%	11	R107, R111, R119, R122, R123, R323, R401, R411, R412, R413, R804
12	RESISTOR	1/16W 6.8K ±5%	2	R810, R813
13	RESISTOR	1/16W 10K ±5%	15	R101, R402~R405, R509, R521, R522, R533, R627, R631, R632, R718, R719, R803
14	RESISTOR	1/16W 15K ±5%	1	R124
15	RESISTOR	1/16W 22K ±5%	3	R201, R202, R213
16	RESISTOR	1/16W 33K ±5%	1	R621
17	RESISTOR	1/16W 100Ω ±5%	6	R116, R117, R118, R622, R801, R802
18	RESISTOR	1/16W 100K ±5%	1	R603
19	RESISTOR	1/16W 3.9K ±5%	1	R806
20	RESISTOR	1/16W 5.6K ±5%	8	R508, R524, R215~R220
21	RESISTOR	1/16W 150Ω ±5%	2	R203, R204
22	RESISTOR	1/16W 91Ω ±5%	1	R602
23	RESISTOR	1/16W62Ω±5%	2	R409, R410
24	ELEC.CAP	CD11 16V10U±20%5×11 2	15	CE105, CE106, CE201, CE202, CE206, CE207, CE210~CE213, CE403, CE404, CE405, CE406, CE608
25	ELEC.CAP	CD11 16V47U±20%5×11 2	10	CE301, CE402, CE407, CE410, CE412, CE603, CE607, CE609, CE610, CE702
26	ELEC.CAP	CD11 16V100U±20%6×12 2.5	4	CE303, CE501, CE701, CE801
27	ELEC.CAP	CD11 16V220U±20%6×12 2.5	8	CE302, CE401, CE408, CE409, CE601, CE602, CE605, CE802
28	ELEC.CAP	CD11 50V1U+20%-10%5×11 2	3	CE203, CE204, CE205

PARTS LIST main board

ITEM	DESCRIPTION		QTY	LOCATION
29	ELEC.CAP	CD11 50V4.7U±20%5×11 2	1	CE104
30	ELEC.CAP	CD11 50V3.3U±20%5×11 2	2	CE208,CE209
31	ELEC.CAP	CD11 16V330U±20%8×12 3.5	5	CE101,CE102,CE103,CE411, CE606
32	CER.CAP	50V 47P ±5% NPO 0603	2	C405,C406
33	CER.CAP	50V 101 ±5% NPO 0603	11	C101,C102,C103,C111,C112,C808,C810,C814,C816,C820,C822
34	CER.CAP	50V 122 ±10% 0603	6	C209~C214
35	CER.CAP	50V 102 ±10% 0603	2	C616,C625
36	CER.CAP	50V 27P ±5% NPO 0603	4	C310,C311,C620,C621
37	CER.CAP	50V 473 ±10% 0603	2	C308,C309
38	CER.CAP	50V104 ±20% 0603	121	C104,C105,C106,C110,C201~C208,C301~C307,C323~C329,C401~C404,C407~C461,C501,C502,C503,C601~C615,C617,C618,C619,C622,C623,C624,C701~C704,C707~C710,C801~C804
39	FERRITE BEAD	FCM1608-601T02	12	L202,L602,L603,L808,L402~L409
40	FERRITE BEAD	FB	10	L102,L103,L105,L106,L201,L301,L302,L303,L401,L801
41	INDUCTOR IRON	1.8UH ±10% 1608	6	L802~L807
42	DIODE	1N4148	3	D601,D701,D702
43	TRANSISTOR	9014C	2	Q801,Q802
44	IC	74HCU04D SOP	1	U603
45	IC	MM74HCU04M SOP	1	U603
46	IC	HCU04 SOP	1	U603
47	IC	LVU04 SOP	1	U603
48	IC	VHCU04 SOP	1	U603
49	IC	MM74HCT14M SOP	1	U604
50	IC	HCT14 SOP	1	U604
51	IC	CS4360 SSOP	1	U203
52	IC	CS4955-CQ TQFP	1	U801
53	IC	LM1117MP-1.8 SOT-223	1	U406
54	IC	W981616BH-7 SOP	4	U402~U405
55	IC	PQ070XZ01ZP SC-63	1	U602
56	IC	W986432DH-7 TSOP	1	U701
57	IC	SAA7114 QFP	1	U301
58	IC	CS92288 BGA	1	U401
59	IC	CS98000 QFP	1	U601

PARTS LIST main board

ITEM	DESCRIPTION		QTY	LOCATION
60	IC	CS5331A-KS SOP	1	U202
61	IC	24C08 SOP	1	U605
62	IC	HC157 SOP	1	U201
63	IC	MM74HC157M SOP	1	U201
64	CRYSTAL	27.00MHz 49-S	1	Y601
65	CRYSTAL	24.576MHz 49-S	1	Y301
66	CRYSTAL	24.576MHz 49-U	1	Y301
67	PCB	2AB9905-1	1	
68	WAFER	10P 2.0mm	1	CN104
69	WAFER	9P 2.5mm	1	CN101
70	WAFER	20P 2.5mm	1	XS501
71	WAFER	13P 1.0mm	1	CN103
72	WAFER	12P1.0mm	1	CN102

PARTS LIST key board

ITEM	DESCRIPTION		QTY	LOCATION
1	ELEC.CAP	CD11C 50V22U±20%6×7 2.5	1	C1
2	ELEC.CAP	CD11C 16V10U±20%4×7 1.5	1	C7
3	ELEC.CAP	CD11C 16V47U±20%5×7 2	1	C3
4	CER.CAP	50V 104 ±20% 5mm	5	C2,C4,C5,C6,C8
5	CER.CAP	50V 100P ±10% 5mm	2	C9,C10
6	LED	2R 53HD RED	2	D1,D7
7	DIODE	1N4148	3	D2~D4
8	LED	2G 53HD 2×5×7	2	D5,D6
9	LED	3B4ST	2	D8,D9
10	Tact Switch	6×6×1	9	K1~K9
11	Transistor	9015C	1	Q1
12	REMOTE RECEIVING	HS0038B3V	1	REM1
13	Carbon film Resistor	1/6W2.2K±5%	4	R5~R8
14	Carbon film Resistor	1/6W51K±5%	1	R2
15	Carbon film Resistor	1/6W10K±5%	2	R11,R12
16	Carbon film Resistor	1/6W10Ω±5%	1	R13
17	Carbon film Resistor	1/6W2.2Ω±5%	1	R14
18	Carbon film Resistor	1/6W330Ω±5%	2	R1,R4
19	Carbon film Resistor	1/6W1K±5%	2	R3,R17
20	Carbon film Resistor	1/6W220Ω±5%	2	R15,R16
21	Carbon film Resistor	1/4W10K±5%	2	R9,R10
22	IC	PT6312LQ QFP	1	U1
23	LED Displays	HNVC06SC020	1	VFD1
24	PCB	4AB9907-0	1	

PARTS LIST power board

ITEM	DESCRIPTION		QTY	LOCATION
1	RESISTOR	1/4W22Ω±5% 10	1	R13
2	RESISTOR	1/4W33Ω±5% 10	1	R5
3	RESISTOR	1/4W330Ω±5% 10	1	R8
4	RESISTOR	1/4W470Ω±5% 10	1	R15
5	RESISTOR	1/4W1K±5% 10	2	R4,R20
6	RESISTOR	1/4W4.7K±5% 10	1	R17
7	RESISTOR	1/4W10K±5% 10	4	R3,R7,R19,R10
8	RESISTOR	1/4W47K±5% 10	1	R9
9	RESISTOR	1/4W1.2K±5% 10	1	R14
10	RESISTOR	1W0.47Ω±5% 12.5	1	R12
11	METAL FILM RESISTOR	1/4W10K±1% 10	2	R11,R18
12	METAL OXIDE FILM RESISTOR	2W68K±5% 15	1	R2
13	METAL OXIDE FILM RESISTOR	1/2W470K±5% 12.5	2	R1,R6
14	CER.CAP	50V 104 +80%-20% 5mm	7	C2,C7,C8,C11,C12,C15,C16
15	CER.CAP	1000V 103 +80%-20% 7.5mm	1	C4
16	CER.CAP	500V 101 ±10% 5mm	1	C17
17	CAP	CT81 400V221±10% 10mm	2	C3,C14
18	CAP	400VAC 222 ±20% 10mm	1	C6
19	CAP	275V 104 ±20% 15mm	1	C13
20	CER.CAP	50V 473 ±20% 2.5mm	1	C10
21	ELEC.CAP	ELEC.CAP11 25V100U±20%6×12 2.5	5	CE1,CE2,CE12,CE14,CE16
22	ELEC.CAP	ELEC.CAP11 25V10U±10%5×11 2	1	CE7
23	ELEC.CAP	ELEC.CAP110 25V470U±20%10×16 5	2	CE3,CE4
24	ELEC.CAP	ELEC.CAP110 25V22U±20%5×11 2	1	CE11
25	ELEC.CAP	ELEC.CAP110 50V47U±20%6×12 2.5	1	CE13
26	ELEC.CAP	LS 400V100U±20%22×30 10	1	CE5
27	ELEC.CAP	ELEC.CAP110 16V220U±20%6×12 2.5	2	CE15,CE17
28	ELEC.CAP	GZ 10V2200U±20%10×20 5	2	CE6,CE9
29	ELEC.CAP	GZ 10V1000U±20%8×16 3.5	2	CE8,CE10
30	FERRITE BEAD	FB	3	L1,L2,L4
31	INDUCTOR IRON	10UH 3A 5mm	2	L3,L5
32	TRANSFOMER	BCK-28-0300	1	T1
33	DIODE	1N4007	4	D9,D10,D11,D12
34	DIODE	HER105	4	D1,D6,D7,D8
35	DIODE	HER107	1	D4
36	DIODE	HER303	1	D2
37	ZENER	5.1V 1/2W	1	D13

PARTS LIST power board

ITEM	DESCRIPTION		QTY	LOCATION
38	DIODE	MBR1060 TO-220	1	D3
39	DIODE	BYW29E-200 TO-220	1	D5
40	TRANSISTOR	2N5401	1	Q4
41	TRANSISTOR	2N5551	2	Q3,Q5
42	MOSFET	AP40N03P TO-220	2	Q1,Q2
43	IC	LM431ACZ TO-92	1	IC3
44	IC	PQ12RD21 TO-220	1	IC4
45	IC	ICE 2A265 DIP	1	IC1
46	INDUCTOR IRON	UT-20 40mH ±20% 10×13	1	LF1
47	THERM RESISTOR	NTC SCK-104MS±20%	1	RT1
48	OPTOTRANSISTOR	NEC2561	1	IC2
49	PCB	5AB9915-0	1	
50	WAFER	5P 2.5mm	1	CN2
51	WAFER	5P 2.0mm	1	CN5
52	WAFER	2P 2.5mm	1	CN1
53	WAFER	9P 2.5mm	1	CN3 1~9PIN
54	WAFER	4P 3.96mm	1	CN4
55	WAFER	2P 8.0mm 2#	1	BCN1
60	FUSE	T2AL 250V	1	F1
62	RADIATOR	11×15×31 LFDR9905	2	
64	RESISTOR	1/2W910K±5% 12.5×7	1	RV1

PARTS LIST AVV board

ITEM	DESCRIPTION		QTY	LOCATION
1	RESISTOR	1/16W 0Ω ±5%	7	R18,R33,R41,R55,R99,R108,R113
2	RESISTOR	1/16W 10Ω ±5%	2	R71,R66
3	RESISTOR	1/16W 22Ω ±5%	1	R23
4	RESISTOR	1/16W 220Ω ±5%	8	R1,R8,R36,R43,R63,R103,R110,R115
5	RESISTOR	1/16W 330Ω ±5%	6	R48,R59,R76,R83,R88,R95
6	RESISTOR	1/16W 470Ω ±5%	5	R37,R44,R104,R111,R116
7	RESISTOR	1/16W 1K ±5%	7	R26,R53,R56,R79,R80,R91,R92
8	RESISTOR	1/16W 2.2K ±5%	3	R68,R72,R131
9	RESISTOR	1/16W 3.3K ±5%	4	R119~R122
10	RESISTOR	1/16W 4.7K ±5%	15	R24,R40,R46,R47,R57,R58,R74,R75,R81,R82,R86,R87,R93,R94,R126
11	RESISTOR	1/16W 6.8K ±5%	10	R32,R35,R39,R42,R97,R102,R106,R109,R112,R114
12	RESISTOR	1/16W 10K ±5%	7	R4,R5,R29,R30,R69,R117,R118
13	RESISTOR	1/16W 20K ±5%	6	R45,R51,R73,R78,R85,R90
14	RESISTOR	1/16W 22K ±5%	1	R60
16	RESISTOR	1/16W 47K ±5%	6	R49,R62,R77,R84,R89,R96
17	RESISTOR	1/16W 100K ±5%	1	R52
18	RESISTOR	1/16W 100Ω ±5%	1	R123
19	RESISTOR	1/16W 30K ±5%	1	R67
20	RESISTOR	1/16W 3.9K ±5%	4	R2,R3,R25,R27
21	RESISTOR	1/16W 18Ω ±5%	4	R6,R9,R10,R16
22	ELEC.CAP	ELEC.CAP11 10V220U±20%6×12 2.5	6	C18,C25,C26,C60,C61,C63
23	ELEC.CAP	ELEC.CAP11 16V10U±20%5×11 2	6	C31,C36,C45,C49,C53,C57
24	ELEC.CAP	ELEC.CAP11 16V47U±20%5×11 2	4	C1,C7,C40,C42
25	ELEC.CAP	ELEC.CAP11 16V100U±20%6×12 2.5	2	C12,C39
26	ELEC.CAP	ELEC.CAP11 16V4.7U±20%5×11 2	7	C3~C6,C17,C23,C24
27	CER.CAP	50V 102 ±10% 0603	13	C20,C32,C33,C37,C38,C46,C47,C50,C51,C54,C55,C58,C59
28	CER.CAP	50V 103 ±10% 0603	5	C13,C19,C34,C41,C43,
29	CER.CAP	50V 20P ±5% 0603	1	C28
30	CER.CAP	50V104 ±20% 0603	6	C2,C9,C22,C27,C62,C65
31	CER.CAP	50V 151 ±5% NPO 0603	6	C30,C35,C44,C48,C52,C56
32	FERRITE BEAD	FCM1608K-221T05	12	R31,R34,R38,R98,R100,R101,R105,R107,C8,C10,C11,C15
33	ZENER	6.2V 1/2W	2	D1,D3
34	DIODE	1N4148	9	D2,D4~D8,D11,D12,D13
35	TRANSISTOR	3904	9	Q2,Q3,Q4,Q11,Q16~Q20
36	TRANSISTOR	3906	3	Q1,Q7,Q10
37	TRANSISTOR	8050D	6	Q5,Q8,Q12~Q15
38	IC	ELEC.CAP4052BCN DIP	1	U1
39	IC	PCF8563T SO8	1	U2
40	IC	RC4558D SOP	3	U3,U4,U5
41	CRYSTAL	32.768KHz 3×9	1	X1
42	TUNER	JS-6B2/L121	1	TUN1
43	OPTICAL OUTPUT	TP01A	1	OP1
44	BATTERY	CR2032	1	BT1
45	PCB	7AB9905K-2	1	