FS6128-04
PLL Clock Generator IC with VXCO

1.0 Key Features

- Phase-locked loop (PLL) device synthesizes output clock frequency from crystal oscillator or external reference clock
- On-chip tunable voltage-controlled crystal oscillator (VCXO) allows precise system frequency tuning
- Typically used for generation of MPEG-2 decoder clock
- 3.3V supply voltage
- Very low phase noise PLL
- Use with “pullable” 14pF crystals – no external padding capacitors required
- Small circuit board footprint (8-pin 0.150” SOIC)
- Custom frequency selections available - contact your local ON Semiconductor sales representative for more information

2.0 Description

The FS6128 is a monolithic CMOS clock generator IC designed to minimize cost and component count in digital video/audio systems.

At the core of the FS6128 is circuitry that implements a voltage-controlled crystal oscillator (VCXO) when an external resonator (nominally 13.5MHz) is attached. The VCXO allows device frequencies to be precisely adjusted for use in systems that have frequency matching requirements, such as digital satellite receivers.

A high-resolution phase-locked loop generates an output clock (CLK) through a post-divider. The CLK frequency is ratiometrically derived from the VCXO frequency. The locking of the CLK frequency to other system reference frequencies can eliminate unpredictable artifacts in video systems and reduce electromagnetic interference (EMI) due to frequency harmonic stacking.

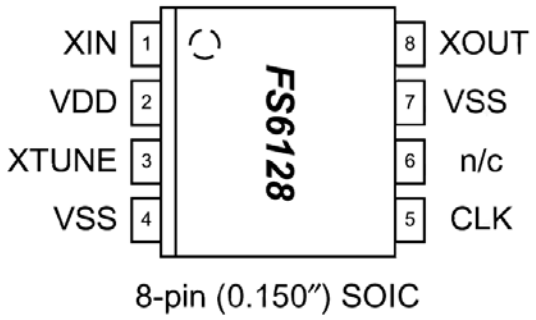

Figure 1: Pin Configuration

May 2008 – Rev. 2

Publication Order Number:
FS6128-04/D

Table 1: Crystal / Output Frequencies

Device	f_{XIN} (MHz)	CLK (MHz)
FS128-04	13.500	27.000

Note: Contact ON Semiconductor for custom PLL frequencies.

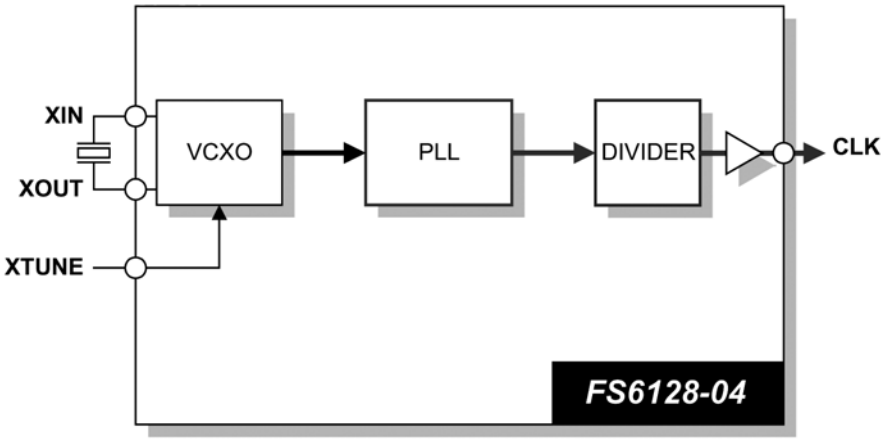

Figure 2: Block Diagram

Table 2: Pin Descriptions

Pin	Type	Name	Description
1	AI	XIN	VCXO feedback
2	P	VDD	Power supply (+3.3V)
3	AI	XTUNE	VCXO tune
4	P	VSS	Ground
5	DO	CLK	Clock output
6	-	n/c	No connection
7	DO	VSS	Ground
8	AO	XOUT	VCXO drive

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input With Internal Pull-Up; DI_D = Input With Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low Pin

3.0 Functional Block Diagram

3.1 Voltage-Controlled Crystal Oscillator (VCXO)

The VCXO provides a tunable, low-jitter frequency reference for the rest of the FS6128 system components. Loading capacitance for the crystal is internal to the FS6128. No external components (other than the resonator itself) are required for operation of the VCXO.

Continuous fine-tuning of the VCXO frequency is accomplished by varying the voltage on the XTUNE pin. The value of this voltage controls the effective capacitance presented to the crystal. The actual amount that this load capacitance change will alter the oscillator frequency depends on the characteristics of the crystal as well as the oscillator circuit itself.

It is important that the crystal load capacitance is specified correctly to “center” the tuning range. See Table 5.

A simple formula to obtain the “pulling” capability of a crystal oscillator is:

$$\Delta f\,(ppm) = \frac{C_1 \times (C_{L2} - C_{L1}) \times 10^6}{2 \times (C_0 + C_{L2}) \times (C_0 + C_{L1})}$$

where:
C_0 = the shunt (or holder) capacitance of the crystal
C_1 = the motional capacitance of the crystal
C_{L1} and C_{L2} = the two extremes (minimum and maximum) of the applied load capacitance presented by the FS6128.

EXAMPLE: A crystal with the following parameters is used: C_1 = 0.025pF and C_0 = 6pF. Using the minimum and maximum C_{L1} = 10pF, and C_{L2} = 20pF, the tuning range (peak-to-peak) is:

$$\Delta f = \frac{0.025 \times (20 - 10) \times 10^6}{2 \times (6 + 20) \times (6 + 10)} = 300\,ppm$$

3.2 Phase-Locked Loop (PLL)

The on-chip PLL is a standard frequency- and phase locked loop architecture. The PLL multiplies the reference oscillator frequency to the desired output frequency by a ratio of integers. The frequency multiplication is exact with a zero synthesis error (unless otherwise specified).

4.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage (V_{ss} = ground)	V_{DD}	V_{SS} – 0.5	7	V
Input voltage, DC	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage, DC	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Input clamp current, DC (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output clamp current, DC (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage temperature range (non-condensing)	T_S	-65	150	°C
Ambient temperature range, under bias	T_A	-55	125	°C
Junction temperature	T_J		125	°C
Re-flow solder profile				Per IPC/JEDEC J-STD-020B
Input static discharge voltage protection (MLD-STD 883E, Method 3015.7)			2	kv

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality and reliability.

CAUTION: ELECTROSTATIC SENSITIVE DEVICE
Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high energy electrostatic discharge.

Table 4: Operating Conditions

Parameter	Symbol	Conditions/Descriptions	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}	3.3V ± 10%	3.0	3.3	3.6	V
Ambient operating temperature range	T_A	0			70	°C
Crystal resonator frequency	f_{XTAL}	Functional mode	12	13.5	18	MHz

Table 5: DC Electrical Specifications

Parameter	Symbol	Conditions/Descriptions	Min.	Typ.	Max.	Units
Overall						
Supply current, dynamic, with loaded outputs	I_{DD}	f_{XAL} = 13.5MHz; CL = 10pF; VDD = 3.6V		30		mA
Supply current, static	I_{DD}	XIN = 0V; VDD = 3.6V		3		mA
Voltage-Controlled Crystal Oscillator (contact factory for approved crystal sources or other application assistance)						
Crystal loading capacitance at center tuning voltage	$C_{L(xtal)}$	Order crystal for this capacitance (parallel load) at desired center frequency		14		pF
Crystal resonator motional capacitance	C_1	Specified motional capacitance of the crystal will affect pullability (see text)		25		fF
XTUNE effective range			0		3	V
Synthesized load capacitance min.	C_{L1}	@V(XTUNE) = minimum value		10		pF
Synthesized load capacitance max.	C_{L2}	@V(XTUNE) = maximum value		20		pF
VCXO tuning range		f_{XTAL} = 13.5MHz; $C_{L(xtal)}$ = 14pF; C_1(xtal) = 25fF (peak-to-peak)		300		ppm
VCXO tuning characteristic		Note: positive change of XTUNE = positive change of VCXO frequency		150		ppm/V
Crystal drive level		R_{XTAL} = 20Ω; C_L = 20pF		200		µW
Clock Output (CLK)						
High-level output source current*	I_{OH}	V_O = 2.0V		-40		mA
Low-level output sink current*	I_{OL}	V_O = 0.4V		17		mA
Output impedance*	Z_{OH} Z_{OL}	V_O = 0.1V_{DD}; output driving high V_O = 0.1V_{DD}; output driving low		25 25		Ω
Short circuit source current*	I_{OSH}	V_O = 0V; shorted for 30s, max.		-55		mA
Short circuit sink current*	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		55		mA

Note: Unless otherwise stated V_{DD} = 3.3V ±10% no load on any output and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ±3σ from typical. Negative currents indicate current flows out of the device.

Table 6: AC Timing Specifications

Parameter	Symbol	Conditions/Descriptions	Min.	Typ.	Max.	Units
Overall						
VCXO stabilization time*	$t_{VCXOSTB}$	From power valid		10		ms
PLL stabilization time*	t_{PLLSTB}	From VCXO stable		100		µs
Synthesis error		(Unless otherwise noted in frequency table)		0		ppm
Clock Output (CLK)						
Duty cycle*		Ratio of high pulse width (as measured from rising edge to next falling edge at V_{DD}/2) to one clock period	45		55	%
Jitter, period (peak-peak)*	$t_{j(\Delta P)}$	From rising edge to next rising edge at V_{DD}/2, CL = 10pF 200 ps		200		ps
Jitter, long term ($\sigma_\gamma(\tau)$	$t_{j(LT)}$	From 0-500µs at V_{DD}/2, CL = 10pF compared to ideal clock source		100		ps
Rise time*	t_r	V_{DD} = 3.3V; V_O = 0.3V to 3.0V; C_L = 10pF		1.7		ns
Fall time*	t_f	V_{DD} = 3.3V; V_O = 3.0V to 0.3V; C_L = 10pF		1.7		ns

Note: Unless otherwise stated, V_{DD} = 3.3V ±10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ±3σ from typical.

5.0 Package Information – For Both ‘Green’ and ‘Non-Green’

Table 7: 8-pin SOIC (0.150") Package Dimensions

	Dimensions			
	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	.033	0.49
C	0.0075	0.0098	0.191	0.249
D	0.189	0.196	4.80	4.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

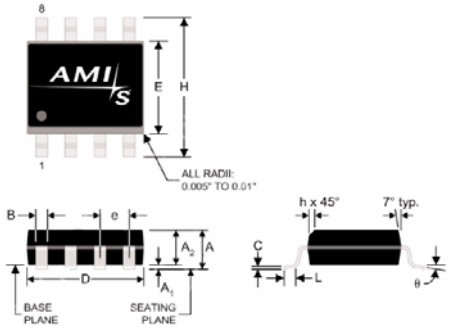

Table 8: 8-pin SOIC (0.150") Package Characteristics

Parameter	Symbol	Conditions/Descriptions	Typ.	Units
Thermal impedance, junction to free-air 8-pin 0.150” SOIC	Θ_{JA}	Air flow = 0 m/s	110	°C/W
Lead inductance, self	L_{11}	Corner lead	2.0	nH
Lead inductance, mutual	L_{12}	Center lead Any lead to any adjacent lead	1.6 0.4	nH
Lead capacitance, bulk	C_{11}	Andy lead to V_{SS}	0.27	pF

6.0 Ordering Information

Part Number	Package	Shipping Configuration	Temperature Range
FS6128-04G-XTD	8-pin (0.150”) SOIC ‘Green’ or lead-free packaging	Tube/Tray	0°C to 70°C (commercial)
FS6128-04G-XTP	8-pin (0.150”) SOIC ‘Green’ or lead-free packaging	Tape & Reel	0°C to 70°C (commercial)

7.0 Revision History

Revision	Date	Modification
1	March 2004	Initial release
2	May 2008	Update to new ON Semiconductor template

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855
Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative