HWD2161

1.1W 关断模式音频功率放大器

一、概述:

HWD2161 是一种桥式连接音频功率放大器，使用 5V 电压源，能给一个 8Ω的负载传输 1.1W 的平均连续功率，THD+N 为 1%。

HWD2161 音频功率放大器是为提供高质量的输出功率而设计的，它采用表面封装技术，外部组件最少。HWD2161 不需要输出耦合电容、自举电容和缓冲器网络，它最适合低功率便携式系统。

HWD2161 采用外部控制的低功耗关断模式，以及内部热敏关断保护机制。

整体增益稳定的 HWD2161 可以通过外部增益配置电阻设置一直到 10 的差动增益，而不必使用外部补偿成分。更高的增益则可通过适当的补偿获得。

二、重要规格

1．1kHz，1W 连续平均输出功率，8Ω负载。THD+N 为 :1.0%(最大)

2．1kHz，10%的 THD+N。 输出功率为 :1.5(典型)

3．关断电流 ： 0.6μA (典型)

三、特征

1. 不需要输出耦合电容、自举电容或缓冲电路
2. 外形小
3. 和 PC 电源兼容
4. 整体增益稳定
5. 具有外部增益配置能力

四、应用

1. 个人计算机
2. 便携式消费产品
3. 自动扬声器
4. 玩具、游戏

五、绝对最大额定值

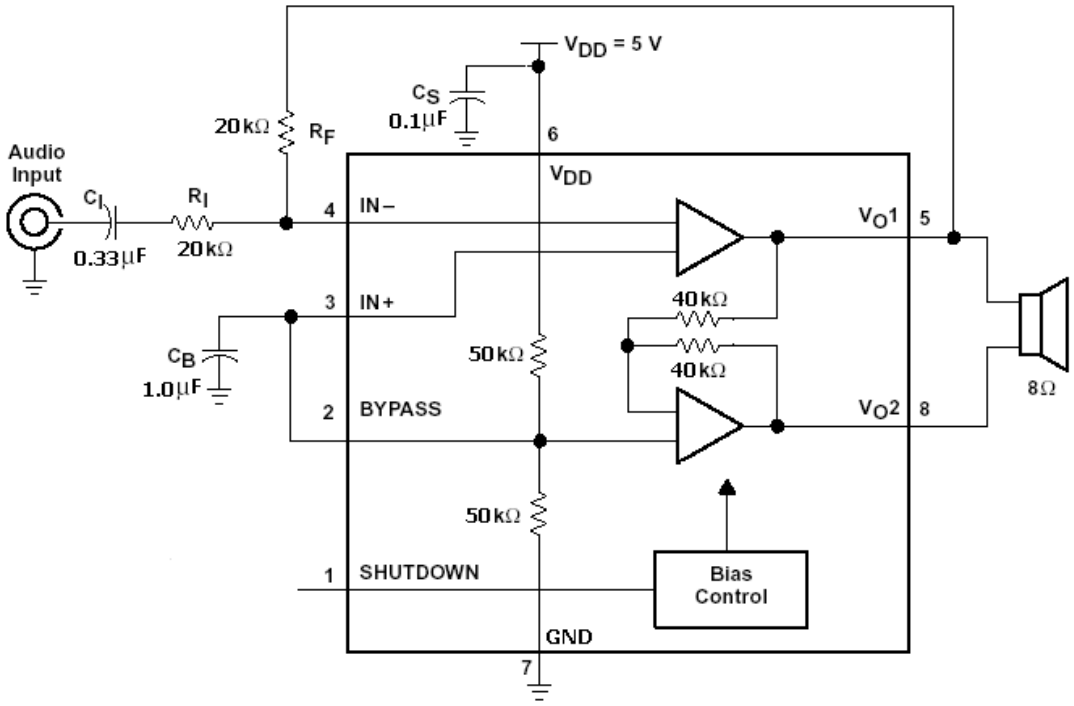
电源电压	6.0V
存储温度	- 65 ℃ ～ + 150 ℃

输入电压	- 0.3v ～ + 0.3v
功耗(注释 3)	内部限制
ESD 磁化系数(注释 4)	3000v
ESD 磁化系数(注释 5)	250v
结温	150 °C
焊接信息	
小型包装	
气化态(60 秒)	215 °C
红外线(15 秒)	220 °C

六、工作额定值

温度范围 $T_{MIN} \leqslant T_A \leqslant T_{MAX}$	- 40 °C$\leqslant T_A \leqslant$+ 85 °C
电源电压	2.0V$\leqslant V_{DD} \leqslant$5.5V
热阻 θ_{JC}(典型) -M80A	35 °C /W
θ_{JA}(典型) -M80A	140 °C/W
θ_{JC}(典型) -M80E	37 °C/W
θ_{JA}(典型) -M80E	107 °C/W

七、典型应用

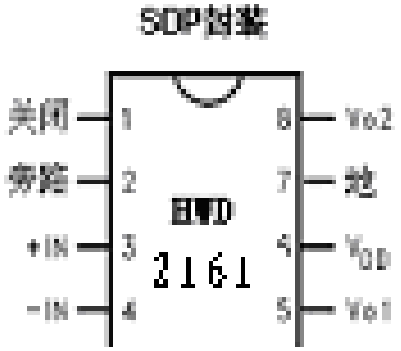


图（1）HWD2161 典型应用电路

外部组件描述

组件	功能描述
1. R_i	反相输入电阻，连接 R_f 建立死循环增益，与 C_i 形成高通滤波器
2. C_i	输入耦合电容，阻止输入端直流电压，和 R_i 形成高通滤波器
3. R_f	反馈电阻，连接 R_i 建立死循环增益
4. C_s	电源旁路电容，提供电源滤波
5. C_B	旁路电极电容，提供电源滤波
6. C_f	连接 R_f 产生低通滤波器，其带宽约束放大器，防止可能产生的高平振荡

封装形式



八、电学特性(除非另外指明，以下都是 V_{DD}=5V，限制应用在 Ta=25 °C)

符号	参　　数	条　　件	HWD2161		单 位
			标　　准 (note6)	限　　制 (note7)	
V_{DD}	电源电压			2.0 5.5	V(min) V(max)
I_{DD}	静态功耗 电源电流	V_{IN}=0V I_O=0A(note8)	6.5	10.0	mA(max)
I_{SD}	关断电流	$V_{pin1}=V_{DD}$	0.6	10.0	uA(max)
V_{OS}	输出偏置电压	V_{IN}=0V	5.0	50.0	mV(max)
P_O	输出功率	THD=1%(max)f=1kHz	1.1	1.0	W(min)
THD+N	总谐波失真+噪声	P_O=1Wrms 20Hz≤f≤20kHz	0.72		%
PSRR	电源抑制比	V_{DD}=4.9V～5.1V	65		dB

注释 1:如果没有额外的说明，所有电压都以地面引脚为标准。

注释 2:绝对最大额度值是指器件可能发生损害的界限，操作额度是指设备工作条件，但不能保证特殊的性能界限。在保证特定的工作范围的精确测试条件下，电学特性规定了直流和交流的电学规格，这时认为设备就是在工作额度内。说明书没有参数的范围，然而，这些参数值却是设备性能的一个很好的体现。

注释 3:当升高温度时必须降低最大功耗，最大功耗可用 T_{jmax}, θ_{JA}和环境温度 T_A来确定，最大允许功耗为: $P_{DMAX}=(T_{jmax}-T_A)/\theta_{JA}$, 或者是绝对最大额度值中给出的数值，任何一个都会更低。对 HWD2161 来说， T_{jmax}=150 °C，当版面固定时，标准结点的环境热电阻是 140 °C/W。

注释 4:对于人体模型，100pF 电容通过 1.5Ω 电阻放电。

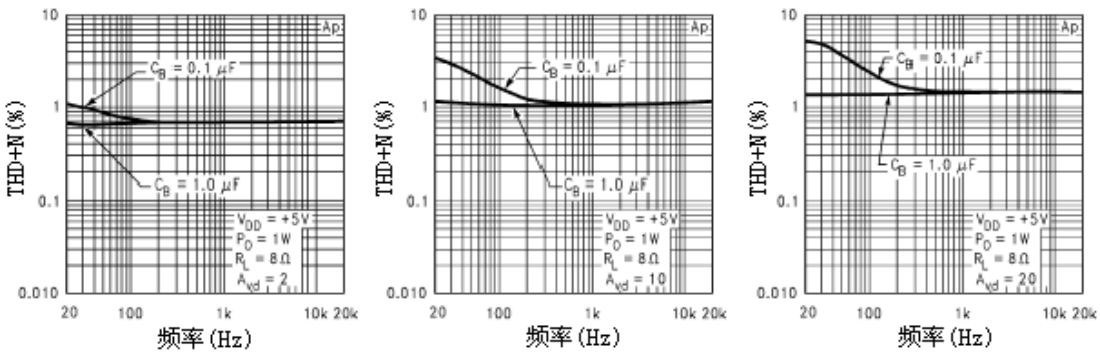
注释 5:器件模型，220PF～240PF 电容通过全部引脚放电。

注释 6:标准被定在 25 °C，以代表参数规格。

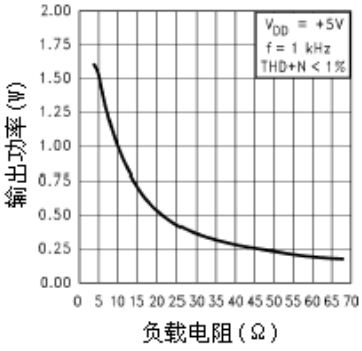
注释 7:限制确保在国际平均输出质量标准内。

注释 8:当实际的负载被连接到放大器时，这个静态电源电流依赖于偏置电压。

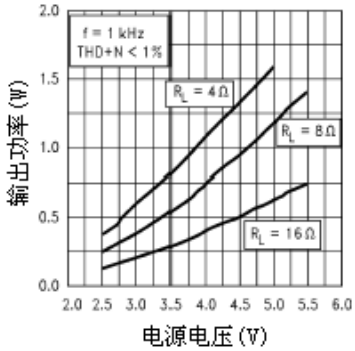
九、典型性能特征曲线



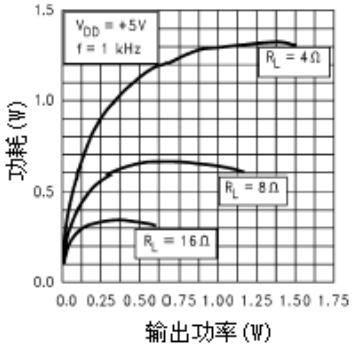
失真度与频率



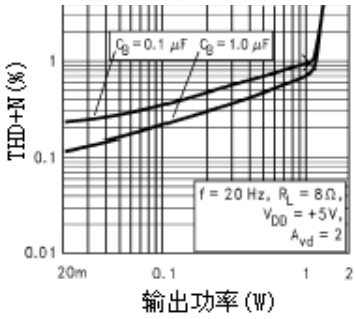
输出功率与负载电阻

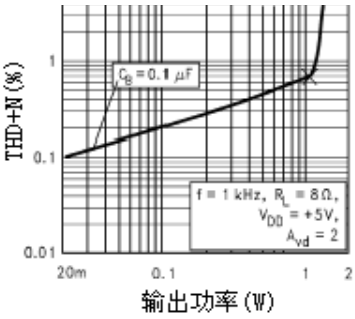


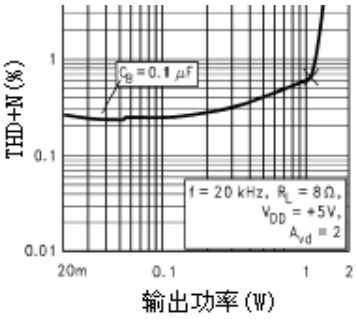
输出功率与电源电压



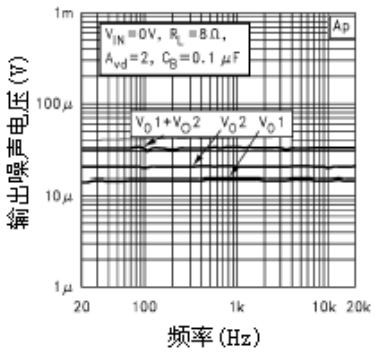
功耗与输出功率



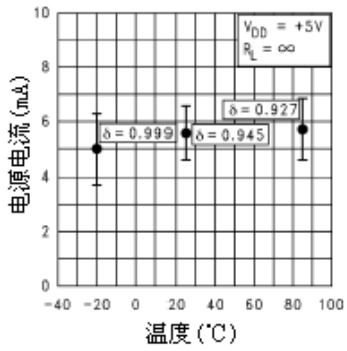




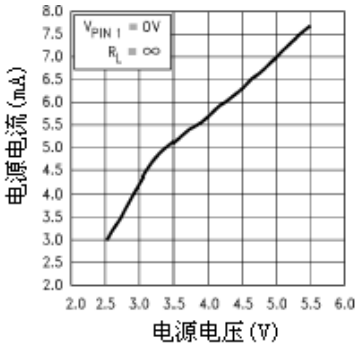
失真度与输出功率



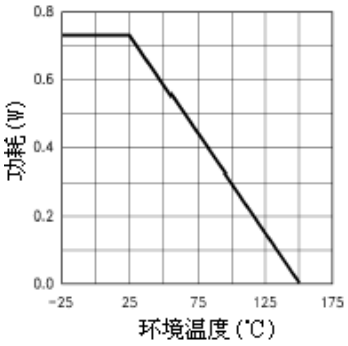
噪声与频率



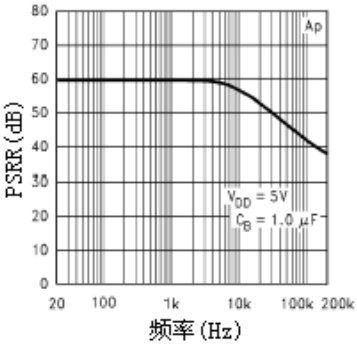
电源电流与温度



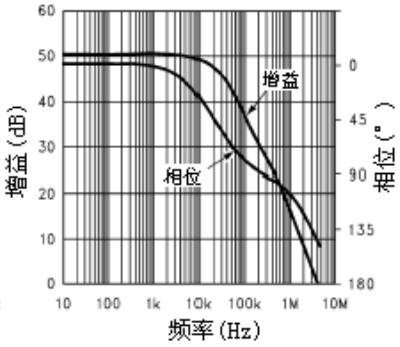
电源电流与电源电压



功率下降曲线



电源抑制比



开环频率响应

十、应用信息

1. 桥式功能

如图(1)所示，HWD2161 内部有两个运算放大器，允许少数不同的放大器配置，第一个放大器的增益是外部结构，而第二个放大器在整体增益中被内部固定，是倒相装置。

第一个放大器的死循环增益通过选择 R_f 和 R_i 的比值来决定，而第二个放大器的增益则通过两个 40kΩ 的内部电阻固定。图(1)表明放大器 1 的输出作为放大器 2 的输入，这样导致两个放大器产生大量相同信号，但相位相差 180° 。因此，该 IC 的差动增益为：$A_{VD}=2(R_f/R_i)$。通过输出端 V_{O1} 和 V_{O2} 驱动不同的负载，一个通常被称作“桥式模型”的放大器就确定了。桥式模型的运行不同于传统的单终端放大器结构，在单终端结构中负载的一端接地。桥式放大器设计比单终端结构有一些明显的优点。当它给负载提供差动驱动时，双输出差动作为一确定的电源电压。因此，在相同条件下，输出功率可能是单终端放大器的 4 倍。

在可获得的输出功率中，这种增加假定放大器没有电流限制或断路。过分失真将会损坏扬声器系统中的高频率传感器，为了选择一个不引起过分失真的放大器死循环增益，请参考《HWD2161 技术说明》中“音频功率放大器设计”部分。

桥式结构，正如用在音频放大器中的一样，也产生了优于单终端放大器的第二个优点。由于差动输出 V_{O1} 和 V_{O2} 在半供给中偏置，通过负载不存在净直流电压，这就消除了输出耦合电容。但在单电源 、单终端放大器中则需要输出耦合电容，否则，通过负载的半供给偏置就会导致内部 IC 功耗的增加，以及扩音器永久性损坏。输出耦合电容和负载形成一个高通滤波器，要求 470μF 的电容和 8Ω 负载，以保持低频响应。这种组合不会产生降至 20Hz 的平带回应，但相对于低频响应，它能在印制的电路板尺寸和系统成本之间提供一种折衷。

2．电源旁路

对于任何功率放大器，适当的电源旁路对于低噪音运行和高电源截止是很关键的。在旁路和电源插头上的电容器应尽可能靠近旁路。就如在典型工作特性一节所阐述的，由于增加了半供给的稳定性，一个更大的旁路电容的影响，改善了低频 THD+N。典型运用中，使用一个 5V 的调节器，这个调节器具有一个 10μF 和一个 0.1μF 的旁路电容，有助于电源稳定，但不能消除 HWD2161 的旁路电源的节点。旁路电容的选择，特别是 C_B，依赖于低频 THD+N、系统成本和尺寸约束。

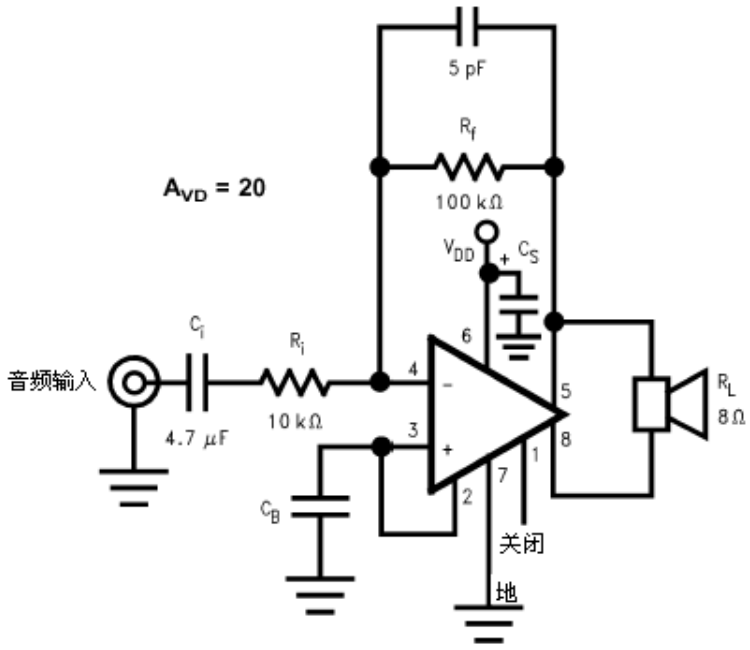
3．关断功能

为了减少不使用时的功耗，HWD2161 用一个关断引线从外部断开放大器的偏置电路。当一个逻辑高电平加在关断引线上时，关断部件就会断开放大器。一旦进入断开状态，输出立刻和扬声器分开。当电源电压加在关断引线上时，就产生一个 0.6μA 的标准静态电流。在许多应用中，一个微控制器或微处理器输出用来控制关断电路，它使电路迅速、平稳的转向关断状态。另一个方法是关断时使用一个单极、单掷开关进行切换，它接地使放大器启动。如果开关打开，一个 47KΩ 的软上拉电阻使 HWD2161 至截止。在 HWD2161 中没有软上拉电阻。因此，一个确定的关断引线电压必须由外部供给或者内部逻辑门悬空，它能意外地停止放大器运行。

4．高增益音频放大器

HWD2161 整体增益稳定，在典型应用中，除了增益设置电阻、一个输入耦合电容和一个适当的旁路电源外，不需要其它的外部组件。但是如果要求大于 10 的闭环差动增益，则

需要加入一个反馈电容，由带宽限制放大器，如图(2)所示。反馈电容形成一个低通滤波器，以消除可能出现的高频振荡。计算-3dB 频率时，应该注意 R_F 和 C_F 搭配不当会引起 20kHz 前的衰减。一种标准的反馈电阻和电容组合不会产生音频范围内的高频衰减，即 R_F=100kΩ、C_F=5pF。这种组合会产生一个大约 320kHz 的-3dB 点。一旦计算出放大器的差动增益，就可选择 R_F，而且 C_F 也能由“外部组件描述”一节中所表述的公式计算出来。

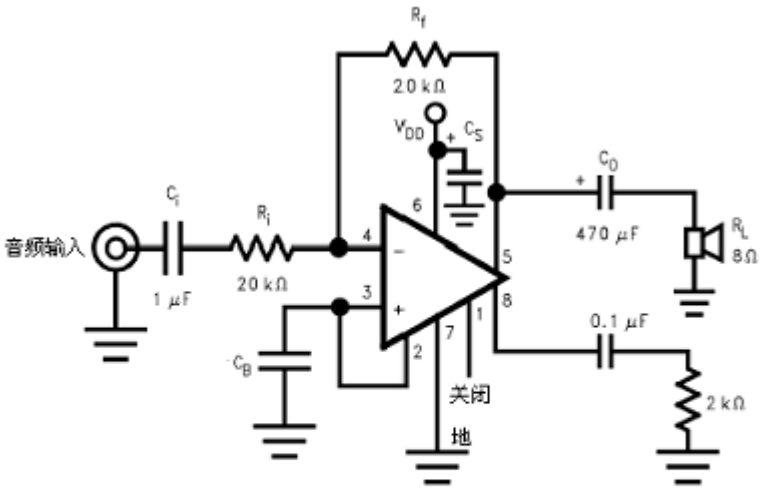


图（2）高增益电路

5．单端音频放大器

HWD2161 的典型应用是桥式单声道放大器，但它也可用来驱动一个单端负载，例如 PC 卡，它要求负载的一端接地。图（3）展示了一个普通的单端应用，这里 V_{01} 用来驱动扬声器。输出通过一个 470μF 的电容耦合，这个电容可以阻止所有单电源放大器装置中的半供给直流偏置。这个电容，在图（3）中标记为 C_0，和 R_L 连接形成一个高通滤波器。这个高通滤波器的-3dB 点是 $1/(2\pi R_L C_O)$，因此，应确保产品的 R_L 和 C_O 足够大，以能使低频信

号传到负载。当驱动一个 8Ω 负载时，若要求再现全部音频范围，则 C_O 至少为 470μF。输出 V_{02} 是没有用的，通过一个 0.1μF 的电容连到一个 2kΩ 负载上，以增加稳定性。但这种（不）稳定性将不会影响 V_{01} 的波形，它是实现二次输出的一个很好设计。



CB及Cs取值视需要而定，典型值为0.1uF
管脚1连至VDD关闭放大器或连至地开启放大器，不可悬空
管脚8上作为伪负载连接的电阻和电容起稳定作用

图（3） 单端应用电路

6．音频功率放大器的设计

设计一个 1W/8Ω 音频放大器，给定条件：

功率输出	1Wrms
负载阻抗	8Ω
输入电平	1Vrms
输入阻抗	20KΩ
带宽	100Hz~20KHz±0.25dB

设计者必须首先确定所需的电源范围，以获得规定的输出功率。在“典型运行特性”一节中，从“输出功率对电源电压”曲线图，可以很容易推出电源范围。确定最小电源范围的第二种方式是用等式（3）计算所需的 V_{OPEAK}，并增加开路电压。使用这种方法，最小的电源电压为（$V_{OPEAK}+V_{OD}$），其中 $V_{OD}=0.6V$。

$$V_{OPEAK} = (2R_LP_O) \qquad (3)$$

为使 1W 的输出功率带动 8Ω 负载，要求 V_{OPEAK} 为 4.0V，由 $V_{OPEAK}+V_{OD}$ 得到最小电压 4.6 V。但在许多应用中，4.6 V 并不是标准电压，由于这个原因，设计了 5 V 的电源范围，额外的电源电压产生的动态空间允许 HWD2161 再现一个峰值超过 1W 而没有被剪切的信号。同时设计者必须确定电源电压的选择和输出阻抗不能超过在“功耗”一节中所阐述的条件。

一旦功耗因素被确定，所要求的差动增益就可由等式（4）确定。

$$A_{VD} \geq (P_OR_L)/(VIN) = Vorms / Vinrms \qquad (4)$$

$$Rf/Ri = A_{VD} / 2 \qquad (5)$$

由等式（4）得：最小的 $A_{VD}=2.83$，取 $A_{VD}=3$。

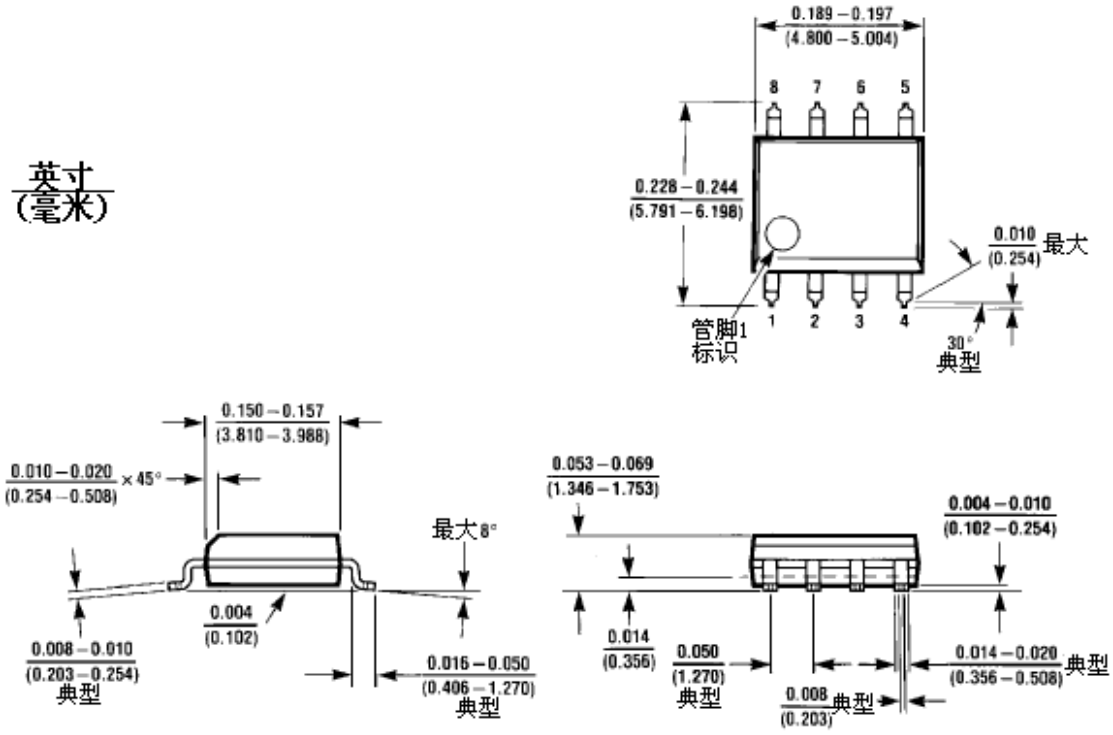
由于要求输入阻抗为 20 kΩ，且 $A_{VD}=3$，$Rf/R_i=1/1.5$，使得 $R_i=20$ KΩ，Rf=30 KΩ。最后的设计是确定带宽规格，它必须作为-3dB 频率点的一部分来规定。-3dB 点的 5 倍频程处正是从平带响应下降 0.17dB，这比所要求的±0.25dB 要好。这就使得低频和高频极点分别为 20Hz 和 100kHz，如在“外部组件”一节中所描述的，R_i 和 C_i 连接形成一个高通滤波器。

$$C \geq 1 / (2\pi * 20k\Omega * 20Hz) = 0.397\mu f ; \quad 取\ 0.39\mu F$$

高频极值由产品所规定的高频极值 f_H 和差动增益 A_{VD} 来决定。由 $A_{VD}=2$，$f_H=100KHz$ 可得 GBWP=100KHz，这比 HWD2161 的 4MHz 的 GBWP 小得多。该数据表明，如果设计者要设计一个高增益放大器，HWD2161 仍然适用而不会产生带宽问题。

十一、SOP 封装参数

英寸
(毫米)


0.189 – 0.197
(4.800 – 5.004)
8 7 6 5
0.228 – 0.244
(5.791 – 6.198)
0.010
(0.254) 最大
管脚1
标识
1 2 3 4
30°
典型
0.150 – 0.157
(3.810 – 3.988)
0.010 – 0.020
(0.254 – 0.508) × 45°
最大8°
0.004
(0.102)
0.008 – 0.010
(0.203 – 0.254)
典型
0.015 – 0.050
(0.406 – 1.270)
典型
0.053 – 0.069
(1.346 – 1.753)
0.004 – 0.010
(0.102 – 0.254)
0.014
(0.356)
0.050
(1.270)
典型
0.008
(0.203)
典型
0.014 – 0.020
(0.356 – 0.508)
典型

HWD2161
1.1W Audio Power Amplifier with Shutdown Mode

General Description

The HWD2161 is a bridge-connected audio power amplifier capable of delivering 1.1W of continuous average power to an 8Ω load with 1% THD+N using a 5V power supply.

audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the HWD2161 does not require output coupling capacitors, bootstrap capacitors, or snubber networks, it is optimally suited for low-power portable systems.

The HWD2161 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable HWD2161 can be configured by external gain-setting resistors for differential gains of up to 10 without the use of external compensation components. Higher gains may be achieved with suitable compensation.

Key Specifications

- THD+N for 1kHz at 1W continuous average output power into 8Ω — 1.0% (max)
- Output power at 10% THD+N at 1kHz into 8Ω — 1.5W (typ)
- Shutdown Current — 0.6µA (typ)

Features

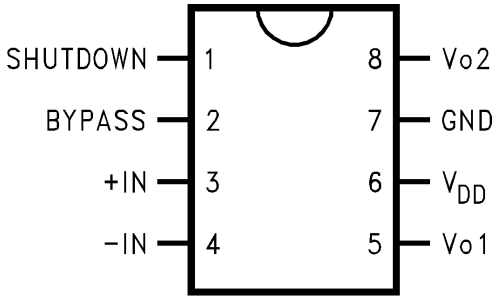
- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Small Outline (SO) packaging
- Compatible with PC power supplies
- Thermal shutdown protection circuitry
- Unity-gain stable
- External gain configuration capability

Applications

- Personal computers
- Portable consumer products
- Self-powered speakers
- Toys and games

Connection Diagram

Small Outline Package



Top View
Order Number HWD2161M

Typical Application

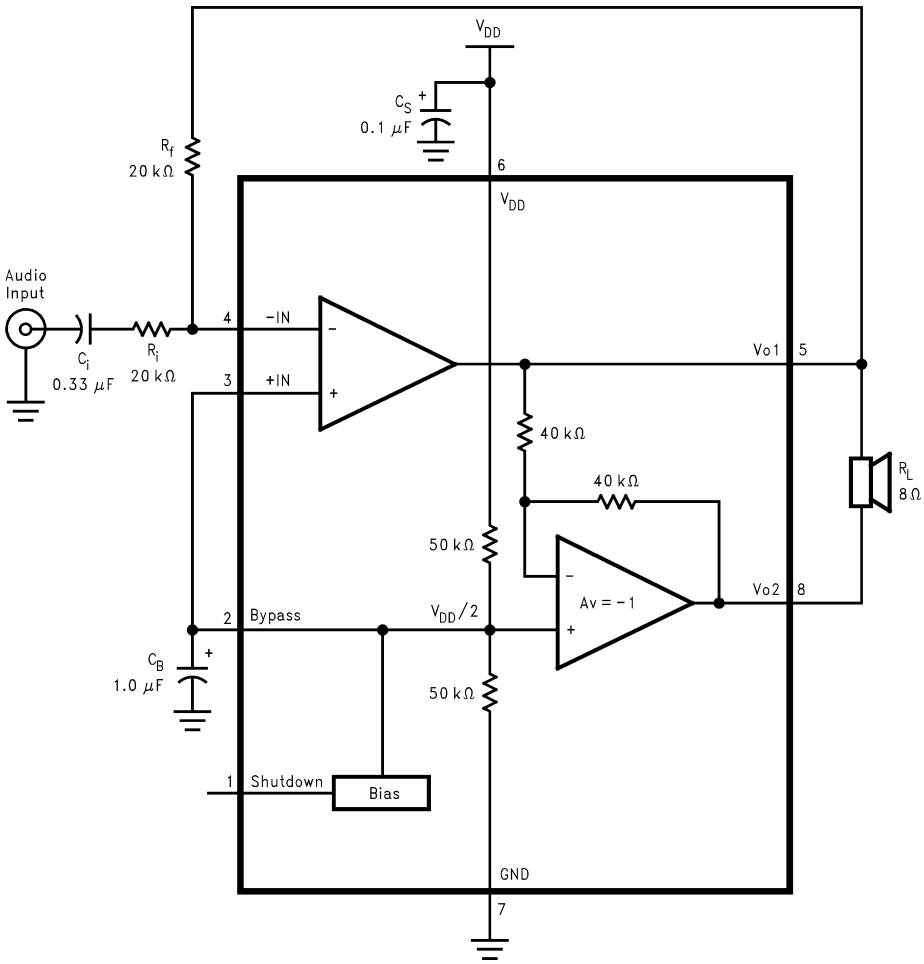


FIGURE 1. Typical Audio Amplifier Application Circuit

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the ©SMSC Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	−65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} + 0.3V
Power Dissipation (Note 3)	Internally limited
ESD Susceptibility (Note 4)	3000V
ESD Susceptibility (Note 5)	250V
Junction Temperature	150˚C
Soldering Information	
Small Outline Package	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 *"Surface Mounting and their Effects on Product Reliability"* for other methods of soldering surface mount devices.

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	−40˚C ≤ T_A ≤ +85˚C
Supply Voltage	2.0V ≤ V_{DD} ≤ 5.5V
Thermal Resistance	
θ_{JC} (typ)—M08A	35˚C/W
θ_{JA} (typ)—M08A	140˚C/W
θ_{JC} (typ)—N08E	37˚C/W
θ_{JA} (typ)—N08E	107˚C/W

Electrical Characteristics (Note 1) (Note 2)

The following specifications apply for V_{DD} = 5V, unless otherwise specified. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	HWD2161		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
V_{DD}	Supply Voltage			2.0 5.5	V (min) V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (Note 8)	6.5	10.0	mA (max)
I_{SD}	Shutdown Current	V_{pin1} = V_{DD}	0.6	10.0	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5.0	50.0	mV (max)
P_O	Output Power	THD = 1% (max); f = 1 kHz	1.1	1.0	W (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 1Wrms; 20 Hz ≤ f ≤ 20 kHz	0.72		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 4.9V to 5.1V	65		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the HWD2161, T_{JMAX} = 150˚C, and the typical junction-to-ambient thermal resistance, when board mounted, is 140˚C/W.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF–240pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

High Gain Application Circuit

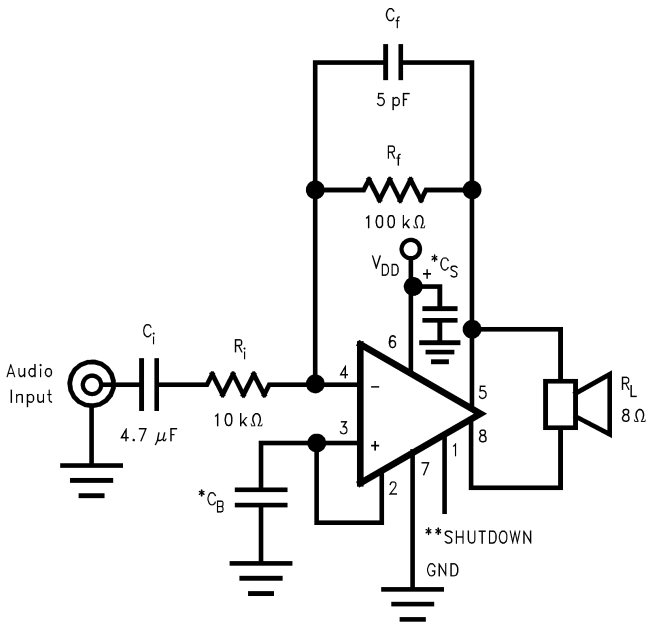
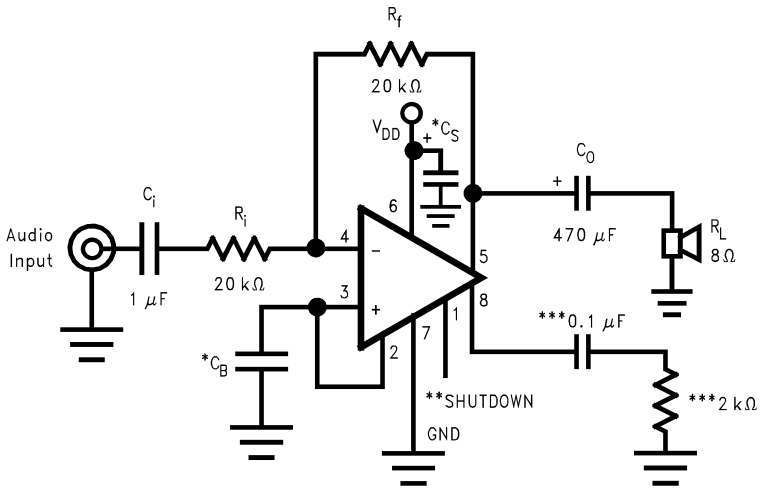


FIGURE 2. Audio Ampiifier with A_{VD} = 20

Single Ended Application Circuit



*C_S and C_B size depend on specific application requirements and constraints. Typical vaiues of C_S and C_B are 0.1 μF.

**Pin 1 should be connected to V_{DD} to disable the amplifier or to GND to enable the amplifier. This pin should not be left floating.

***These components create a “dummy” load for pin 8 for stability purposes.

FIGURE 3. Single-Ended Amplifier with A_V = –1

External Components Description

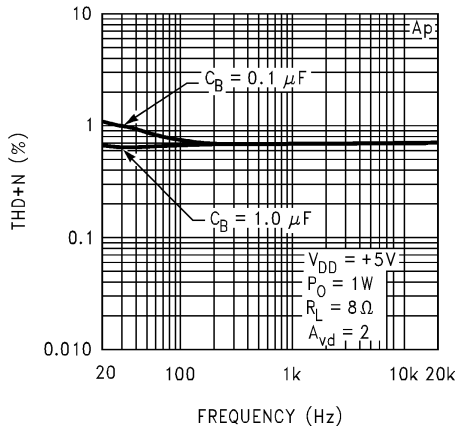
(*Figures 1, 2*)

Components	Functional Description
1. R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1 / (2\pi R_i C_i)$.
2. C_i	Input coupling capacitor which blocks DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_i at $f_C = 1 / (2\pi R_i C_i)$.
3. R_f	Feedback resistance which sets closed-loop gain in conjunction with R_i.
4. C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Application Information** section for proper placement and selection of supply bypass capacitor.
5. C_B	Bypass pin capacitor which provides half supply filtering. Refer to the **Application Information** section for proper placement and selection of bypass capacitor.
6. C_f (Note 9)	C_f in conjunction with R_f creates a low-pass filter which bandwidth limits the amplifier and prevents possible high frequency oscillation bursts. $f_C = 1 / (2\pi R_f C_f)$

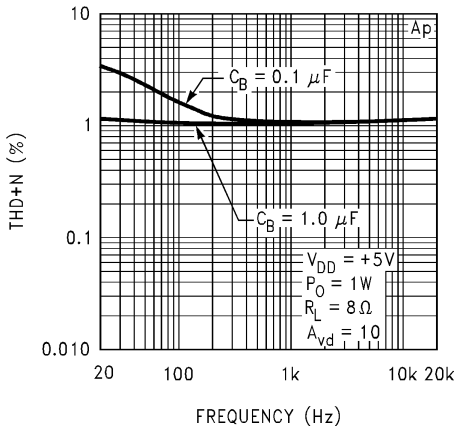
Note 9: Optional component dependent upon specific design requirements. Refer to the **Application Information** section for more information.

Typical Performance Characteristics

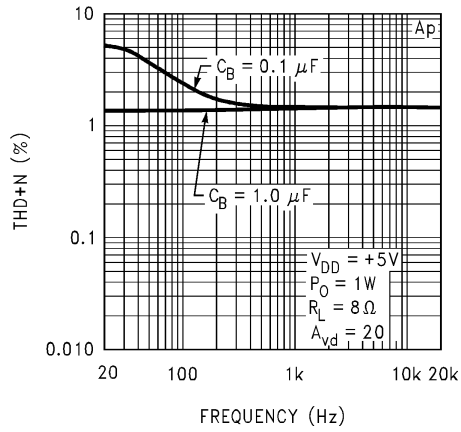
THD+N vs Frequency



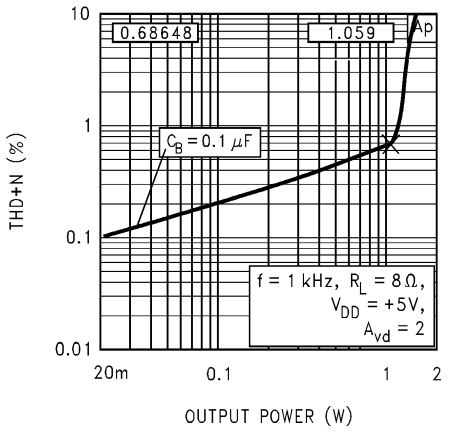
THD+N vs Frequency



THD+N vs Frequency

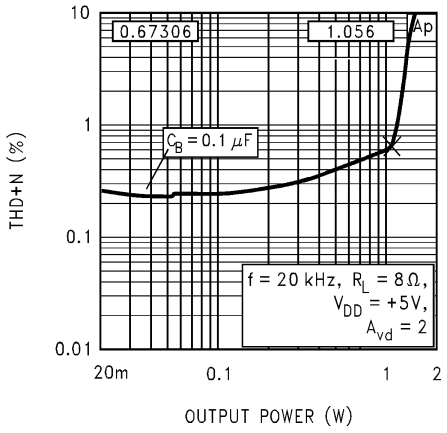


THD+N vs Output Power

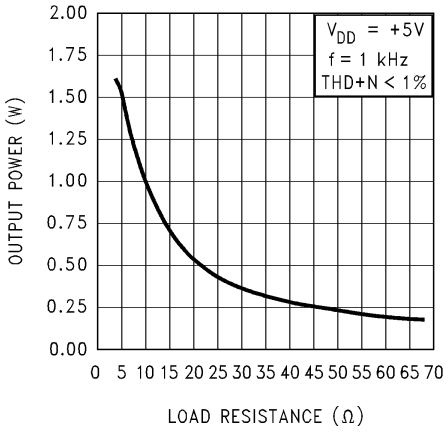


Typical Performance Characteristics (Continued)

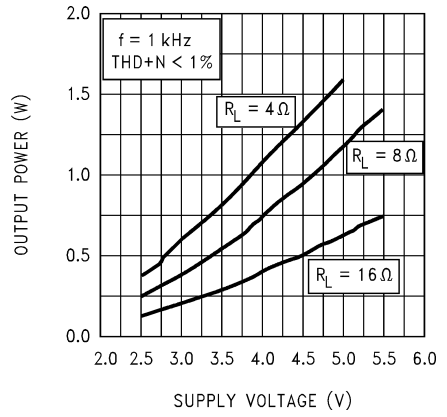
THD+N vs Output Power



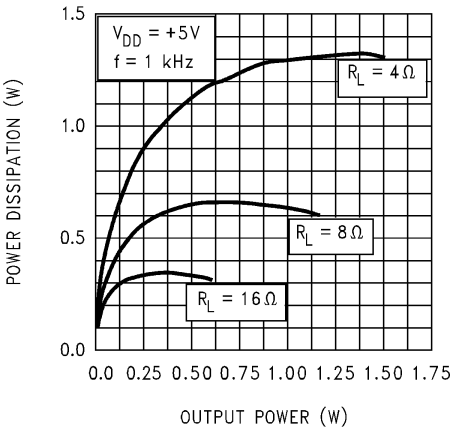
Output Power vs Load Resistance



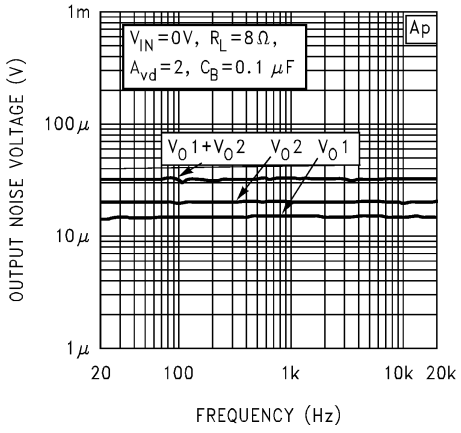
Output Power vs Supply Voltage



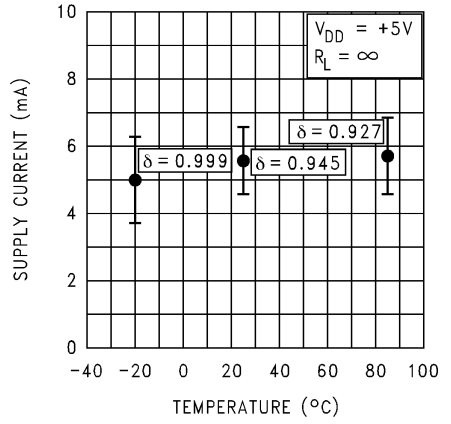
Power Dissipation vs Output Power



Noise Floor vs Frequency

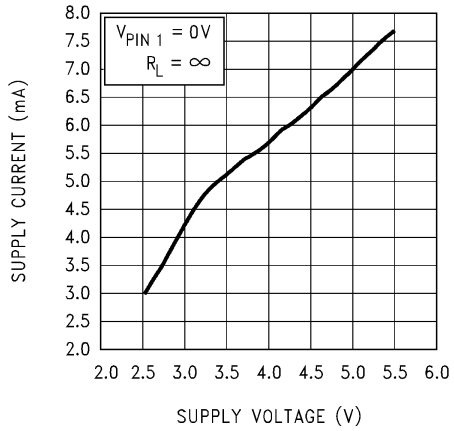


Supply Current Distribution vs Temperature

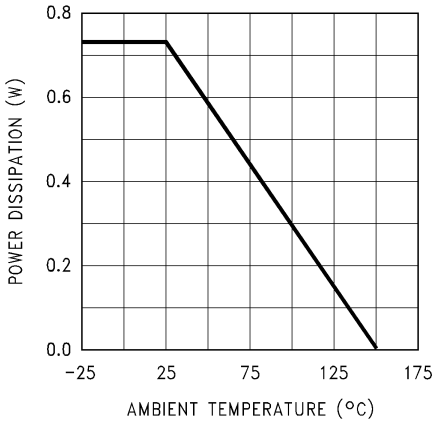


Typical Performance Characteristics (Continued)

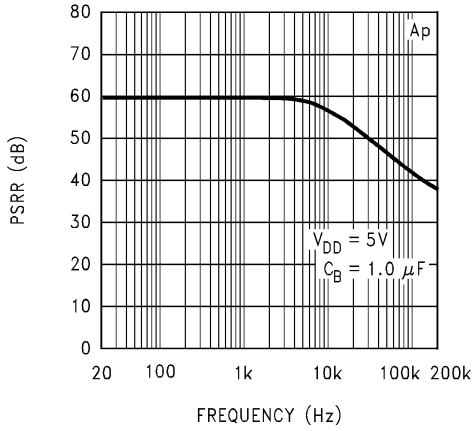
Supply Current vs Supply Voltage



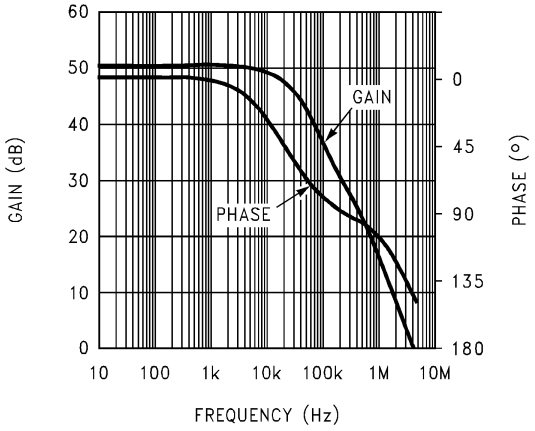
Power Derating Curve



Power Supply Rejection Ratio



Open Loop Frequency Response



Application Information

BRIDGE CONFIGURATION EXPLANATION

As shown in *Figure 1* , the HWD2161 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 40kΩ resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase 180˚. Consequently, the differential gain for the IC is:

$$A_{vd} = 2 * (R_f / R_i)$$

By driving the load differentially through outputs V_{O1} and V_{O2}, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Consequently, four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping which will damage high frequency transducers used in loudspeaker systems, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in Audio Power Amplifiers, also creates a second advantage over single-ended amplifiers. Since the differential outputs, V_{O1} and V_{O2}, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor in a single supply, single-ended amplifier, the half-supply bias across the load would result in both increased internal IC power dissipation and also permanent loudspeaker damage. An output coupling capacitor forms a high pass filter with the load requiring that a large value such as 470µF be used with an 8Ω load to preserve low frequency response. This combination does not produce a flat response down to 20Hz, but does offer a compromise between printed circuit board size and system cost, versus low frequency response.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Equation 1 states the maximum power dissipation point for a bridge amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = 4*(V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

Since the HWD2161 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the HWD2161 does not require heatsinking. From Equation 1, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 625mW.The maximum power dissipation point obtained from Equation 1 must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (2)$$

For the HWD2161 surface mount package θ_{JA} = 140˚C/W and T_{JMAX} = 150˚C. Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased or the load impedance increased. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 62.5˚C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to the **Typical Performance Characteristics** curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. As displayed in the **Typical Performance Characteristics** section, the effect of a larger half supply bypass capacitor is improved low frequency THD+N due to increased half-supply stability. Typical applications employ a 5V regulator with 10µF and a 0.1µF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the HWD2161. The selection of bypass capacitors, especially C_B, is thus dependant upon desired low frequency THD+N, system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the HWD2161 contains a shutdown pin to externally turn off the amplifier's bias circuitry. The shutdown feature turns the amplifier off when a logic high is placed on the shutdown pin. Upon going into shutdown, the output is immediately disconnected from the speaker. A typical quiescent current of 0.6µA results when the supply voltage is applied to the shutdown pin. In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch that when closed, is connected to ground and enables the amplifier. If the switch is open, then a soft pull-up resistor of 47kΩ will disable the HWD2161. There are no soft pull-down resistors inside the HWD2161, so a definite shutdown pin voltage must be applied externally, or the internal logic gate will be left floating which could disable the amplifier unexpectedly.

HIGHER GAIN AUDIO AMPLIFIER

The HWD2161 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor may be needed, as shown in *Figure 2*, to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates

Application Information (Continued)

possible high frequency oscillations. Care should be taken when calculating the –3dB frequency in that an incorrect combination of R_f and C_f will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_f = 100kΩ and C_f = 5pF. These components result in a –3dB point of approximately 320kHz. Once the differential gain of the amplifier has been calculated, a choice of R_f will result, and C_f can then be calculated from the formula stated in the **External Components Description** section.

VOICE-BAND AUDIO AMPLIFIER

Many applications, such as telephony, only require a voice-band frequency response. Such an application usually requires a flat frequency response from 300Hz to 3.5kHz. By adjusting the component values of *Figure 2*, this common application requirement can be implemented. The combination of R_i and C_i form a highpass filter while R_f and C_f form a lowpass filter. Using the typical voice-band frequency range, with a passband differential gain of approximately 100, the following values of R_i, C_i, R_f, and C_f follow from the equations stated in the **External Components Description** section.

R_i = 10kΩ, R_f = 510k ,C_i = 0.22µF, and C_f = 15pF

Five times away from a –3dB point is 0.17dB down from the flatband response. With this selection of components, the resulting –3dB points, f_L and f_H, are 72Hz and 20kHz, respectively, resulting in a flatband frequency response of better than ±0.25dB with a rolloff of 6dB/octave outside of the passband. If a steeper rolloff is required, other common bandpass filtering techniques can be used to achieve higher order filters.

SINGLE-ENDED AUDIO AMPLIFIER

Although the typical application for the HWD2161 is a bridged monoaural amp, it can also be used to drive a load single-endedly in applications, such as PC cards, which require that one side of the load is tied to ground. *Figure 3* shows a common single-ended application, where V_{O1} is used to drive the speaker. This output is coupled through a 470µF capacitor, which blocks the half-supply DC bias that exists in all single-supply amplifier configurations. This capacitor, designated C_O in *Figure 3*, in conjunction with R_L, forms a highpass filter. The –3dB point of this high pass filter is $1/(2\pi R_L C_O)$, so care should be taken to make sure that the product of R_L and C_O is large enough to pass low frequencies to the load. When driving an 8Ω load, and if a full audio spectrum reproduction is required, C_O should be at least 470µF. V_{O2}, the output that is not used, is connected through a 0.1 µF capacitor to a 2kΩ load to prevent instability. While such an instability will not affect the waveform of V_{O1}, it is good design practice to load the second output.

AUDIO POWER AMPLIFIER DESIGN

Design a 1W / 8Ω Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the needed supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graph in the **Typical Performance Characteristics** section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{opeak} using Equation 3 and add the dropout voltage. Using this method, the minimum supply voltage would be (V_{opeak} + V_{OD} , where V_{OD} is typically 0.6V.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (3)$$

For 1W of output power into an 8Ω load, the required V_{opeak} is 4.0V. A minumum supply rail of 4.6V results from adding V_{opeak} and V_{od}. But 4.6V is not a standard voltage that exists in many applications and for this reason, a supply rail of 5V is designated. Extra supply voltage creates dynamic headroom that allows the HWD2161 to reproduce peaks in excess of 1Wwithout clipping the signal. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 4.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

$$R_f/R_i = A_{VD} / 2 \quad (5)$$

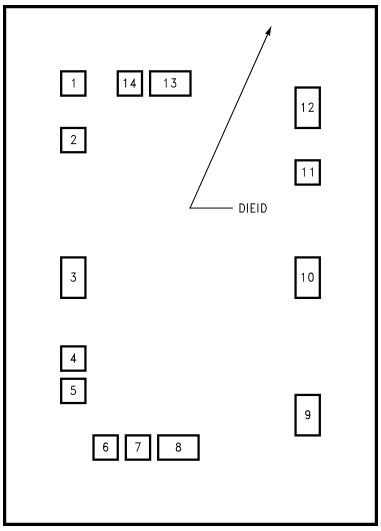
From equation 4, the minimum A_{vd} is 2.83: A_{vd} = 3

Since the desired input impedance was 20kΩ, and with a A_{vd} of 3, a ratio of 1:1.5 of R_f to R_i results in an allocation of R_i = 20kΩ, R_f = 30kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of –3dB frequency points. Five times away from a –3db point is 0.17dB down from passband response which is better than the required ±0.25dB specified. This fact results in a low and high frequency pole of 20Hz and 100kHz respectively. As stated in the **External Components** section, R_i in conjunction with C_i create a highpass filter.

$C_i \geq 1 / (2\pi * 20k\Omega * 20Hz) = 0.397\mu F$; use 0.39µF.

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the differential gain, A_{vd}. With a A_{vd} = 2 and f_H = 100kHz, the resulting GBWP = 100kHz which is much smaller than the HWD2161 GBWP of 4MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the HWD2161 can still be used without running into bandwidth problems.

HWD2161 MDA MWA
1.1W Audio Power Amplifier with Shutdown Mode



Die Layout (B - Step)

DIE/WAFER CHARACTERISTICS

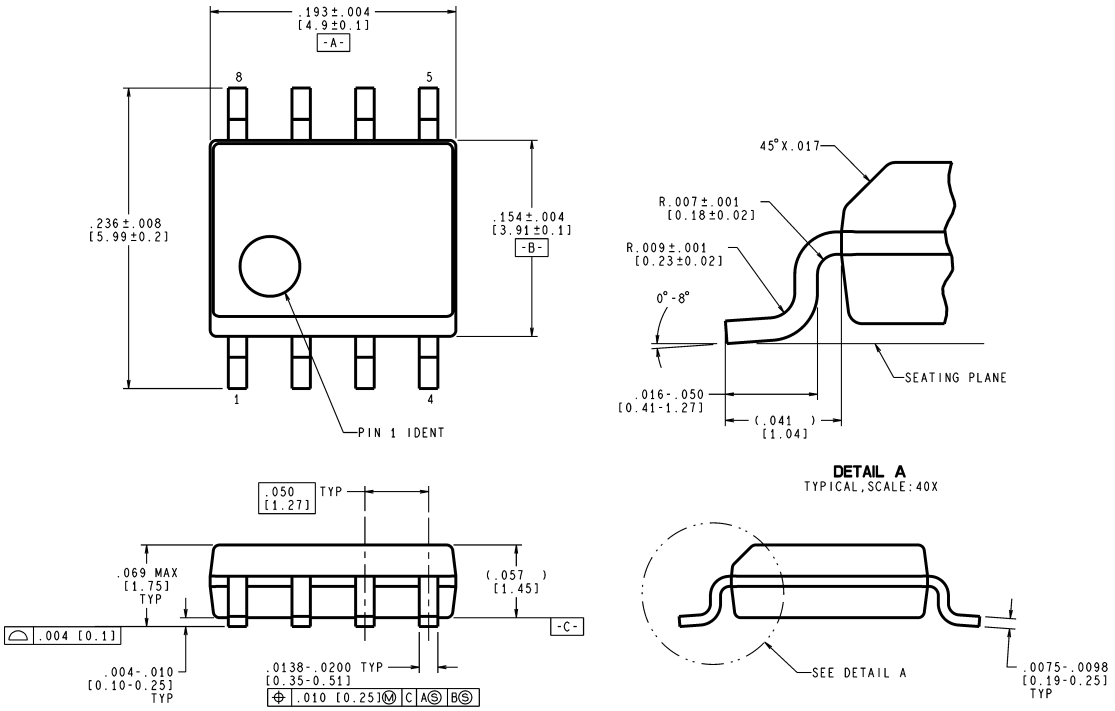
Fabrication Attributes		**General Die Information**	
Physical Die Identification	HWD2161B	Bond Pad Opening Size (min)	83µm x 83µm
Die Step	B	Bond Pad Metalization	ALUMINUM
Physical Attributes		Passivation	VOM NITRIDE
Wafer Diameter	150mm	Back Side Metal	BARE BACK
Dise Size (Drawn)	1372µm x 2032µm 54.0mils x 80.0mils	Back Side Connection	GND
Thickness	406µm Nominal		
Min Pitch	108µm Nominal		

Special Assembly Requirements:
Note: Actual die size is rounded to the nearest micron.

Die Bond Pad Coordinate Locations (B - Step)						
(Referenced to die center, coordinates in µm) NC = No Connection, N.U. = Not Used						
SIGNAL NAME	PAD# NUMBER	X/Y COORDINATES		PAD SIZE		
		X	Y	X		Y
SHUTDOWN	1	-425	710	83	x	83
BYPASS	2	-445	499	83	x	83
NC	3	-445	-34	83	x	170
NC	4	-445	-383	83	x	83
INPUT +	5	-445	-492	83	x	83
INPUT -	6	-352	-710	83	x	83
GND	7	-243	-710	83	x	83
Vo1	8	-91	-710	170	x	83
GND	9	445	-574	83	x	170
VDD	10	445	-2	83	x	170
NC	11	445	387	83	x	83
GND	12	445	633	83	x	170
Vo2	13	-63	710	170	x	83
GND	14	-215	710	83	x	83

Physical Dimensions inches (millimeters)

unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

M08A (Rev J)

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