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THE CORTEX-A8 MICROPROCESSOR

The Need

Next-generation digital entertainment and mobile communications devices are driving the need for flexible high-performance processing solutions that can meet the needs of the low-power, cost sensitive markets. Smart phones are becoming the center of your life, combining entertainment, gaming, internet services and seamless connectivity to digital entertainment devices. In a competitive and changing marketplace where digital entertainment and communications devices are converging, the need for a high-performance processor that can meet both the demanding performance requirements of leading-edge consumer entertainment devices and the tight power requirements for advanced mobile products is clear.

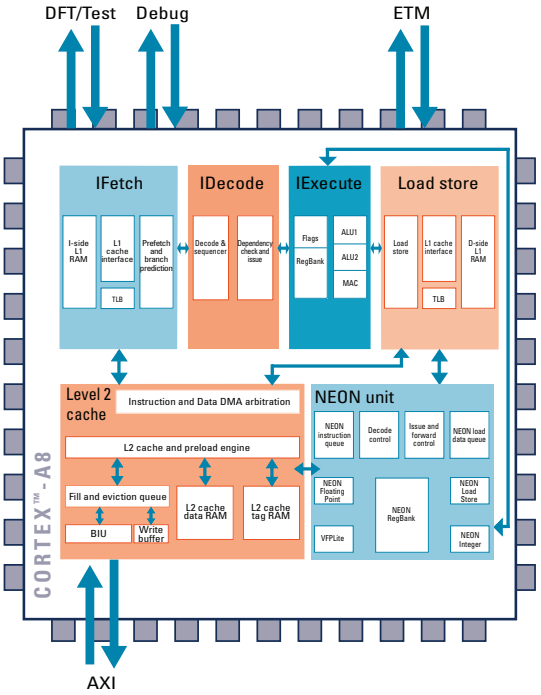
The Solution

The Cortex™-A8 processor is the highest performance, most power-efficient processor ever developed by ARM. With the ability to scale in speed from 600MHz to greater than 1GHz, the Cortex-A8 processor can meet the requirements for power optimized mobile devices with a power budget of less than 300mW and for performance optimized consumer applications requiring 2000 Dhrystone MIPS. The Cortex-A8 processor is ARM's first superscalar processor featuring NEON™ technology for multimedia and signal processing, Jazelle®-RCT (Realtime Compilation Target) technology for efficient support of ahead-of-time and just-in-time compilation of Java and other bytecode languages and Thumb®-2 technology for enhanced code density and performance. The Cortex-A8 processor also supports TrustZone™ technology for security and the AMBA 3 AXI bus, making it the next natural step up in performance for next-generation applications.

What enables it

The ARM Cortex-A8 processor's sophisticated pipeline architecture is based on dual, symmetric, in-order issue, 13-stage pipelines with advanced dynamic branch prediction and static scheduling achieving 2.0 DMIPS/MHz.

NEON media engine operates as a data processing engine attached to the end of the main processor pipeline and is able to process demanding applications such as VGA H.264 30fps video decode with a clock frequency as low as 400MHz. Both the main pipeline and the NEON engine are supported directly by integrated high-performance Level 1 and Level 2 caches that work together to minimize access latency, minimize external bus traffic, and support high bandwidth data streaming to NEON media engine. The Cortex-A8 processor's



industry-leading performance and power efficiency is enabled by combining advanced technology such as the ARM® Artisan® AdvantageHS library with enhanced design flows supporting pure synthesis, as well as structured, and custom design.

Easy to use

The Cortex-A8 processor, supported by ARM's complete ecosystem of technology; makes the Cortex-A8 processor easy to use in complex systems. Innovative new products supporting the Cortex-A8 processor include: RealView® SoC Designer (which provides cycle accurate ESL models for architectural exploration), System Generator (which provides fast instruction accurate simulation models for software development), , RealView Development Suite 3.1 with optional Vectorizing Compiler, AMBA® Designer interconnect design tool, CoreSight™ debug and trace, RealView Hardware Platforms providing implementations of Cortex-A8 on FPGA for evaluation of the technology and early software development and SoC prototyping. and ARM Artisan AdvantageHS libraries and RAMs.

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Feature	Benefit
ARMv7 architecture featuring: NEON, Jazelle-RCT, Thumb-2, TrustZone technologies and the AMBA 3 AXI system bus	Combines the key architecture features to enable a flexible high-performance, low-power architecture and widespread support from operating system and applications software.
High-Performance Superscalar Pipeline	Dual-issue, in-order execution pipeline hardware works in conjunction with a power optimized load store pipeline to deliver 2.0 DMIPS/MHz for power sensitive applications.
Dynamic Branch Prediction	Dynamic prediction enabled by branch target and global history buffers achieve 95% accuracy across industry benchmarks. Replay mechanism minimizes mispredict penalty.
NEON Media Engine	Separate SIMD execution pipeline and register file with shared access to L1 and L2 memory provides flexible media acceleration and system wide design simplification.
Optimized Level 1 Caches	Performance and power optimized L1 caches combine minimal access latency with hash way determination to maximize performance and minimize power consumption.
Integrated Level 2 Cache	An optional integrated, size configurable (128K - 1M) L2 cache provides optimal access to larger data sets; supports data streaming for NEON applications, and minimizes external bus traffic.
Thumb-2 Technology	Thumb-2 architecture delivers a 30% reduction in code size while maintaining almost the same performance of 32-bit ARM code.
TrustZone Technology	Ensures reliable implementation of security applications ranging from digital rights management to electronic payment. Broad support from technology and industry partners.
Jazelle-RCT Technology	Provides up to 3x reduction on code size for just in time and ahead of time compilation of bytecode languages. Benefits a wide range of emerging languages. Broad industry adoption.
64/128-bit Configurable AXI Bus	High bandwidth, configurable 64 or 128-bit data bus with dedicated read, write, and address channels provides for up to 23 outstanding transactions with out-of-order completion.
High Frequency Operation	Capable of 1GHz operation in performance optimized 90nm and 65nm implementations. Optional advanced implementation style supported by reference structured netlists.
Low Power Operation	Low power design optimizations, ARM Artisan AdvantageHS Libraries, and IEM technology enables less then 300mW operation on low-power 65nm process technology.

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