11. High-Speed Differential Interfaces in Cyclone II Devices

CII51011-2.2

Introduction

From high-speed backplane applications to high-end switch boxes, low-voltage differential signaling (LVDS) is the technology of choice. LVDS is a low-voltage differential signaling standard, allowing higher noise immunity than single-ended I/O technologies. Its low-voltage swing allows for high-speed data transfers, low power consumption, and reduced electromagnetic interference (EMI). LVDS I/O signaling is a data interface standard defined in the TIA/EIA-644 and IEEE Std. 1596.3 specifications.

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced EMI. National Semiconductor Corporation and Texas Instruments introduced the RSDS and mini-LVDS specifications, respectively. Currently, many designers use these specifications for flat panel display links between the controller and the drivers that drive display column drivers. Cyclone® II devices support the RSDS and mini-LVDS I/O standards at speeds up to 311 megabits per second (Mbps) at the transmitter.

Altera® Cyclone II devices can transmit and receive data through LVDS signals at a data rate of up to 640 Mbps and 805 Mbps, respectively. For the LVDS transmitter and receiver, the Cyclone II device's input and output pins support serialization and deserialization through internal logic.

This chapter describes how to use Cyclone II I/O pins for differential signaling and contains the following topics:

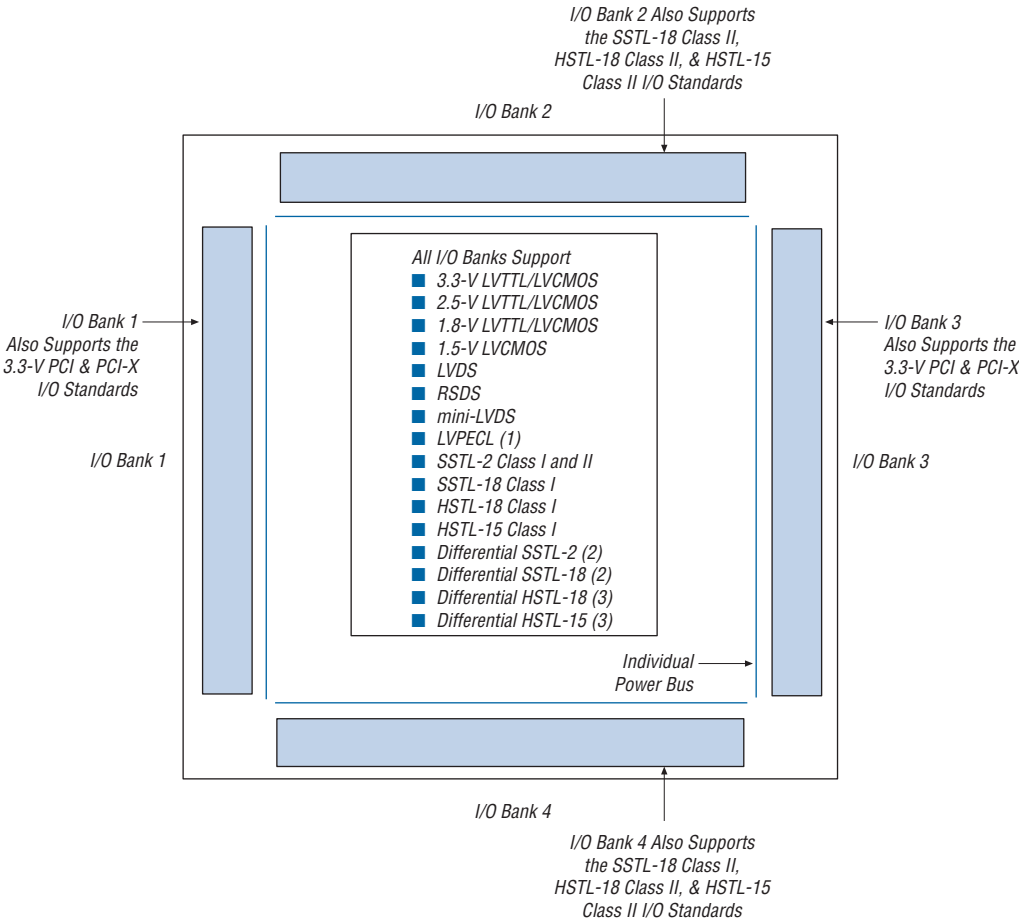
- Cyclone II high-speed I/O banks
- Cyclone II high-speed I/O interface
- LVDS, RSDS, mini-LVDS, LVPECL, differential HSTL, and differential SSTL I/O standards support in Cyclone II devices
- High-speed I/O timing in Cyclone II devices
- Design guidelines

Cyclone II High-Speed I/O Banks

Cyclone II device I/O banks are shown in Figures 11–1 and 11–2. The EP2C5 and EP2C8 devices offer four I/O banks and EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices offer eight I/O banks. A subset of

pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. Cyclone II pin tables list the pins that support the high-speed I/O interface.

Figure 11–1. I/O Banks in EP2C5 & EP2C8 Devices



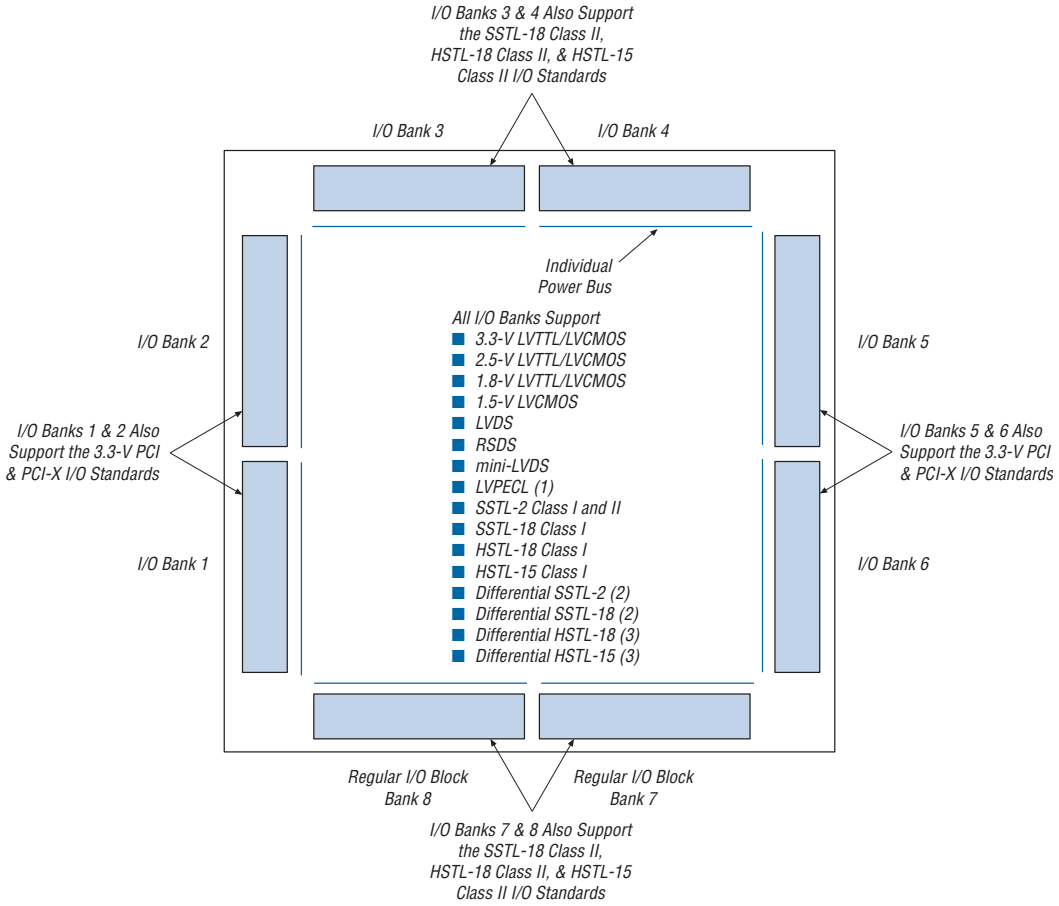
Notes to Figure 11–1:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(2) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(3) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

Figure 11–2. I/O Banks in EP2C15, EP2C20, EP2C35, EP2C50 & EP2C70 Devices



Notes to Figure 11–2:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(2) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(3) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

Cyclone II High-Speed I/O Interface

Cyclone II devices provide a multi-protocol interface that allows communication between a variety of I/O standards, including LVDS, LVPECL, RSDS, mini-LVDS, differential HSTL, and differential SSTL. This feature makes the Cyclone II device family ideal for applications that require multiple I/O standards, such as protocol translation.

You can use I/O pins and internal logic to implement a high-speed I/O receiver and transmitter in Cyclone II devices. Cyclone II devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal global phase-locked loops (PLLs), and I/O cells are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

I/O Standards Support

This section provides information on the I/O standards that Cyclone II devices support.

LVDS Standard Support in Cyclone II Devices

The LVDS I/O standard is a high-speed, low-voltage swing, low power, and general purpose I/O interface standard. The Cyclone II device meets the ANSI/TIA/EIA-644 standard.

I/O banks on all four sides of the Cyclone II device support LVDS channels. See the pin tables on the Altera web site for the number of LVDS channels supported throughout different family members. Cyclone II LVDS receivers (input) support a data rate of up to 805 Mbps while LVDS transmitters (output) support up to 640 Mbps. The maximum internal clock frequency for a receiver and for a transmitter is 402.5 MHz. The maximum input data rate of 805 Mbps and the maximum output data rate of 640 Mbps is only achieved when DDIO registers are used. The LVDS standard does not require an input reference voltage; however, it does require a 100-Ω termination resistor between the two signals at the input buffer.

For LVDS data rates in Cyclone II devices with different speed grades, see the *DC Characteristics & Timing Specifications* chapter of the *Cyclone II Device Handbook*.

Table 11–1 shows LVDS I/O specifications.

Table 11–1. LVDS I/O Specifications (Part 1 of 2) *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCINT}	Supply voltage		1.15	1.2	1.25	V
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		600	mV
ΔV_{OD}	Change in V_{OD} between H and L	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V

Table 11–1. LVDS I/O Specifications (Part 2 of 2) *Note (1)*

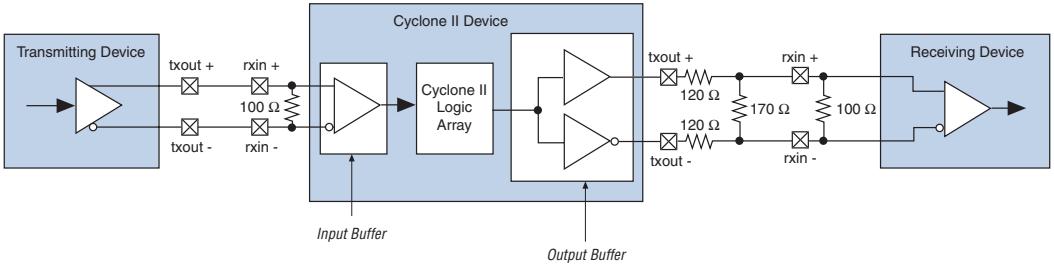
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ID}	Input differential voltage (single-ended)		0.1		0.65	V
V_{ICM}	Input common mode voltage		0.1		2.0	V
ΔV_{OS}	Change in V_{OS} between H and L	R_L = 100 Ω			50	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Note to Table 11–1:
(1) The specifications apply at the resistor network output.

LVDS Receiver & Transmitter

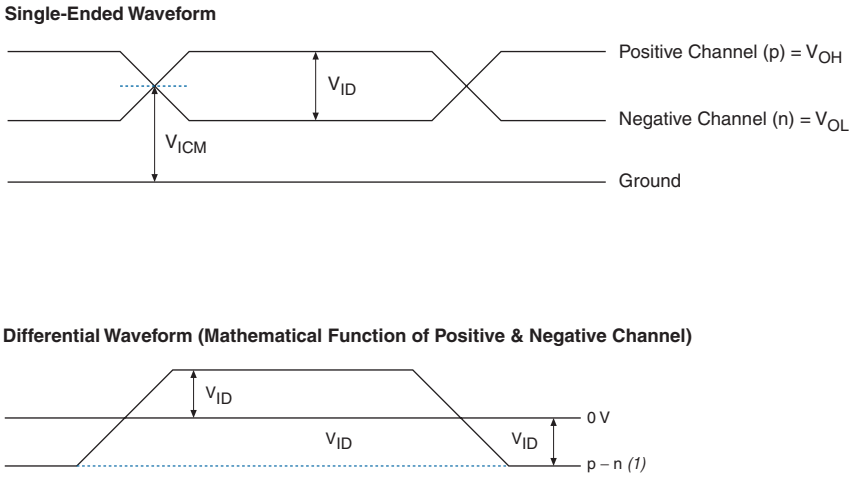
Figure 11–3 shows a simple point-to-point LVDS application where the source of the data is an LVDS transmitter. These LVDS signals are typically transmitted over a pair of printed circuit board (PCB) traces, but a combination of a PCB trace, connectors, and cables is a common application setup.

Figure 11–3. Typical LVDS Application



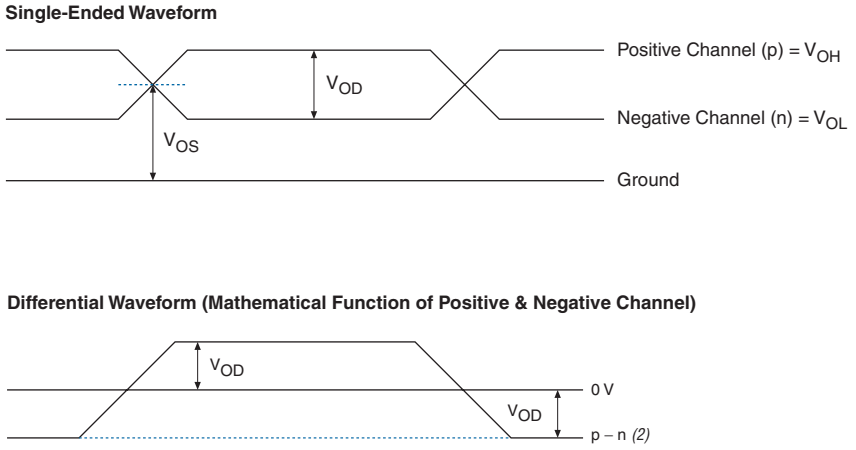
Figures 11–4 and 11–5 show the signaling levels for LVDS receiver inputs and transmitter outputs, respectively.

Figure 11–4. Receiver Input Waveforms for the LVDS Differential I/O Standard



Note to Figure 11–4:
(1) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 11–5. Transmitter Output Waveform for the LVDS Differential I/O Standard *Note (2)*



Notes to Figure 11–5:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

RSDS I/O Standard Support in Cyclone II Devices

The RSDS specification is used in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the National Semiconductor Corporation RSDS Interface Specification and support the RSDS output standard. Table 11–2 shows the RSDS electrical characteristics for Cyclone II devices.

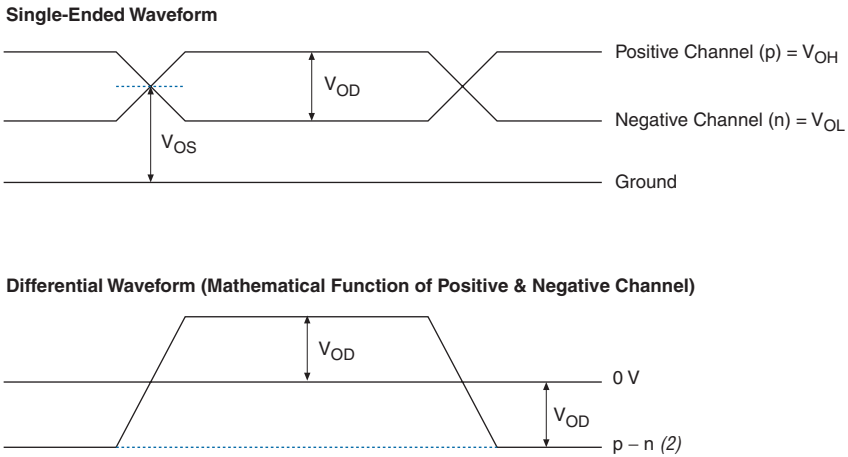
Table 11–2. RSDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	100		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
T_r/T_f	Transition time	20% to 80%		500		ps

Notes to Table 11–2:
(1) The specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

Figure 11–6 shows the RSDS transmitter output signal waveforms.

Figure 11–6. Transmitter Output Signal Level Waveforms for RSDS *Note (1)*

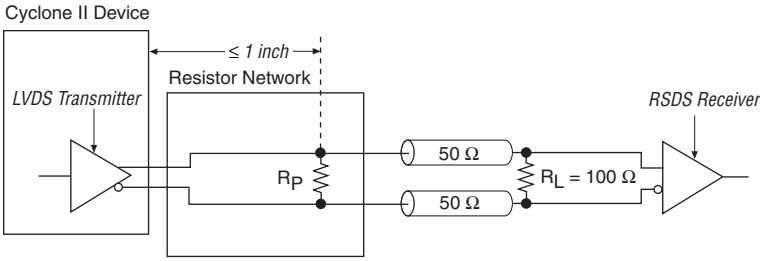


Notes to Figure 11–6:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Designing with RSDS

Cyclone II devices support the RSDS output standard using the LVDS I/O buffer types. For transmitters, the LVDS output buffer can be used with the external resistor network shown in Figure 11–7.

Figure 11–7. RSDS Resistor Network *Note (1)*



Note to Figure 11–7:
(1) R_S = 120 Ω and R_P = 170 Ω

For more information on the RSDS I/O standard, see the RSDS specification from the National Semiconductor web site **(www.national.com)**.

A resistor network is required to attenuate the LVDS output voltage swing to meet the RSDS specifications. The resistor network values can be modified to reduce power or improve the noise margin. The resistor values chosen should satisfy the following equation:

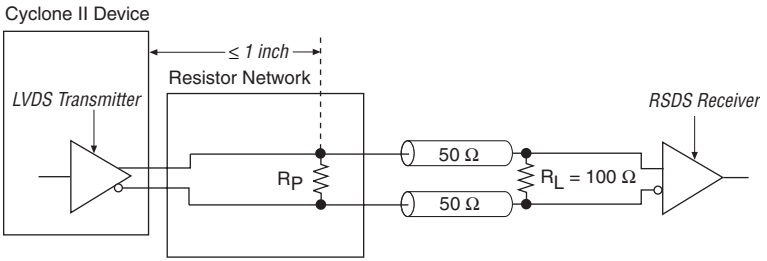
$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\,\Omega$$

Additional simulations using the IBIS models should be performed to validate that custom resistor values meet the RSDS requirements.

Single Resistor RSDS Solution

The external single resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. To transmit the RSDS signal, an external resistor (R_P) is connected in parallel between the two adjacent I/O pins on the board as shown in Figure 11–8. The recommended value of the resistor R_P is 100 Ω

Figure 11–8. RSDS Single Resistor Network *Note (1)*



Note to Figure 11–8:
(1) R_p = 100 Ω

RSDS Software Support

When designing for the RSDS I/O standard, assign the RSDS I/O standard to the I/O pins intended for RSDS in the Quartus® II software. Contact Altera Applications for reference designs.

mini-LVDS Standard Support in Cyclone II Devices

The mini-LVDS specification defines its use in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the Texas Instruments mini-LVDS Interface Specification and support the mini-LVDS output standard. Table 11–3 shows the mini-LVDS electrical characteristics for Cyclone II devices.

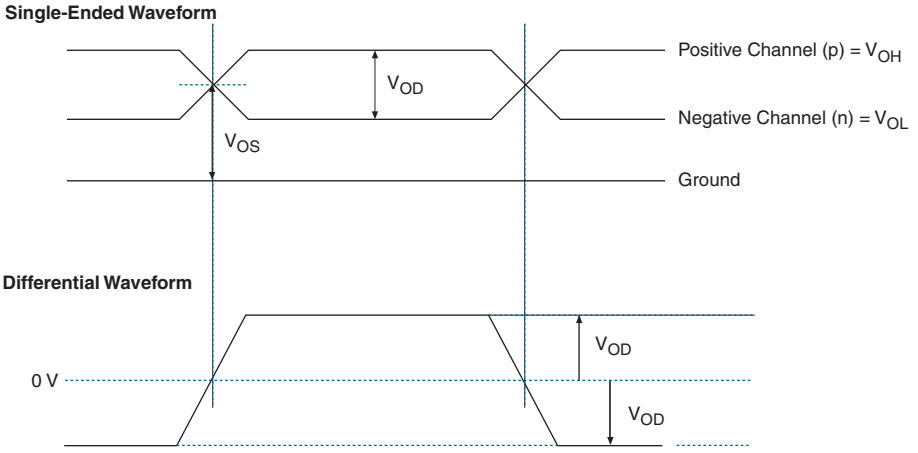
Table 11–3. mini-LVDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	300		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1125	1250	1375	mV
T_r / T_f	Transition time	20% to 80%			500	ps

Notes to Table 11–3:
(1) The V_{OD} specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

Figure 11–9 shows the mini-LVDS receiver and transmitter signal waveforms.

Figure 11–9. Transmitter Output Signal Level Waveforms for mini-LVDS *Note (1)*

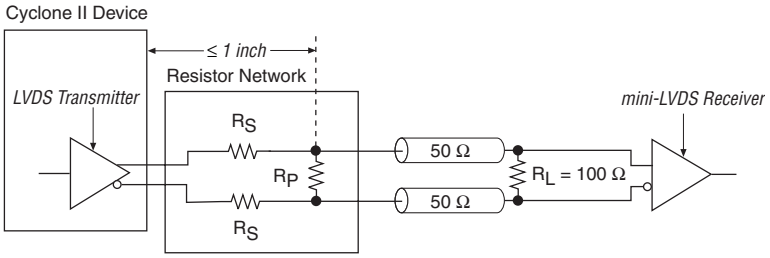


Note to Figure 11–9:
(1) The V_{OD} specifications apply at the resistor network output.

Designing with mini-LVDS

Similar to RSDS, Cyclone II devices support the mini-LVDS output standard using the LVDS I/O buffer types. For transmitters, the LVDS output buffer can be used with the external resistor network shown in Figure 11–10. The resistor values chosen should satisfy the equation on page 11-8.

Figure 11–10. mini-LVDS Resistor Network



Note to Figure 11–10:
(1) R_S = 120 Ω and R_P = 170 Ω

mini-LVDS Software Support

When designing for the mini-LVDS I/O standard, assign the mini-LVDS I/O standard to the I/O pins intended for mini-LVDS in the Quartus II software. Contact Altera Applications for reference designs.

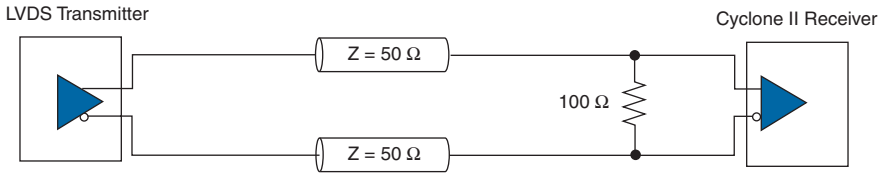
LVPECL Support in Cyclone II

The LVPECL I/O standard is a differential interface standard requiring a 3.3-V V_{CCIO} and is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS. However, LVPECL has a larger differential output voltage swing than LVDS. Cyclone II devices support the LVPECL input standard at the clock input pins only. Table 11–4 shows the LVPECL electrical characteristics for Cyclone II devices. Figure 11–11 shows the LVPECL I/O interface.

Table 11–4. LVPECL Electrical Characteristics for Cyclone II Devices

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		3.135	3.3	3.465	V
V_{IH}	Input high voltage		2,100		2,880	mV
V_{IL}	Input low voltage		0		2,200	mV
V_{ID}	Differential input voltage	Peak to peak	100	600	950	mV

Figure 11–11. LVPECL I/O Interface



Differential SSTL Support in Cyclone II Devices

The differential SSTL I/O standard is a memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. The differential SSTL I/O standard is similar to voltage referenced SSTL and requires two differential inputs with an external termination voltage (V_{TT}) of 0.5 × V_{CCIO} to which termination resistors are connected. A 2.5-V output source voltage is required for differential SSTL-2, while a 1.8-V output source voltage is required for differential SSTL-18. The differential SSTL output standard is only supported at PLLCLKOUT pins using two single-ended SSTL output buffers programmed to have opposite polarity.

The differential SSTL input standard is supported at the global clock (GCLK) pins only, treating differential inputs as two single-ended SSTL, and only decoding one of them.

For SSTL signaling characteristics, see the *DC Characteristics & Timing Specification* chapter and the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Figures 11–12 and 11–13 show the differential SSTL class I and II interfaces, respectively.

Figure 11–12. Differential SSTL Class I Interface

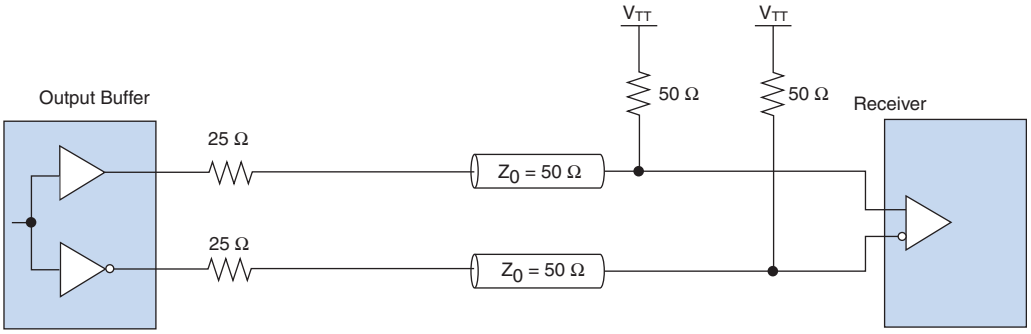
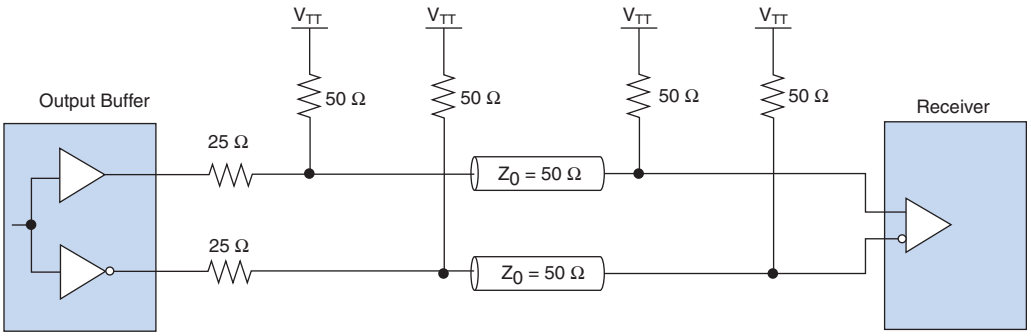


Figure 11–13. Differential SSTL Class II Interface



Differential HSTL Support in Cyclone II Devices

The differential HSTL AC and DC specifications are the same as the HSTL single-ended specifications. The differential HSTL I/O standard is available on the GCLK pins only, treating differential inputs as two single-ended HSTL, and only decoding one of them. The differential HSTL output I/O standard is only supported at the PLLCLKOUT pins using two single-ended HSTL output buffers with the second output programmed as inverted. The standard requires two differential inputs with an external termination voltage (V_{TT}) of 0.5 × V_{CCIO} to which termination resistors are connected.

For the HSTL signaling characteristics, see the *DC Characteristics & Timing Specifications* chapter and the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Figures 11–14 and 11–15 show differential HSTL class I and II interfaces, respectively.

Figure 11–14. Differential HSTL Class I Interface

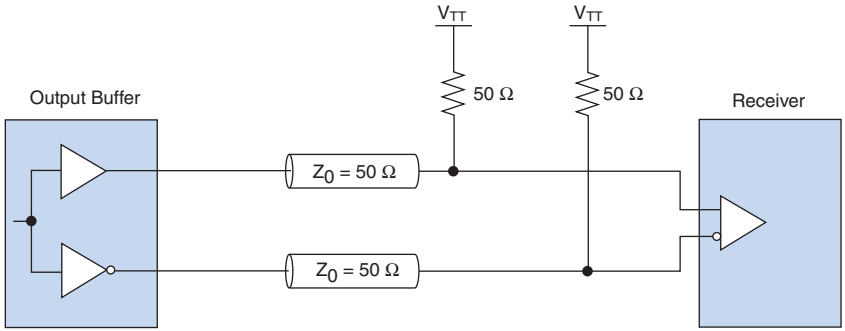
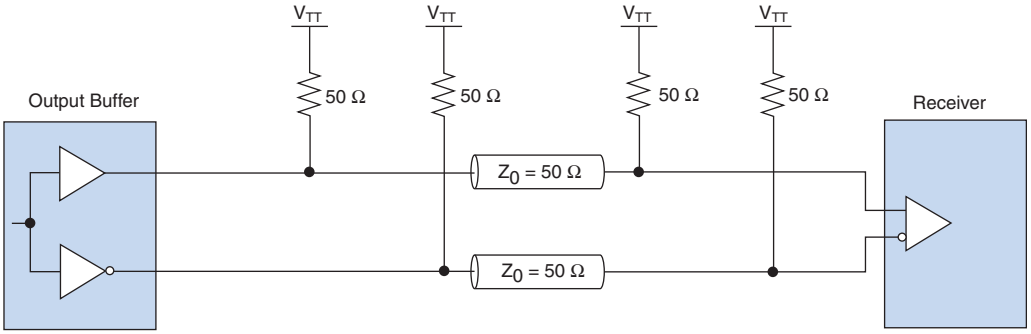


Figure 11–15. Differential HSTL Class II Interface



High-Speed I/O Timing in Cyclone II Devices

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Cyclone II devices. LVDS, LVPECL, RSDS, and mini-LVDS I/O standards enable high-speed data transmission. Timing for these high-speed signals is based on skew between the data and the clock signals.

High-speed differential data transmission requires timing parameters provided by integrated circuit (IC) vendors and requires consideration of board skew, cable skew, and clock jitter. This section provides details on high-speed I/O standards timing parameters in Cyclone II devices.

Table 11–5 defines the parameters of the timing diagram shown in Figure 11–16. Figure 11–17 shows the Cyclone II high-speed I/O timing budget.

Table 11–5. High-Speed I/O Timing Definitions

Parameter	Symbol	Description
Transmitter channel-to-channel skew *(1)*	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window. $T_{SW} = T_{SU} + T_{hd}$ + PLL jitter.
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: RSKM = (TUI – SW – TCCS) / 2.
Input jitter tolerance (peak-to-peak)		Allowed input jitter on the input clock to the PLL that is tolerable while maintaining PLL lock.
Output jitter (peak-to-peak)		Peak-to-peak output jitter from the PLL.

Note to Table 11–5:

(1) The TCCS specification applies to the entire bank of LVDS as long as the SERDES logic are placed within the LAB adjacent to the output pins.

Figure 11–16. High-Speed I/O Timing Diagram

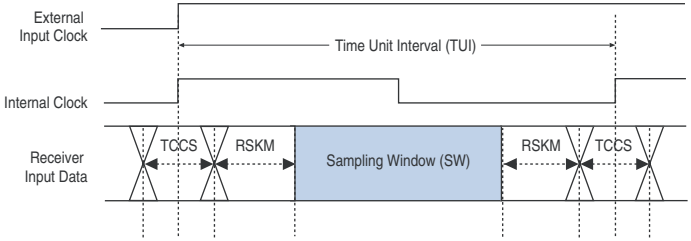
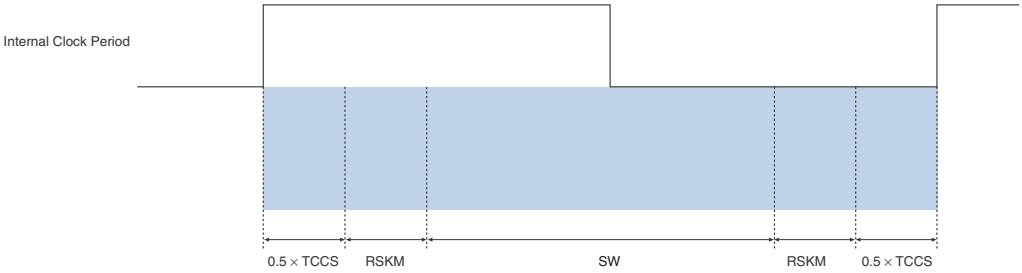


Figure 11–17. Cyclone II High-Speed I/O Timing Budget *Note (1)*



Note to Figure 11–17:
(1) The equation for the high-speed I/O timing budget is: Period = 0.5/TCCS + RSKM + SW + RSKM + 0.5/TCCS.

Design Guidelines

This section provides guidelines for designing with Cyclone II devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pins in relation to differential pads.

See the guidelines in the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook* for placing single-ended pads with respect to differential pads in Cyclone II devices.

Board Design Considerations

This section explains how to get the optimal performance from the Cyclone II I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. The critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques must be considered to get the best performance from the IC. The Cyclone II device generates signals that travel over the media at frequencies as high as 805 Mbps. Use the following general guidelines for improved signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.

- Maintain equal distance between traces in LVDS pairs, as much as possible. Routing the pair of traces close to each other maximizes the common-mode rejection ratio (CMRR).
- Longer traces have more inductance and capacitance. These traces should be as short as possible to limit signal integrity issues.
- Place termination resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° or 45° corners.
- Use high-performance connectors.
- Design backplane and card traces so that trace impedance matches the connector's and/or the termination's impedance.
- Keep equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths result in misplaced crossing points and decrease system margins as the channel-to-channel skew (TCCS) value increases.
- Limit vias because they cause discontinuities.
- Use the common bypass capacitor values such as 0.001, 0.01, and 0.1 µF to decouple the high-speed PLL power and ground planes.
- Keep switching transistor-to-transistor logic (TTL) signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Analyze system-level signals.

For PCB layout guidelines, see *AN 224: High-Speed Board Layout Guidelines*.

Conclusion

Cyclone II differential I/O capabilities enable you to keep pace with increasing design complexity. Support for I/O standards including LVDS, LVPECL, RSDS, mini-LVDS, differential SSTL and differential HSTL allows Cyclone II devices to fit into a wide variety of applications. Taking advantage of these I/O capabilities and Cyclone II pricing allows you to lower your design costs while remaining on the cutting edge of technology.

Document Revision History

Table 11–6 shows the revision history for this document.

Table 11–6. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	• Added document revision history. • Added *Note (1)* to Table 11–1. • Updated Figure 11–5 and added *Note (1)* • Added *Note (1)* to Table 11–2. • Updated Figure 11–6 and added *Note (1)* • Added *Note (1)* to Table 11–3. • Added *Note (1)* to Figure 11–9.	• Added information stating LVDS/RSDS/mini-LVDS I/O standards specifications apply at the external resistors network output.
November 2005 v2.1	• Updated Table 11–2. • Updated Figures 11–7 through 11–9. • Added Resistor Network Solution for RSDS. • Updated note for mini-LVDS Resistor Network table.	
July 2005 v2.0	• Updated "I/O Standards Support" section. • Updated Tables 11–1 through 11–3.	
November 2004 v1.1	• Updated Table 11–1. • Updated Figures 11–4, 11–5, 11–7, and 11–9.	
June 2004, v1.0	Added document to the Cyclone II Device Handbook.	