1. Module Features

-Bluetooth™ V1.1 or 1.2Compliant
-Transmit Power +4dBm(Class2)
-1.8V to 3.6V I/O Operation
-Full Bluetooth data rate over UART
-Dual UART Port Support
-Ultra low power consumption

ABM-450

Class2 Bluetooth Module
Production Information Data Sheet
ID : ABM-450-2CSP
Dec.2004

Rev 1.1

2. General Description

ABM-450-2CSP is a Class2 surface mountable Bluetooth™ Module for Mobile Phone applications.
It provides fully compliant Bluetooth system for data and voice communications. Physical interface to host UART can support full Bluetooth data rate 723.2k/57.6kbps. A-Law, µ-Law,13bit or 16bit linear PCM, 8k sample/sec synchronous bidirectional audio interface is available.

3. Application

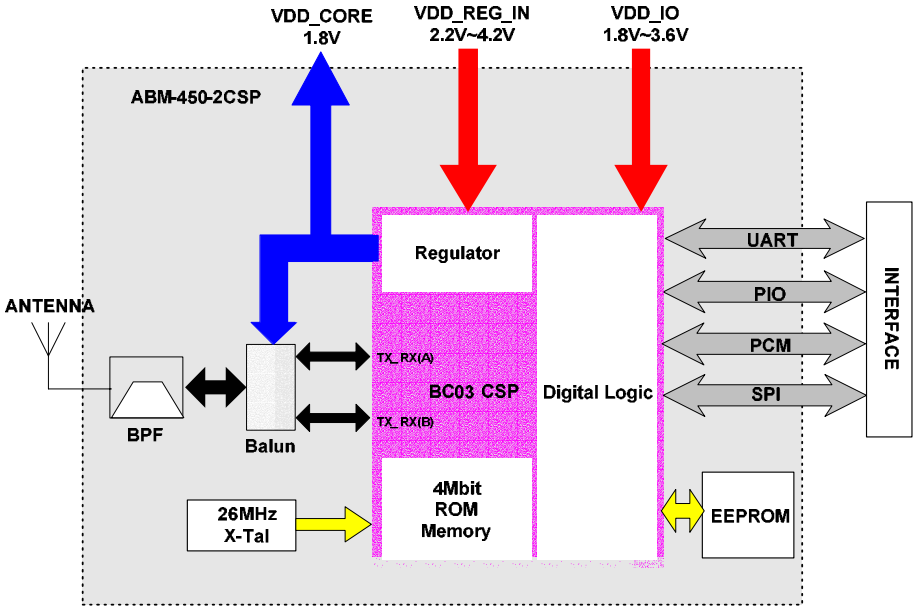
-Personal Digital Assistants (PDAs)
-Mobile Phone(CDMA, W-CDMA, GSM, GPRS)

4. Features

-Size(8 X 8 X 1.7mm)
-Class2 Support(+4dBm)
-Surface Mountable
-Support PCM interface for SCO

5. Specification

-Operating Conditions
Supply Voltage……. VDD: 1.8V ~3.6V
Temperature Range……..… -20~+70°C
-Radio Characteristics
Receiver Sensitivity … -80dBm
Transmitter Power ….. +2dBm(Typical)



6. Electrical Characteristics

Absolute Maximum Ratings			
Parameter	**Min**	**Max**	**Unit**
Storage Temperature	-40	+85	℃
Supply Voltage(VDD_IO)	1.8	3.6	DCV
Supply Voltage(VDD_REG_IN)	2.2	4.2	DCV
Supply Voltage(VDD_Core)	1.7	1.9	DCV
Other Pin Voltage	V_{ss}-0.4	V_{DD_IO}+0.4	DCV

Recommended Operating Conditions			
Parameter	**Min**	**Max**	**Unit**
Temperature	-20	+70	℃
Supply Voltage for UART	3.0	3.6	DCV

7. RF Specification

Transmitter Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Output Power	Normal/extreme test	-6	2	4	dBm
Power Density	Normal/extreme test	-	-	4	dBm
Power Control	Normal/extreme test	2dB ≤ Step size ≤ 8dB			
Frequency Range	Normal/extreme test	2400	-	2483.5	MHz
20dB Bandwidth	Normal/extreme test	-	850	1000	KHz
Adjacent channel power	±2MHz	-	-	-20	dBm
	±3MHz	-	-	-40	dBm
	±4MHz	-	-	-40	dBm
Modulation Characteristics	$\Delta F1_{avg}$	140	-	175	KHz
	$\Delta F2_{max}$	115	-	-	KHz
	$\Delta F2_{avg} / \Delta F1_{avg}$	-	-	80	%
Initial Carrier Frequency Tolerance		-5	-	5	KHz
Carrier Frequency Drift	One slot packet(DH1)	-25	-	25	KHz
	Three slot packet(DH3)	-40	-	40	KHz
	five slot packet(DH5)	-40	-	40	KHz

Transceiver Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Out-of-Band Spurious Emissions	30MHz-1GHz	-	-	-36	dBm
	1GHz-12.75GHz	-	-	-30	dBm
	1.8GHz-5.3GHz	-	-	-47	dBm
	5.1GHz-5.3GHz	-	-	-47	dBm

Receiver Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Sensitivity level	Single slot packets	-70	-80	-	dBm
Sensitivity level	Multi slot packets	-70	-	-	dBm
C/I performance	C/I co-channel	-	-	11	dB
	C/I_{1MHz} (Adjacent channel selectivity)	-	-	0	dB
	C/I_{2MHz} (2nd Adjacent channel selectivity)	-	-	-30	dB
	$C/I_{\geq 3MHz}$ (3rd Adjacent channel selectivity)	-	-	-40	dB
Blocking performance	30MHz-2000MHz	-10	-	-	dBm
	2000MHz-2400MHz	-27	-	-	dBm
	2500MHz-3000MHz	-27	-	-	dBm
	3000MHz-12.75MHz	-10	-	-	dBm
Intermodulation Performance	n=5	-39	-	-	dBm
Maximun Input Level		-20	-10	-	dBm

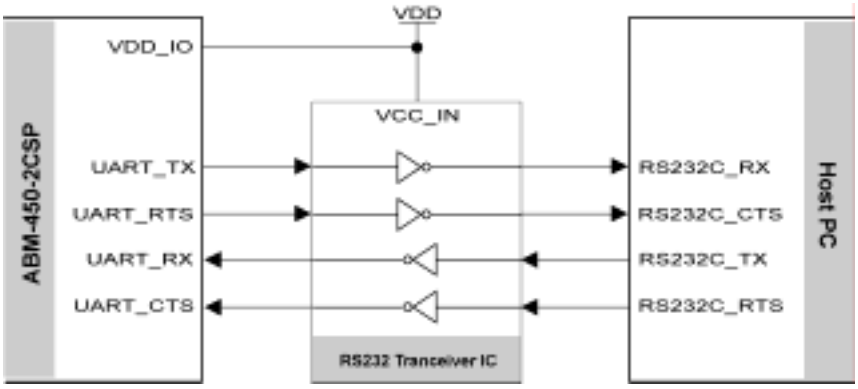
8. Pin Description

Pin No.	Pin Name	Description
1	GND	Ground
2	VDD_IO	Supply I/O Voltage 3.3V
3	PIO(5)	Programmable I/O terminal
4	PIO(4)	Programmable I/O terminal
5	SPI_MOSI	Serial Peripheral Interface data input
6	SPI_CLK	Serial Peripheral Interface clock
7	SPI_CSB	Chip select for Synchronous Serial Interface active low
8	GND	Common ground
9	SPI_MISO	Serial Peripheral Interface data output
10	RESET_IN	Module Reset Input (Active low Reset)
11	PCM_OUT	Synchronous Data output
12	PCM_SYNC	Synchronous data strobe
13	PCM_IN	Synchronous data input
14	PCM_CLK	Synchronous data clock
15	GND	Common ground
16	VDD_CORE	RF & Internal logic supply, but leave not connected when REG_IN is used
17	UART_RTS	UART request to send active low
18	UART_RX	UART data input active low
19	UART_TX	UART data output active low
20	UART_CTS	UART clear to send active low
21	VDD_REG_IN	Supply to built - in LDO for internal logic
22	GND	Ground
23	GND	Ground
24	ANT	RF input and output, connect to antenna, matching Requre
25	PIO(1)	Programmable I/O terminal
26	PIO(0)	Programmable I/O terminal
27	PIO(2)	Programmable I/O terminal
28	PIO(3)	Programmable I/O terminal
29	NC	Not Connect

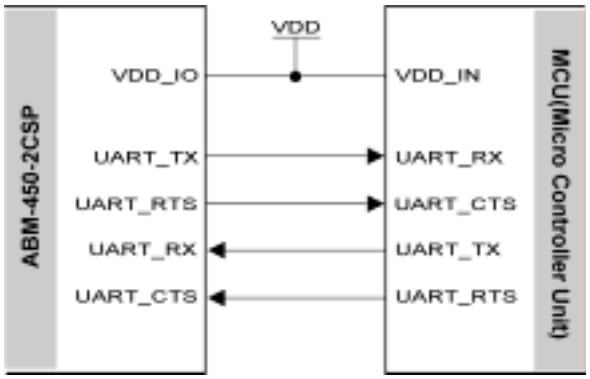
9. UART Interface

ABM-450-2CSP Universal Asynchronous Receiver and Transmitter(UART) interface provides a simple mechanism for communicating with other serial device using the RS232 standard.

When ABM-450-2CSP is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signal, UART_CTS, UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signaling levels of 0V and VDD



<UART connected to Host PC>



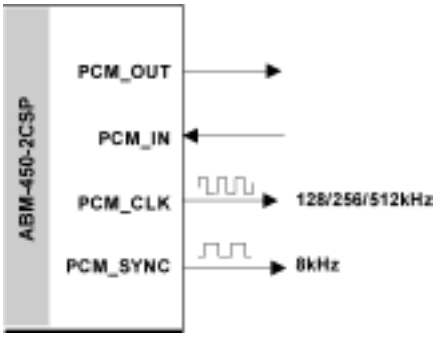
<UART connected to MCU>

10. PCM Interface

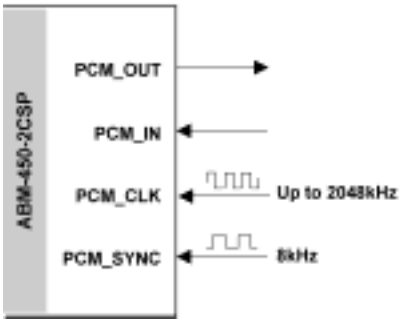
Pulse Code Modulation(PCM) is a standard method used to digitize human voice patterns for transmission over digital communication channels. Through its PCM interface, ABM-450-2CSP has hardware support for continual transmission reception of PCM data, thus reducing processor overhead for wireless application. ABM-450-2CSP offers a bi-directional digital audio interface that routes directly into the baseband layer of the Module firmware. It does not pass through the HCI protocol layer.

ABM-450-2CSP allows the data which received from a SCO connection. To be sent to external hard ware
ABM-450-2CSP can be configured as PCM interface Master generating an output clock of 128, 256, or 512kHz. When configured as PCM interface slave it can operated with input clock up to 2048kHz. ABM-450-2CSP is compatible with a variety of clock formats, including Long Frame Sync, Sort Frame sync and GCI timing environments.

It supports 13-bit or 16-bit liner, 8-bit u-law or A-law companied sample formats at 8k samples/s and can receive and transmit on any selection of the first four slots following PCM_SYNC.



< ABM-450-2CSP as PCM Interface Master>

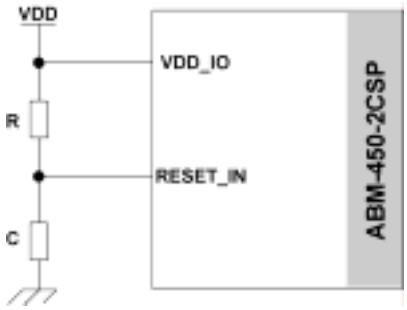


< ABM-450-2CSP as PCM Interface Slave>

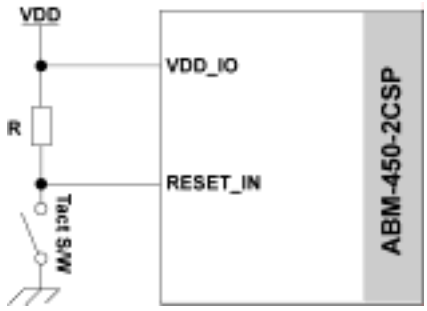
11. RESET

ABM-450-2CSP may be reset from several sources : RESET_IN pin, power on reset, a UART break character or via a software configured watchdog timer.

The RESET_IN pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET_IN being active. It is recommended that RESET_IN is applied for a period greater than 5ms.



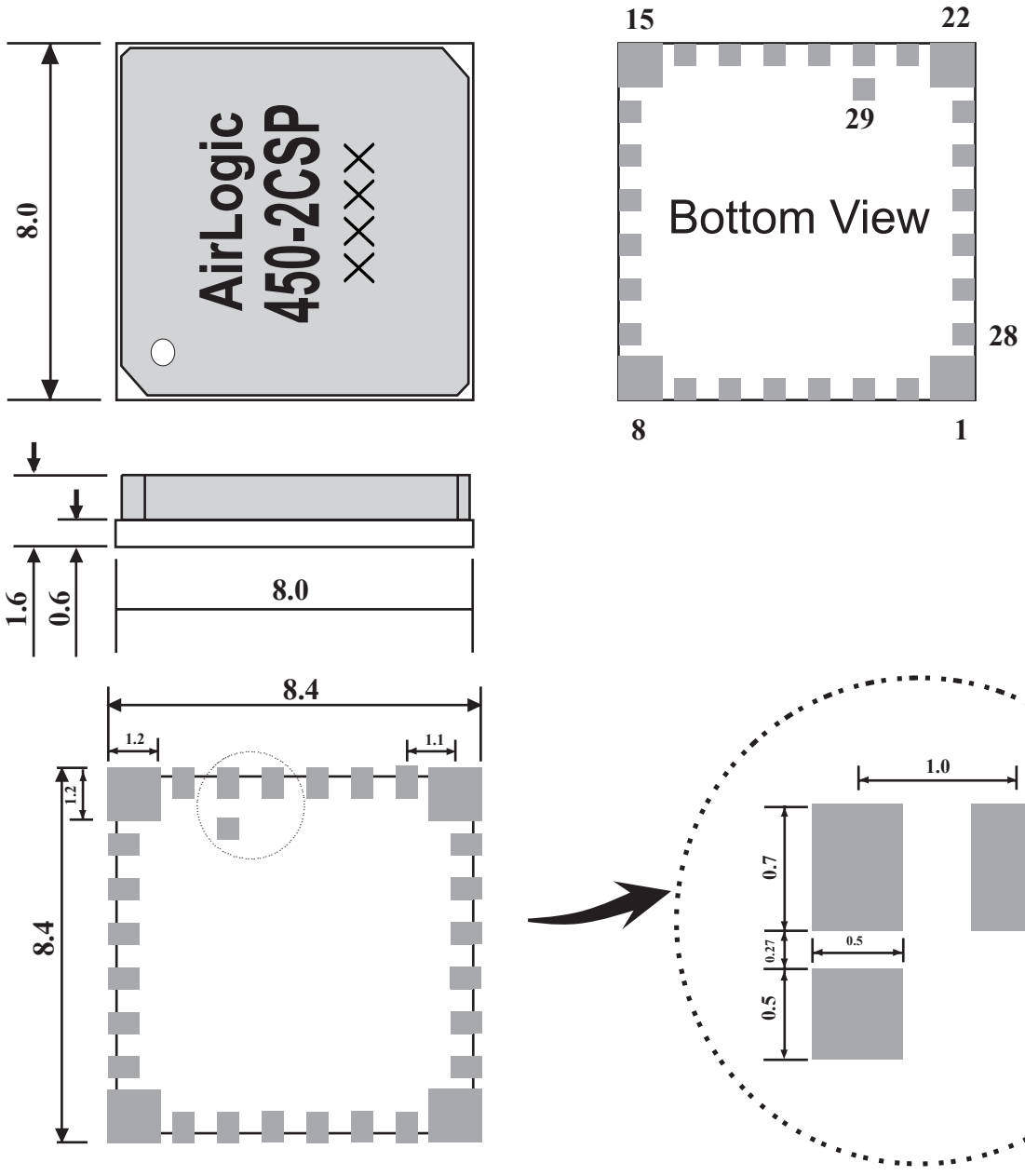
< ABM-450-2CSP as Power ON Reset>



< ABM-450-2CSP as Manual Reset>

12. Dimensions

Unit : mm



PCB Layout

Packing : Tape & Reel(MOQ : 2000EA)

13. Record of Changes

Date	Revision	Reason of Change
Oct. 2004	1.0	-First Issue

AirLogic Bluetooth Module Product Data Book

ABM-450-2CSP

Oct 2004

Rev 1.0