1.2V Drive Nch + Pch MOSFET

VT6M1

● Structure

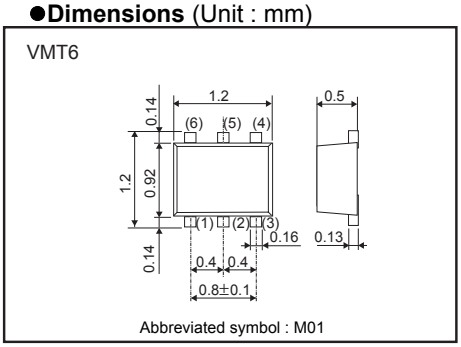
Silicon N-channel MOSFET/
Silicon P-channel MOSFET

●Features

1) Low on-resistance.
2) Small package(VMT6).
3) Low voltage drive(1.2V drive).

●Dimensions (Unit : mm)

VMT6



Abbreviated symbol : M01

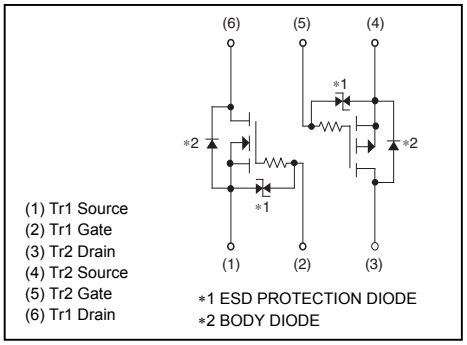
● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	T2CR
	Basic ordering unit (pieces)	8000
VT6M1		○

●Inner circuit



● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage		V_{DSS}	20	−20	V
Gate-source voltage		V_{GSS}	±8	±10	V
Drain current	Continuous	I_D	±100	±100	mA
	Pulsed	I_{DP} *1	±400	±400	mA
Power dissipation		P_D *2	0.15		W / TOTAL
			0.12		W / ELEMENT
Channel temperature		Tch	150		°C
Range of storage temperature		Tstg	−55 to +150		°C

*1 Pw≤10μs, Duty cycle≤1%

*2 Each terminal mounted on a recommended land.

● **Electrical characteristics** (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±8V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	20	-	-	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=20V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	0.3	-	1.0	V	V_{DS}=10V, I_D=100μA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	-	2.5	3.5	Ω	I_D=100mA, V_{GS}=4.5V
		-	3.0	4.2		I_D=100mA, V_{GS}=2.5V
		-	3.8	5.3		I_D=50mA, V_{GS}=1.8V
		-	4.5	9.0		I_D=20mA, V_{GS}=1.5V
		-	6.0	18.0		I_D=10mA, V_{GS}=1.2V
Forward transfer admittance	$\|Y_{fs}\|$*	180	-	-	mS	V_{DS}=10V, I_D=100mA
Input capacitance	C_{iss}	-	7.1	-	pF	V_{DS}=10V
Output capacitance	C_{oss}	-	3.3	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	1.7	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	5	-	ns	V_{DD}≒10V, I_D=50mA
Rise time	t_r *	-	4	-	ns	V_{GS}=4.5V
Turn-off delay time	$t_{d(off)}$*	-	20	-	ns	R_L=200Ω, R_G=10Ω
Fall time	t_f *	-	38	-	ns	

*Pulsed

●**Body diode characteristics** (Source-Drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	1.2	V	I_s=100mA, V_{GS}=0V

*Pulsed

● **Electrical characteristics** (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±10V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	−20	-	-	V	I_D=−1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}		-	−1	μA	V_{DS}=−20V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	−0.3	-	−1.0	V	V_{DS}=−10V, I_D=−100μA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	-	2.5	3.8	Ω	I_D=−100mA, V_{GS}=−4.5V
		-	3.4	5.1		I_D=−50mA, V_{GS}=−2.5V
		-	4.8	8.2		I_D=−20mA, V_{GS}=−1.8V
		-	6.0	13.2		I_D=−10mA, V_{GS}=−1.5V
		-	13.3	53.2		I_D=−1mA, V_{GS}=−1.2V
Forward transfer admittance	$\|Y_{fs}\|$*	120	-	-	mS	V_{DS}=−10V, I_D=−100mA
Input capacitance	C_{iss}	-	15.0	-	pF	V_{DS}=−10V
Output capacitance	C_{oss}	-	4.0	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	1.5	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	46	-	ns	V_{DD}≒ −10V, I_D=−50mA
Rise time	t_r *	-	62	-	ns	V_{GS}=−4.5V
Turn-off delay time	$t_{d(off)}$*	-	325	-	ns	R_L=200Ω, R_G=10Ω
Fall time	t_f *	-	137	-	ns	

*Pulsed

●**Body diode characteristics** (Source-Drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	−1.2	V	I_s=−100mA, V_{GS}=0V

*Pulsed

●Electrical characteristic curves

〈Tr.1(Nch)〉

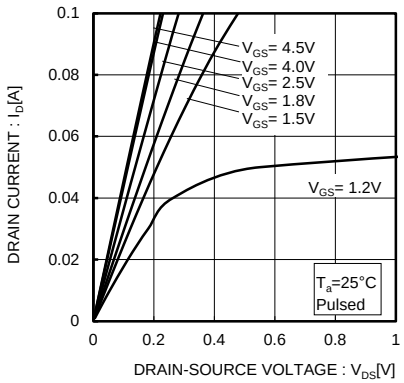


Fig.1 Typical Output Characteristics(Ⅰ)

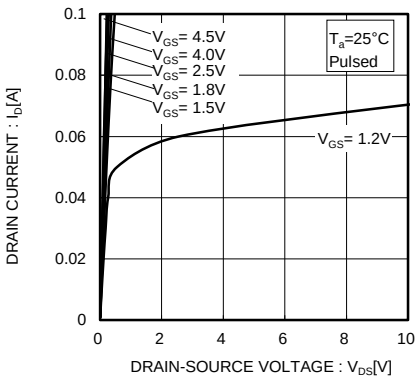


Fig.2 Typical Output Characteristics(Ⅱ)

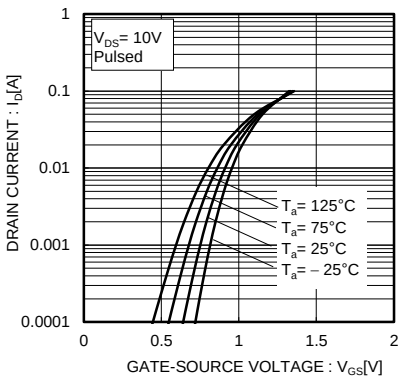


Fig.3 Typical Transfer Characteristics

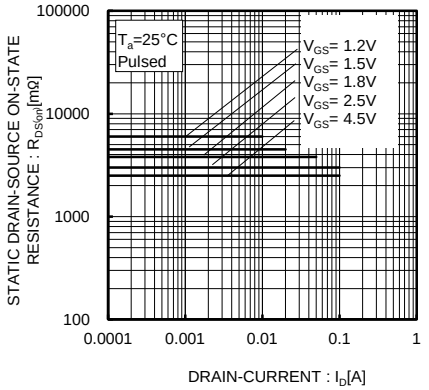


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

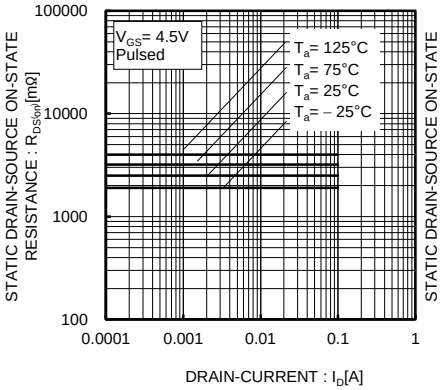


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

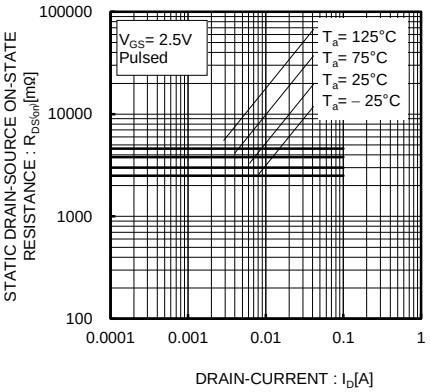


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

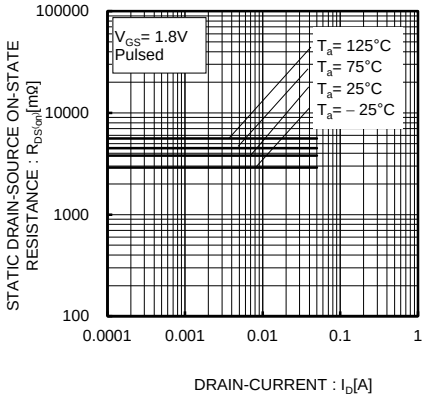


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

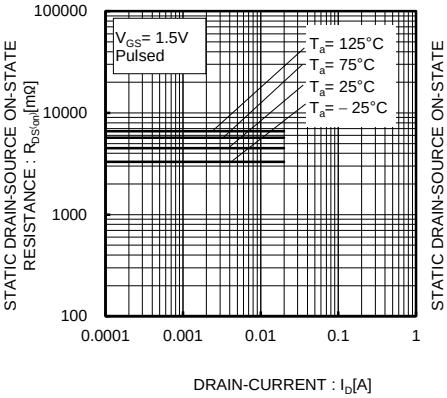


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅴ)

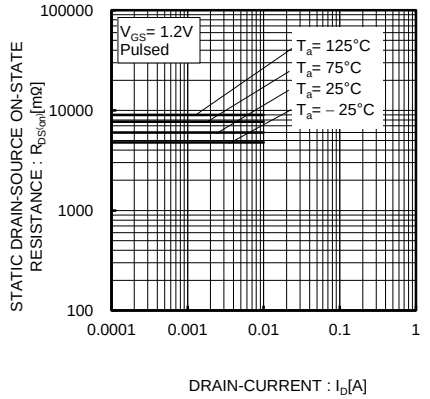


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current(Ⅵ)

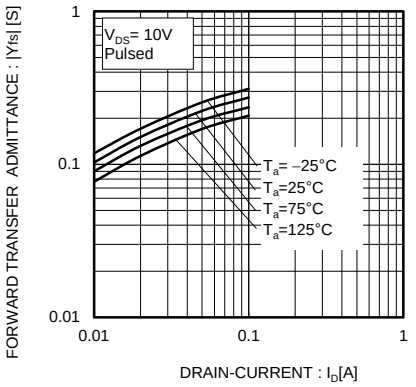


Fig.10 Forward Transfer Admittance vs. Drain Current

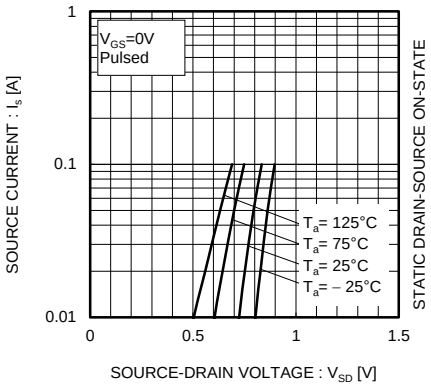


Fig.11 Reverse Drain Current vs. Sourse-Drain Voltage

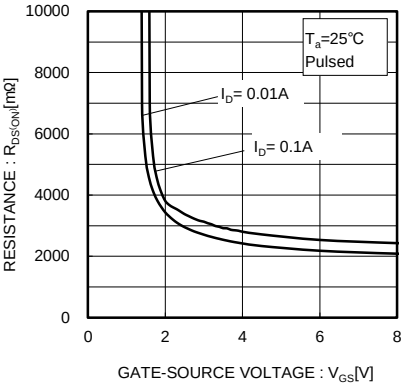


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

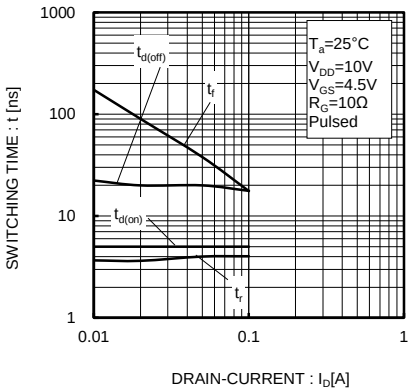


Fig.13 Switching Characteristics

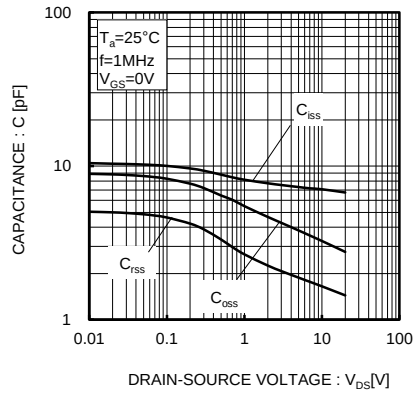


Fig.14 Typical Capacitance vs. Drain-Source Voltage

〈Tr.2(Pch)〉

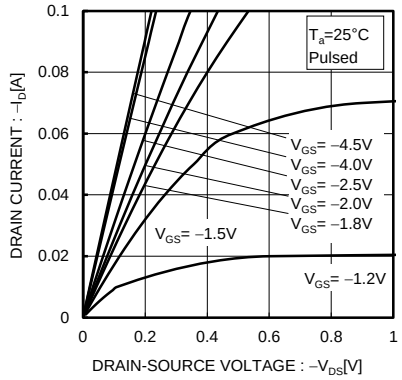


Fig.1 Typical output characteristics(Ⅰ)

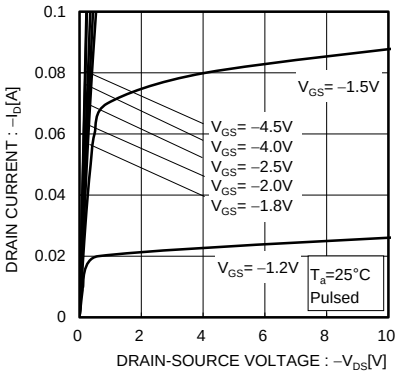


Fig.2 Typical output characteristics(Ⅱ)

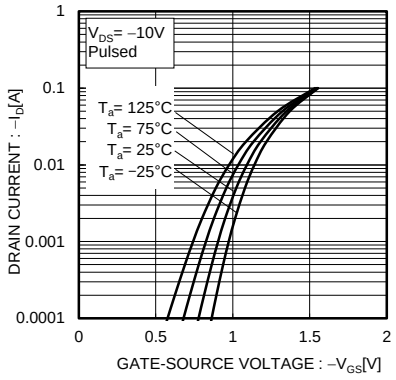


Fig.3 Typical Transfer Characteristics

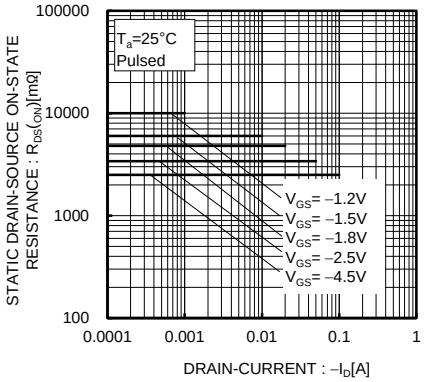


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

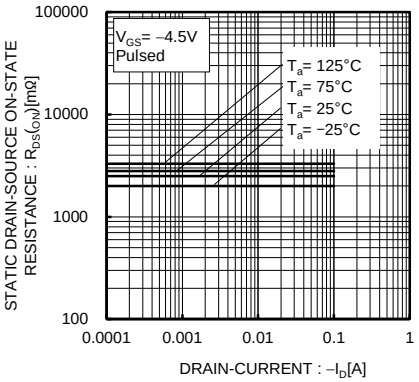


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

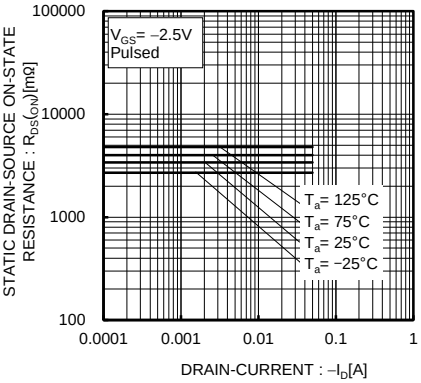


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

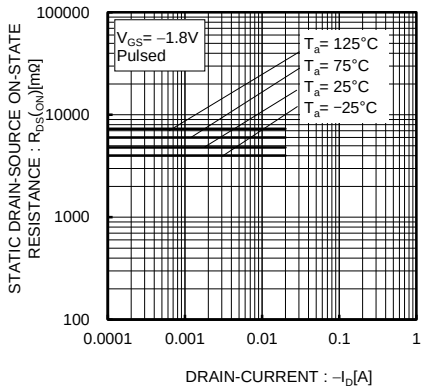


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

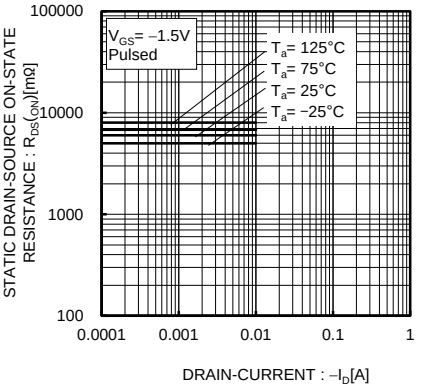


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅴ)

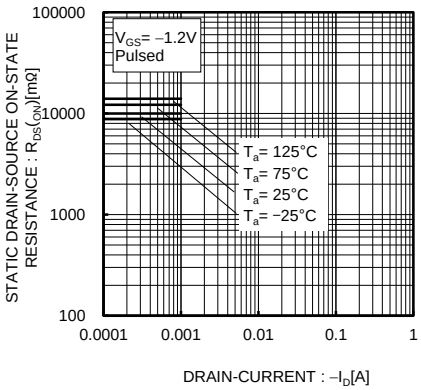


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current(Ⅵ)

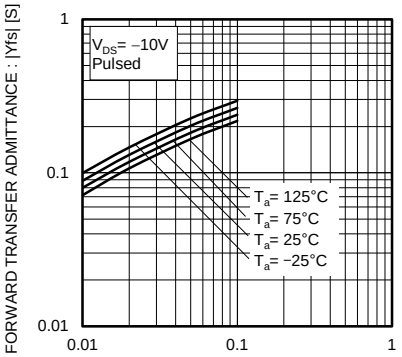


Fig.10 Forward Transfer Admittance vs. Drain Current

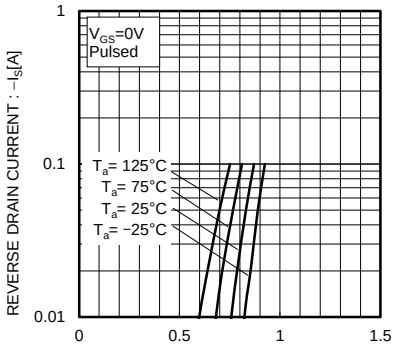


Fig.11 Reverse Drain Current vs. Sourse-Drain Voltage

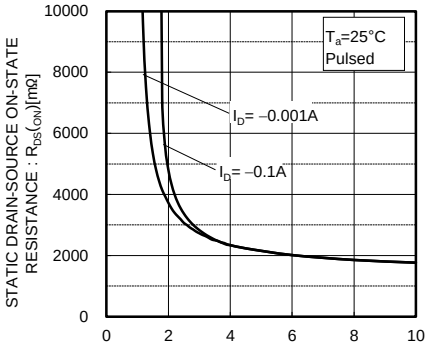


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

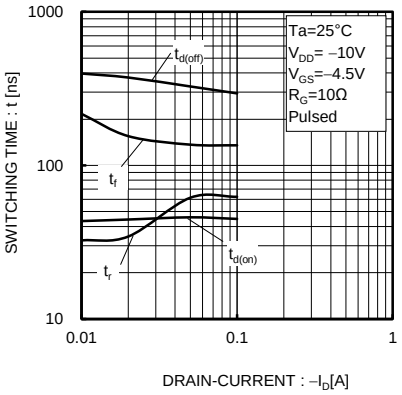


Fig.13 Switching Characteristics

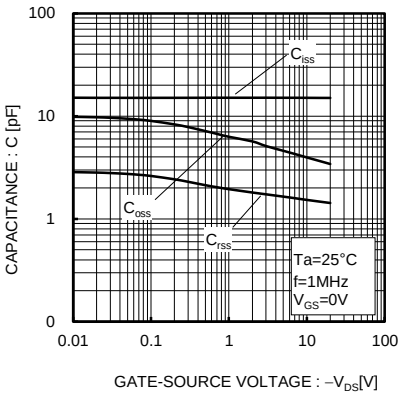


Fig.14 Typical Capacitance vs. Drain-Source Voltage

● **Measurement circuits**

<Tr1(Nch)>

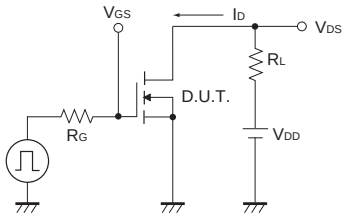


Fig.1-1 Switching Time Measurement Circuit

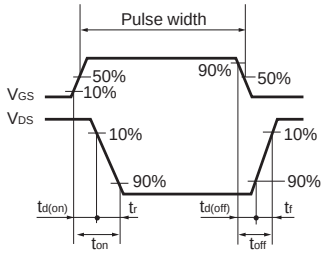


Fig.1-2 Switching Waveforms

<Tr2(Pch)>

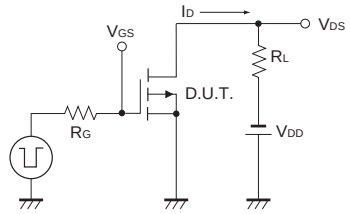


Fig.1-1 Switching Time Measurement Circuit

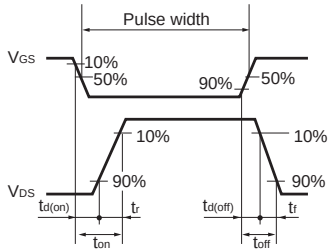


Fig.1-2 Switching Waveforms

● **Notice**

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

Notes

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