

2.5V Drive Nch MOSFET

TT8K2

●Structure

Silicon N-channel MOSFET

●Features

- 1) Low on-state resistance with fast switching.
- 2) Low voltage drive (2.5V).

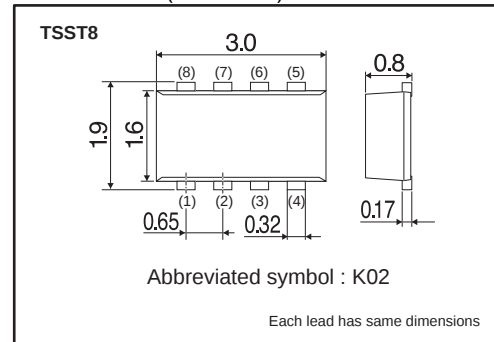
●Application

Switching

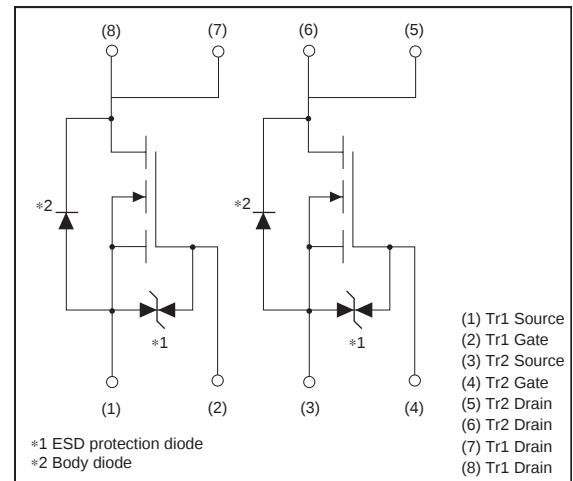
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
TT8K2		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	± 12	V
Drain current	Continuous	I_D	± 2.5	A
	Pulsed	I_{DP} *1	± 10	A
Source current (Body diode)	Continuous	I_S	0.8	A
	Pulsed	I_{SP} *1	10	A
Total power dissipation		P_D *2	1.25	W / TOTAL
			1.0	W / ELEMENT
Channel temperature		T_{ch}	150	°C
Range of Storage temperature		T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 When mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	100	°C / W / TOTAL
		125	°C / W / ELEMENT

* When mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	± 10	μA	$V_{GS}=\pm 12V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D=1mA$, $V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS}=30V$, $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.5	—	1.5	V	$V_{DS}=10V$, $I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	65	90	m Ω	$I_D=2.5A$, $V_{GS}=4.5V$
		—	70	95	m Ω	$I_D=2.5A$, $V_{GS}=4V$
		—	95	130	m Ω	$I_D=2.5A$, $V_{GS}=2.5V$
Forward transfer admittance	$ Y_{fs} $ *	2.2	—	—	S	$V_{DS}=10V$, $I_D=2.5A$
Input capacitance	C_{iss}	—	180	—	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	—	60	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	35	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	7	—	ns	$V_{DD} \doteq 15V$
Rise time	t_r *	—	30	—	ns	$I_D=1.2A$
Turn-off delay time	$t_{d(off)}$ *	—	20	—	ns	$V_{GS}=4.5V$
Fall time	t_f *	—	20	—	ns	$R_L \doteq 12.5\Omega$
Total gate charge	Q_g *	—	3.2	—	nC	$V_{DD} \doteq 15V$, $I_D=2.5A$
Gate-source charge	Q_{gs} *	—	0.9	—	nC	$V_{GS}=4.5V$
Gate-drain charge	Q_{gd} *	—	0.4	—	nC	$R_L \doteq 6\Omega$, $R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	—	—	1.2	V	$I_S=2.5A$, $V_{GS}=0V$

*Pulsed

●Electrical characteristics curves

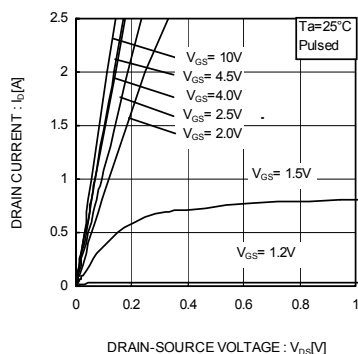


Fig.1 Typical Output Characteristics(I)

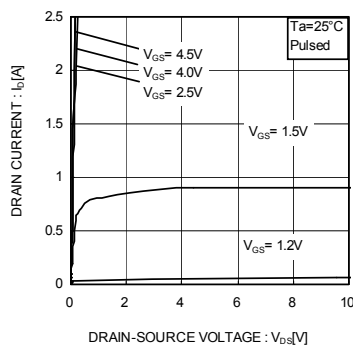


Fig.2 Typical Output Characteristics(II)

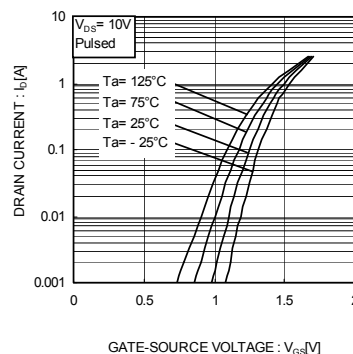


Fig.3 Typical Transfer Characteristics

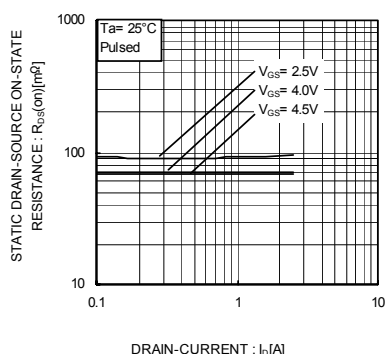


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

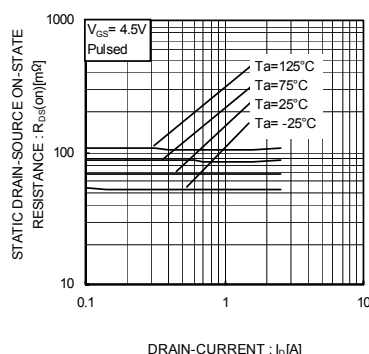


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

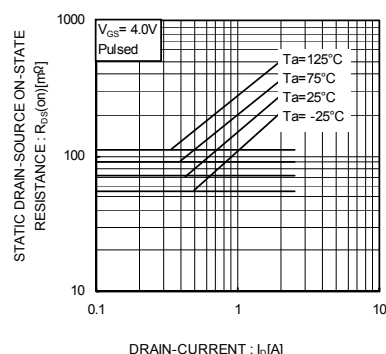


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

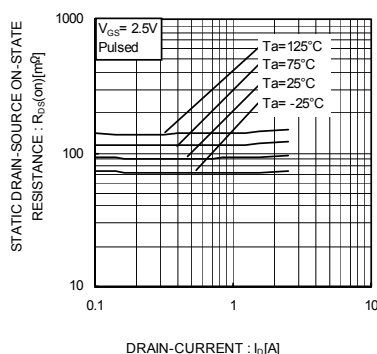


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

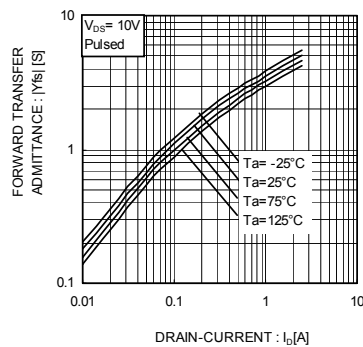


Fig.8 Forward Transfer Admittance vs. Drain Current

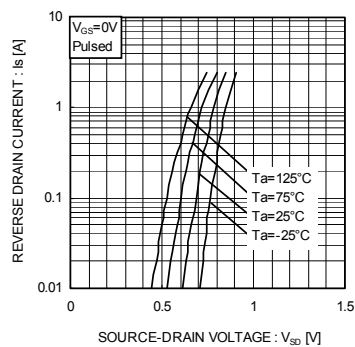


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

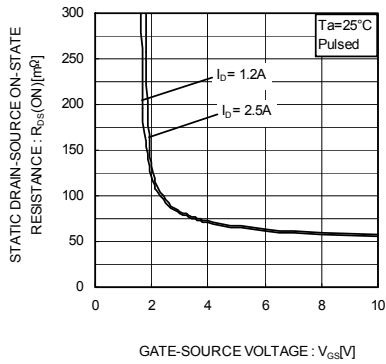


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

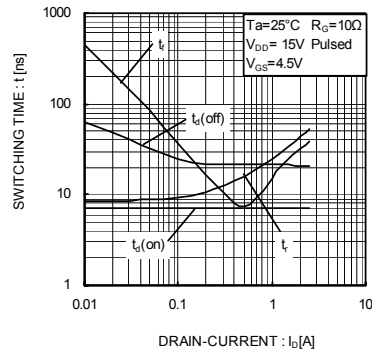


Fig.11 Switching Characteristics

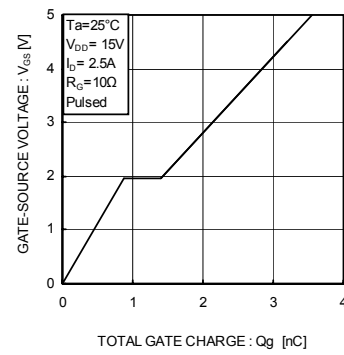


Fig.12 Dynamic Input Characteristics

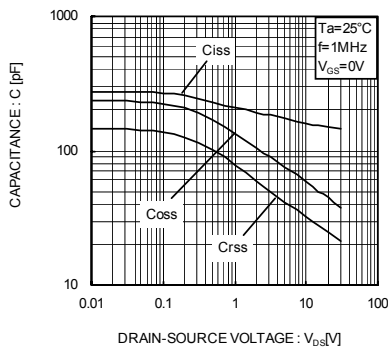


Fig.13 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuits

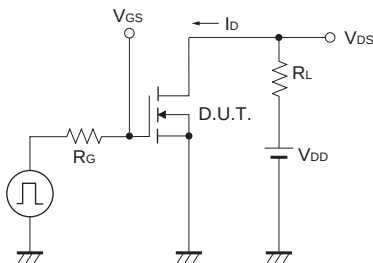


Fig.1-1 Switching Time Measurement Circuit

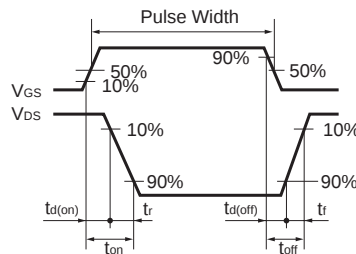


Fig.1-2 Switching Waveforms

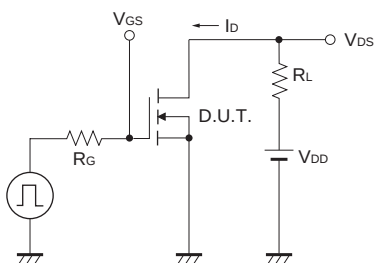


Fig.2-1 Gate Charge Measurement Circuit

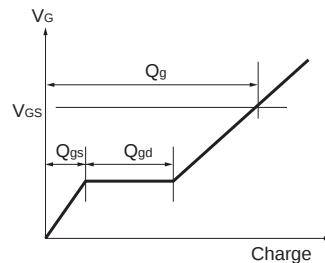


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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