

4V Drive Nch + Nch MOSFET

TT8K11

● Structure

Silicon N-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) Low voltage drive(4V drive).
- 3) Small surface mount package(TSST8).

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TCR
	Basic ordering unit (pieces)	3000
TT8K11		○

● Absolute maximum ratings (Ta = 25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	Continuous	I_D	± 3	A
	Pulsed	I_{DP} *1	± 12	A
Source current (Body Diode)	Continuous	I_s	0.8	A
	Pulsed	I_{sp} *1	12	A
Power dissipation		P_D *2	1.25	W / TOTAL
			1.0	W / ELEMENT
Channel temperature		T_{ch}	150	°C
Range of storage temperature		T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

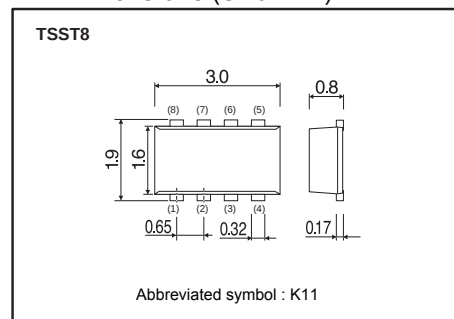
*2 Mounted on a ceramic board.

● Thermal resistance

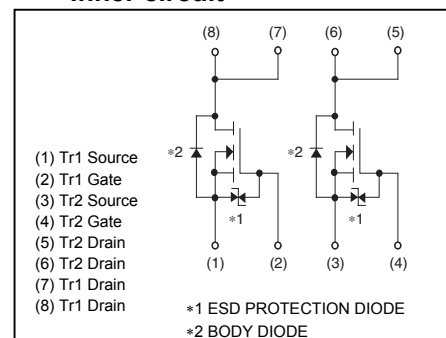
Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)^*$	100	°C / W / TOTAL
		125	°C / W / ELEMENT

*Mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	$V_{GS}=±20V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$I_D=1mA$, $V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=30V$, $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	-	2.5	V	$V_{DS}=10V$, $I_D=1A$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	51	71	mΩ	$I_D=3A$, $V_{GS}=10V$
		-	67	94		$I_D=3A$, $V_{GS}=4.5V$
		-	78	109		$I_D=3A$, $V_{GS}=4V$
Forward transfer admittance	$ Y_{fs} ^*$	2.0	-	-	S	$V_{DS}=10V$, $I_D=3A$
Input capacitance	C_{iss}	-	140	-	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	-	55	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	28	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	5	-	ns	$V_{DD}=15V$, $I_D=1.5A$
Rise time	t_r^*	-	13	-	ns	$V_{GS}=4.5V$
Turn-off delay time	$t_{d(off)}^*$	-	20	-	ns	$R_L=10Ω$
Fall time	t_f^*	-	3	-	ns	$R_G=10Ω$
Total gate charge	Q_g^*	-	2.5	-	nC	$V_{DD}=15V$, $I_D=3A$
Gate-source charge	Q_{gs}^*	-	0.8	-	nC	$V_{GS}=5V$
Gate-drain charge	Q_{gd}^*	-	0.6	-	nC	

*Pulsed

● **Body diode characteristics** (Source-Drain)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	1.2	V	$I_s=3A$, $V_{GS}=0V$

*Pulsed

●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical Output Characteristics (I)

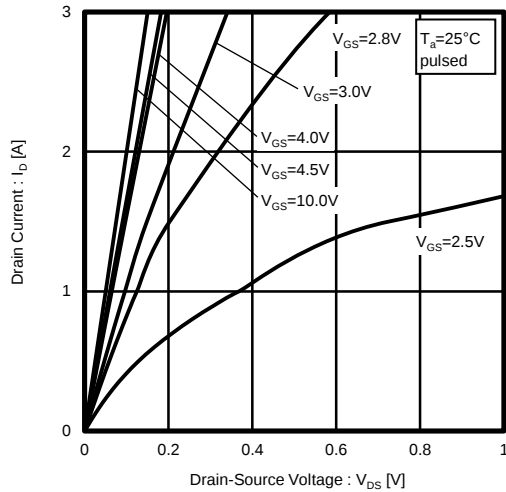


Fig.2 Typical Output Characteristics (II)

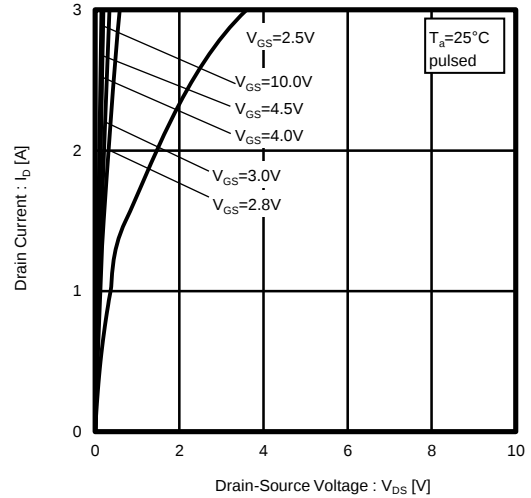


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

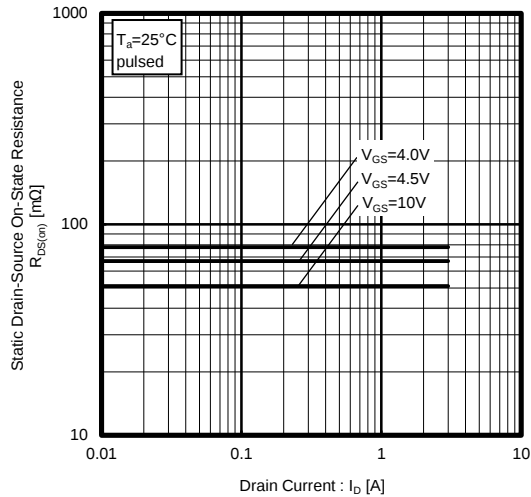


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

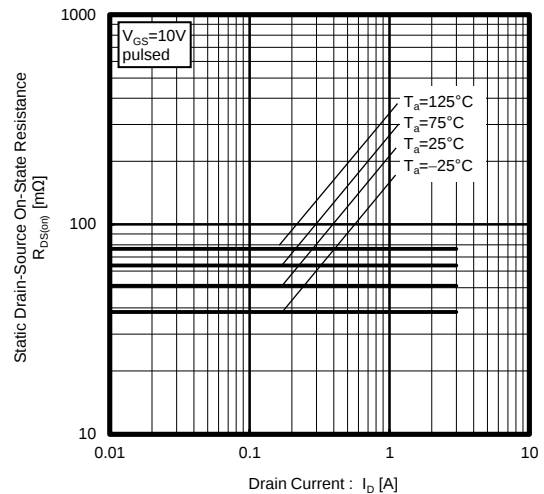


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

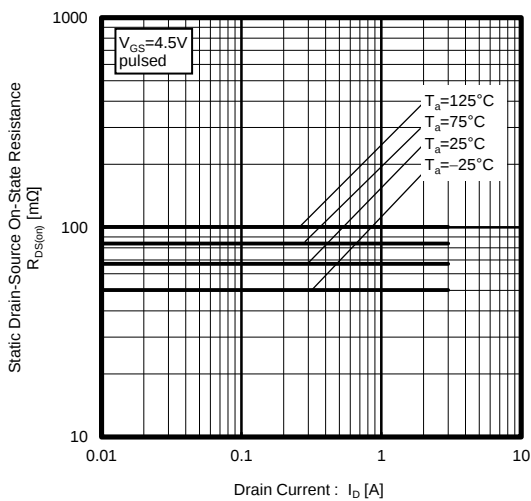


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

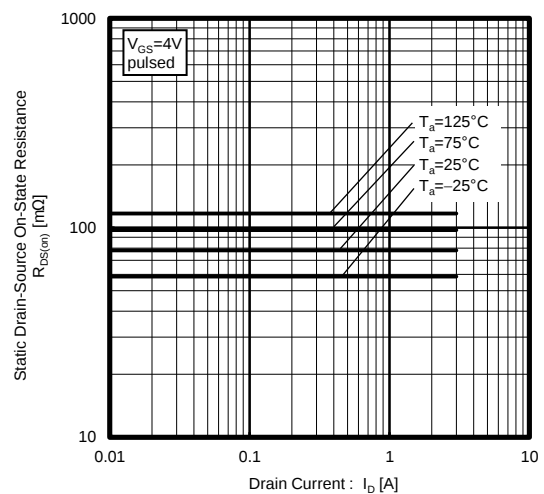


Fig.7 Forward Transfer Admittance vs. Drain Current

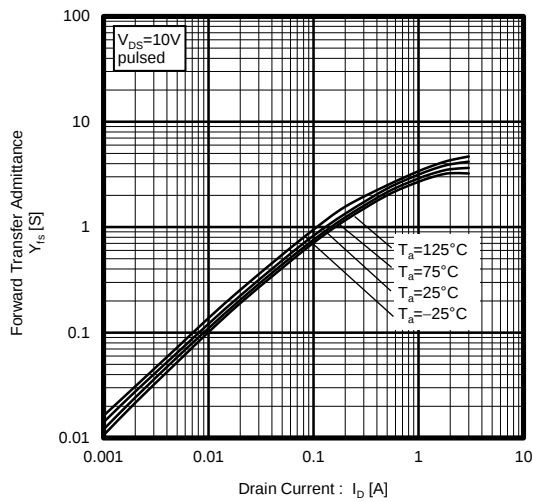


Fig.8 Typical Transfer Characteristics

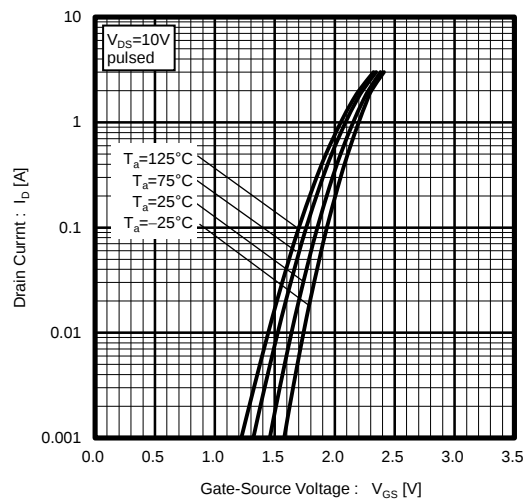


Fig.9 Source Current vs. Source-Drain Voltage

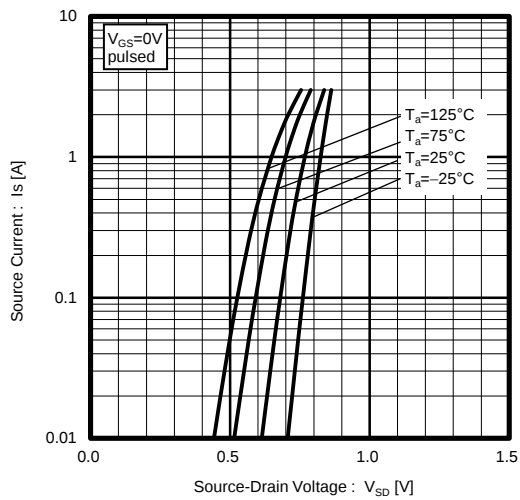


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

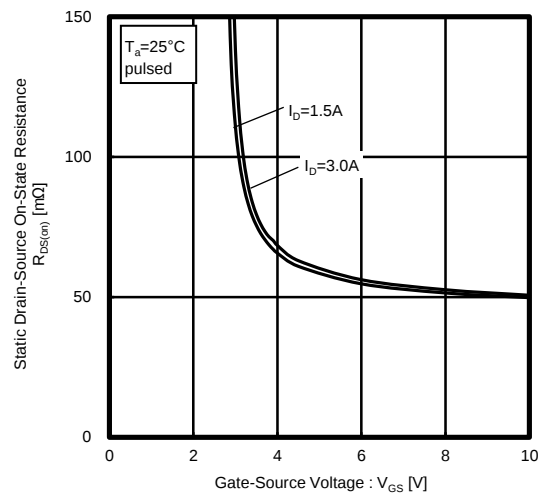


Fig.11 Switching Characteristics

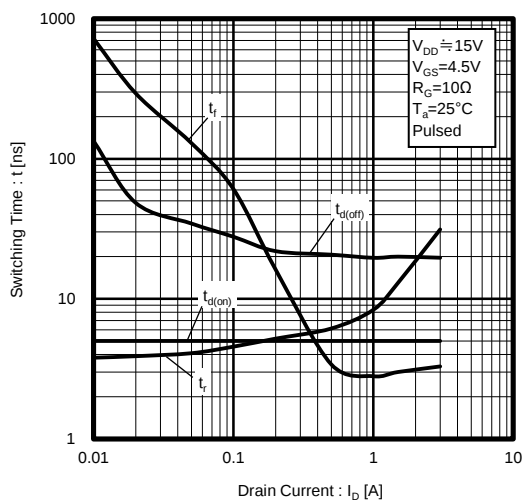


Fig.12 Dynamic Input Characteristics

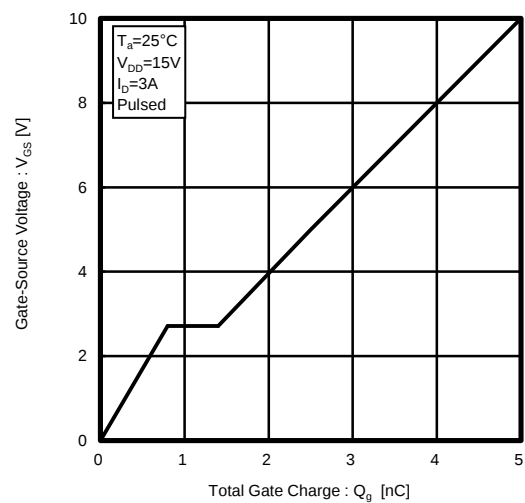


Fig.13 Typical Capacitance vs. Drain-Source Voltage

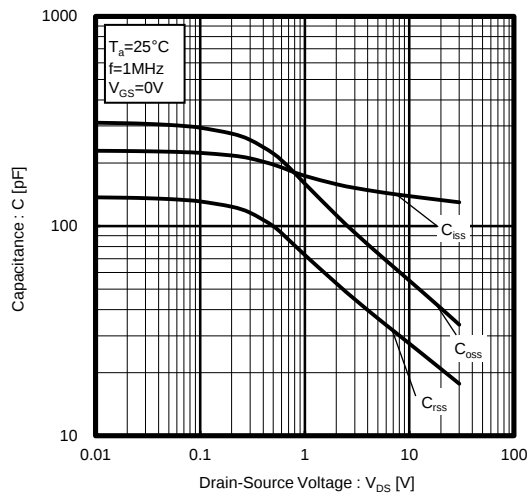


Fig.14 Maximum Safe Operating Area

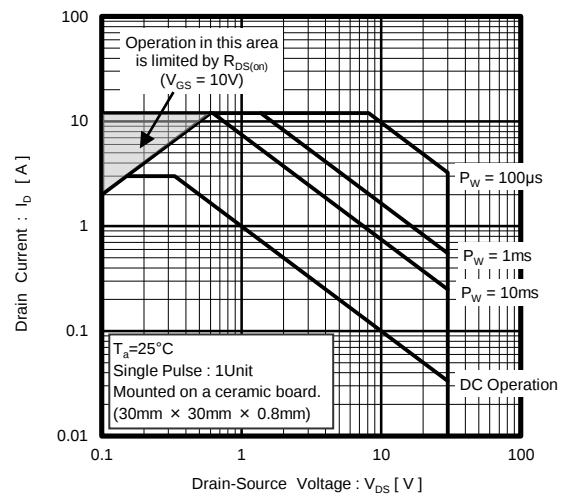
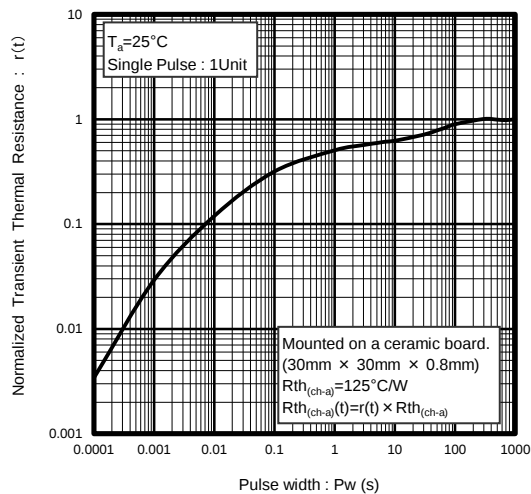


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



● Measurement circuits

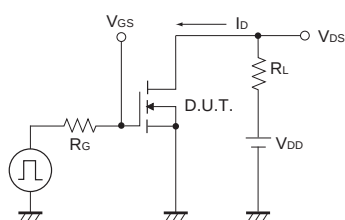


Fig.1-1 Switching Time Measurement Circuit

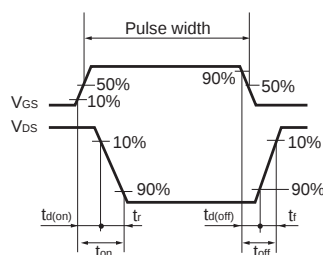


Fig.1-2 Switching Waveforms

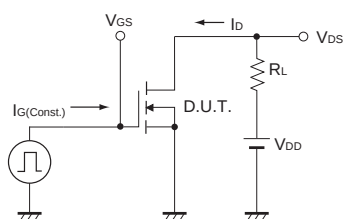


Fig.2-1 Gate Charge Measurement Circuit

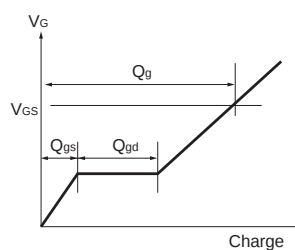


Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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