4V Drive Nch + Pch MOSFET

SH8M14

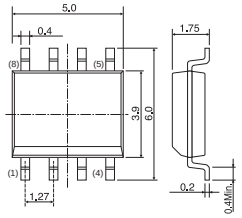
● Structure
Silicon N-channel MOSFET/
Silicon P-channel MOSFET

● Features
1) Low on-resistance.
2) High power package(SOP8).
3) Low voltage drive(4V drive).

● Application
Switching

● Dimensions (Unit : mm)

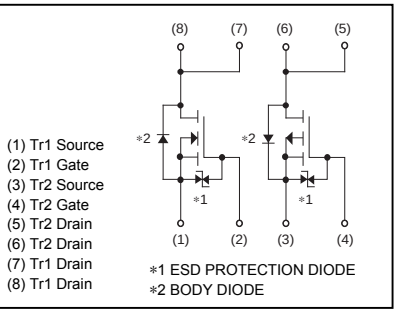
SOP8



● Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SH8M14		O

● Inner circuit



● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage		V_{DSS}	30	−30	V
Gate-source voltage		V_{GSS}	±20	±20	V
Drain current	Continuous	I_D	±9	±7	A
	Pulsed	I_{DP} *1	±36	±28	A
Source current (Body Diode)	Continuous	I_s	1.6	−1.6	A
	Pulsed	I_{sp} *1	36	−28	A
Power dissipation		P_D *2	2.0		W / TOTAL
			1.4		W / ELEMENT
Channel temperature		Tch	150		°C
Range of storage temperature		Tstg	−55 to +150		°C

*1 Pw≤10μs, Duty cycle≤1%

*2 Mounted on a ceramic board.

● **Electrical characteristics** (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1.0	-	2.5	V	V_{DS}=10V, I_D=1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	-	15	21	mΩ	I_D=9A, V_{GS}=10V
		-	18	25		I_D=9A, V_{GS}=4.5V
			20	28		I_D=9A, V_{GS}=4V
Forward transfer admittance	$\|Y_{fs}\|$ *	5.0	-	-	S	V_{DS}=10V, I_D=9A
Input capacitance	C_{iss}	-	630	-	pF	V_{DS}=10V
Output capacitance	C_{oss}	-	230	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	110	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$ *	-	10	-	ns	I_D=4.5A, V_{DD}≒15V
Rise time	t_r *	-	33	-	ns	V_{GS}=10V
Turn-off delay time	$t_{d(off)}$ *	-	42	-	ns	R_L=3.3Ω
Fall time	t_f *	-	10	-	ns	R_G=10Ω
Total gate charge	Q_g *	-	8.5	-	nC	I_D=9A, V_{DD}≒15V
Gate-source charge	Q_{gs} *	-	2.3	-	nC	V_{GS}=5V
Gate-drain charge	Q_{gd} *	-	4.0	-	nC	

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD} *	-	-	1.2	V	I_s=9A, V_{GS}=0V

*Pulsed

● **Electrical characteristics** (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	−30	-	-	V	I_D=−1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}		-	−1	μA	V_{DS}=−30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	−1.0	-	−2.5	V	V_{DS}=−10V, I_D=−1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	-	21.5	29.0	mΩ	I_D=−7A, V_{GS}=−10V
		-	29.0	39.0		I_D=−3.5A, V_{GS}=−4.5V
		-	31.0	40.8		I_D=−3.5A, V_{GS}=−4.0V
Forward transfer admittance	$\|Y_{fs}\|$*	6.0	-	-	S	V_{DS}=−10V, I_D=−7A
Input capacitance	C_{iss}	-	1200	-	pF	V_{DS}=−10V
Output capacitance	C_{oss}	-	170	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	170	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	12	-	ns	I_D=−3.5A, V_{DD}≒−15V
Rise time	t_r *	-	40	-	ns	V_{GS}=−10V
Turn-off delay time	$t_{d(off)}$*	-	80	-	ns	R_L=4.27Ω
Fall time	t_f *	-	65	-	ns	R_G=10Ω
Total gate charge	Q_g *	-	18	-	nC	I_D=−7A, V_{DD}≒−15V
Gate-source charge	Q_{gs} *	-	3.5	-	nC	V_{GS}=−5V
Gate-drain charge	Q_{gd} *	-	6.5	-	nC	

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	−1.2	V	I_s=−7A, V_{GS}=0V

*Pulsed

●Electrical characteristic curves (Ta=25°C)

〈Tr.1(Nch)〉

Fig.1 Typical Output Characteristics (Ⅰ)

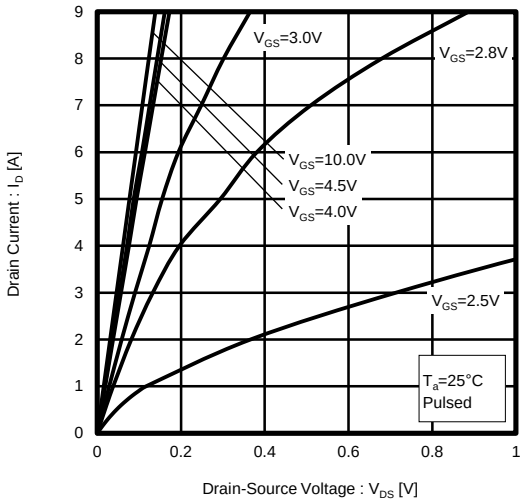


Fig.2 Typical Output Characteristics (Ⅱ)

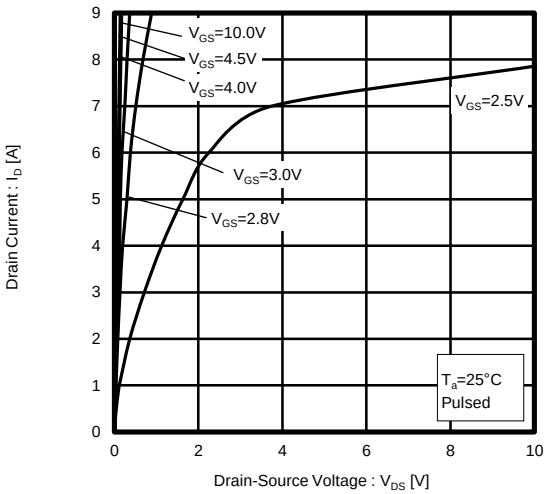


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

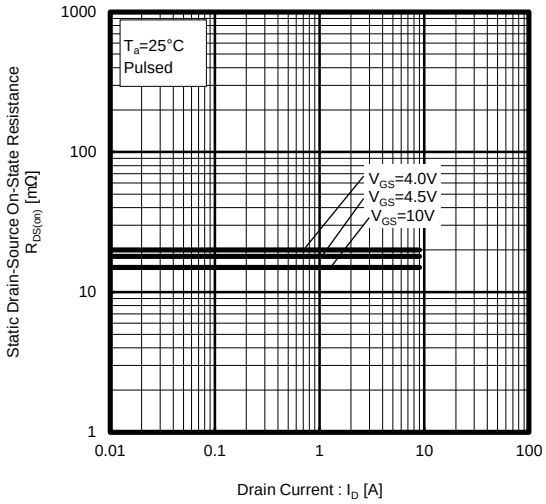


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

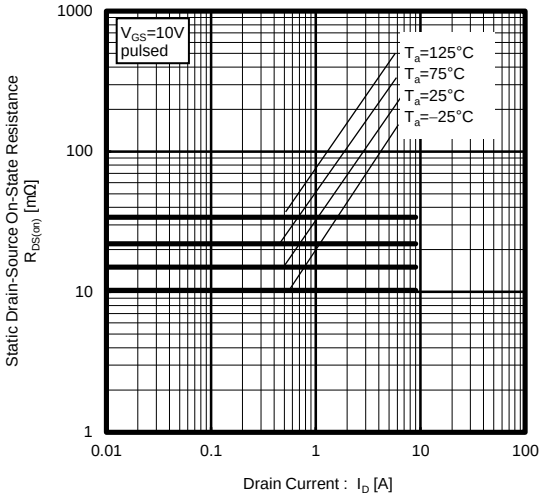


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

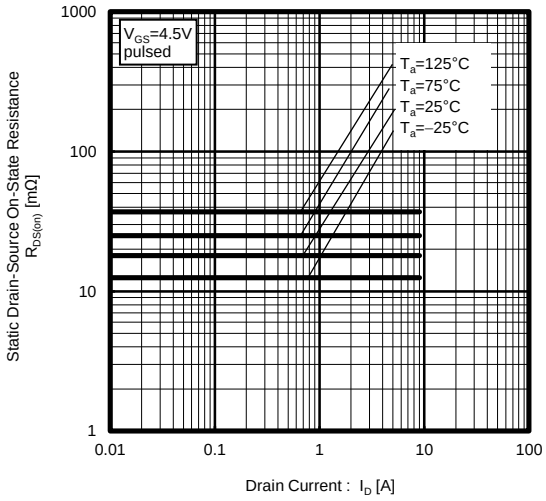


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

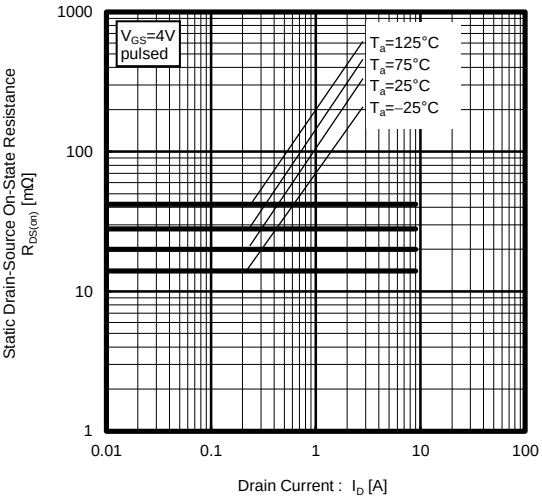


Fig.7 Forward Transfer Admittance vs. Drain Current

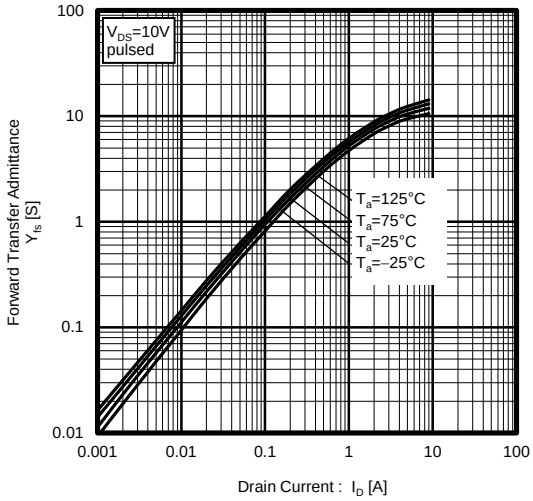


Fig.8 Typical Transfer Characteristics

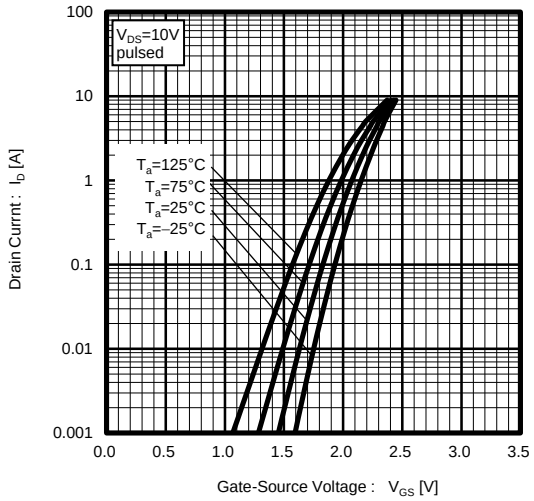


Fig.9 Source Current vs. Source-Drain Voltage

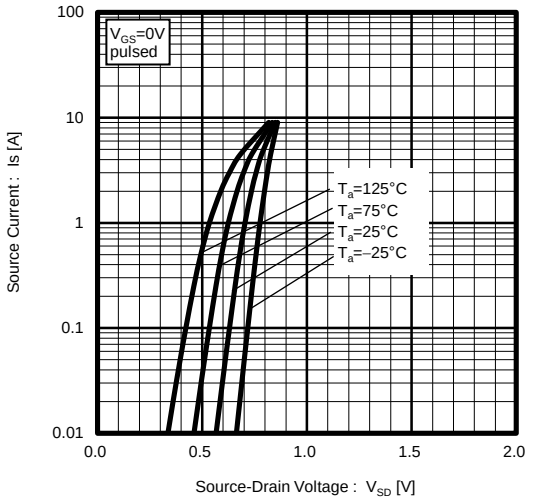


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

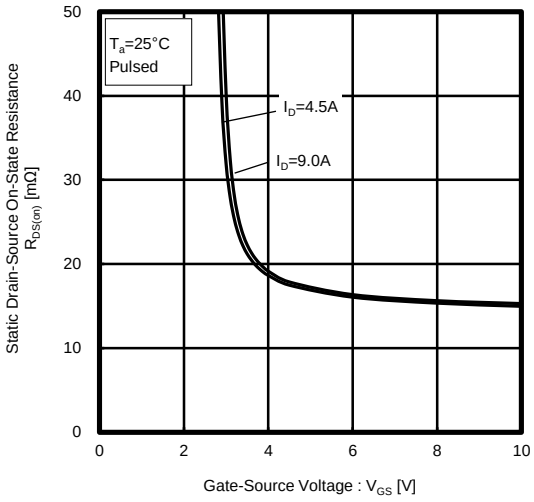


Fig.11 Switching Characteristics

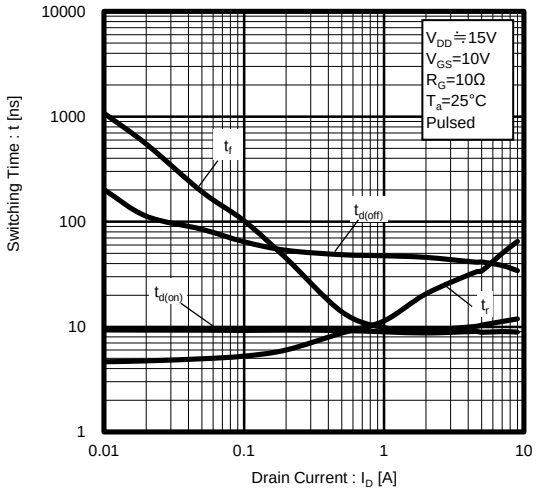


Fig.12 Dynamic Input Characteristics

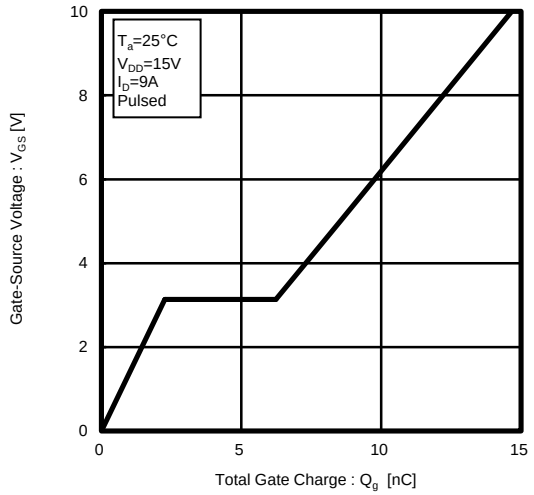


FIg.13 Typical Capacitance vs. Drain-Source Voltage

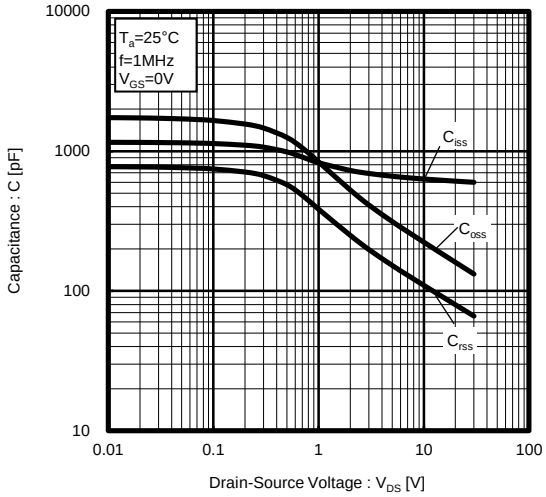


Fig.14 Maximum Safe Operating Area

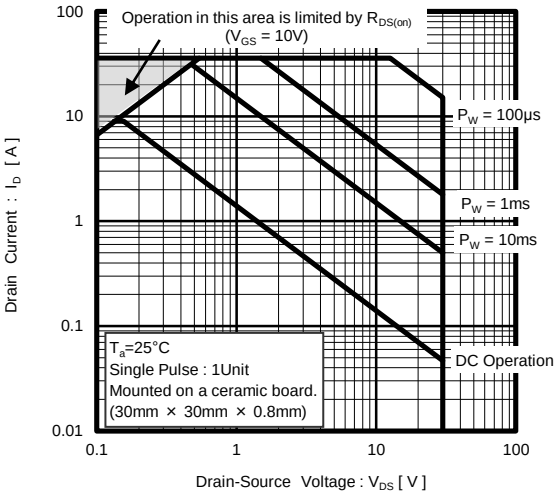
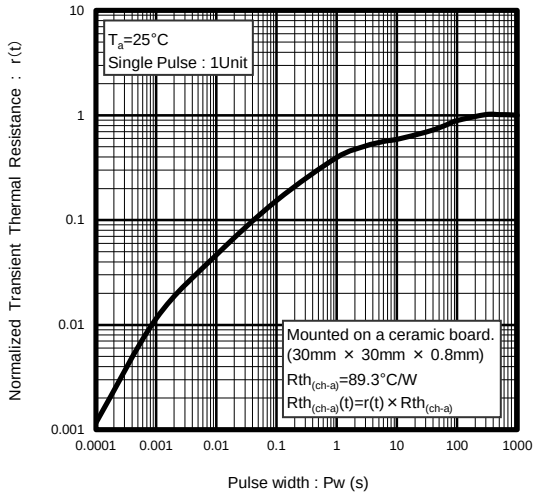


FIg.15 Normalized Transient Thermal Resistance v.s. Pulse Width



〈Tr.2(Pch)〉

Fig.1 Typical Output Characteristics(Ⅰ)

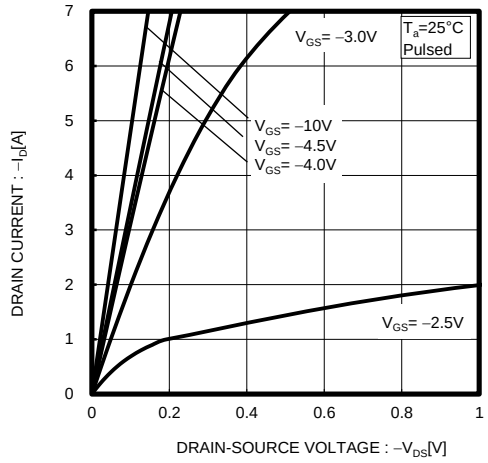


Fig.2 Typical Output Characteristics(Ⅱ)

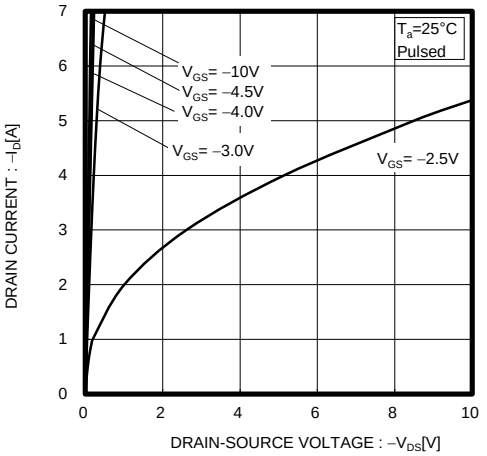


Fig.3 Typical Transfer Characteristics

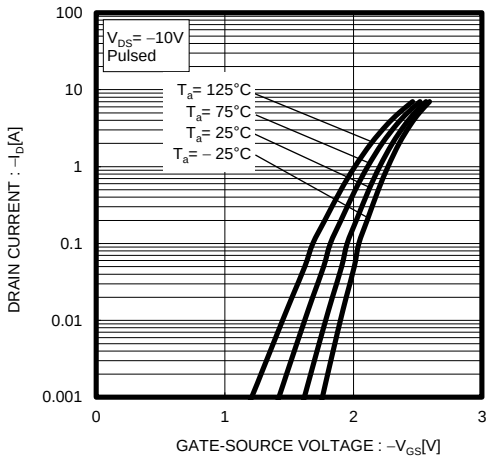


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

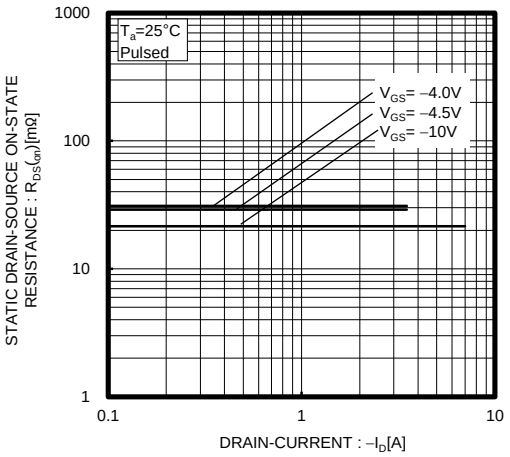


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

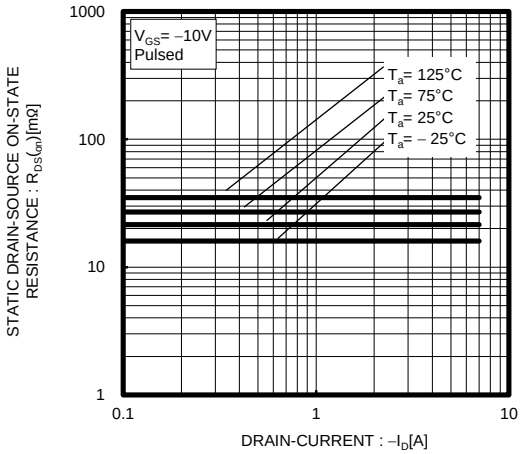


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

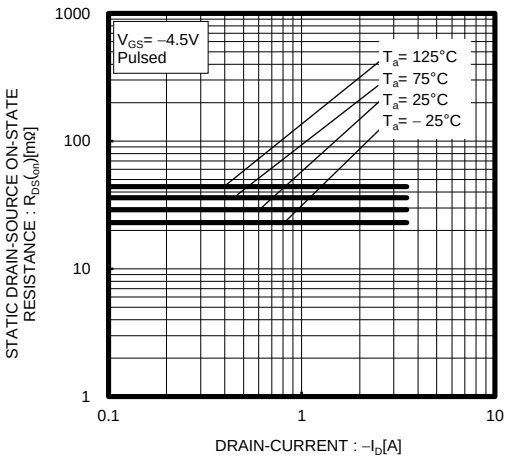


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

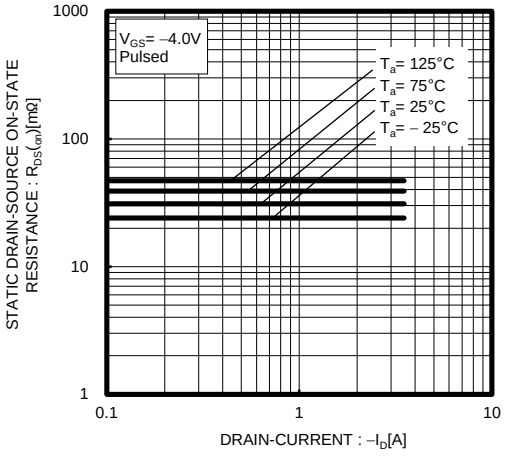


Fig.8 Forward Transfer Admittance vs. Drain Current

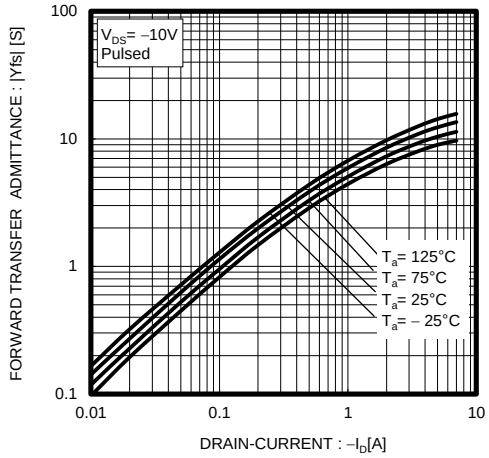


Fig.9 Reverse Drain Current vs. Sourse-Drain Voltage

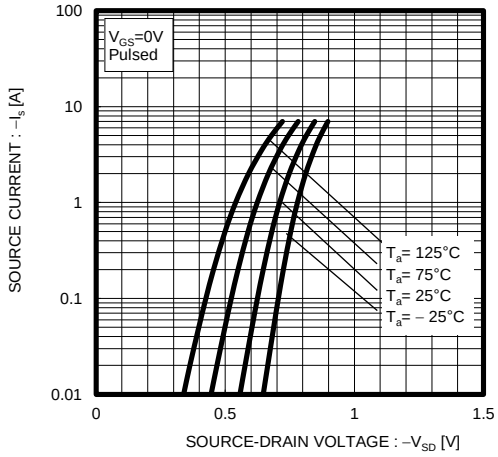


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

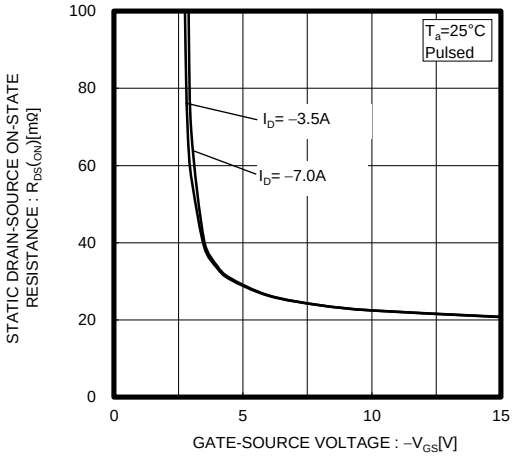


Fig.11 Switching Characteristics

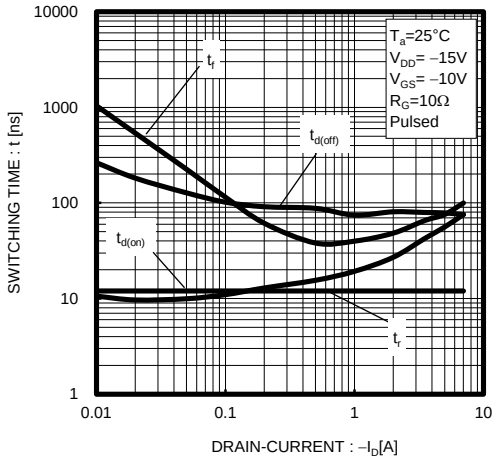


Fig.12 Dynamic Input Characteristics

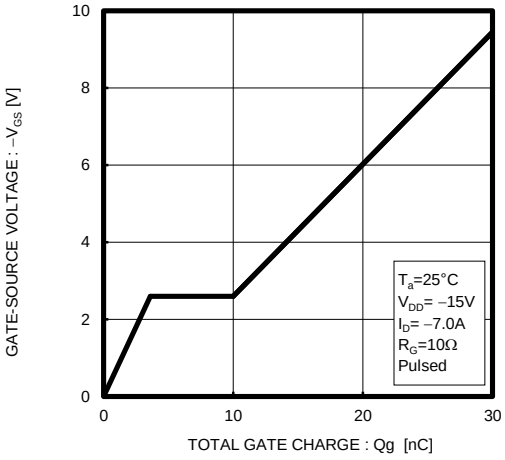


Fig.13 Typical Capacitance vs. Drain-Source Voltage

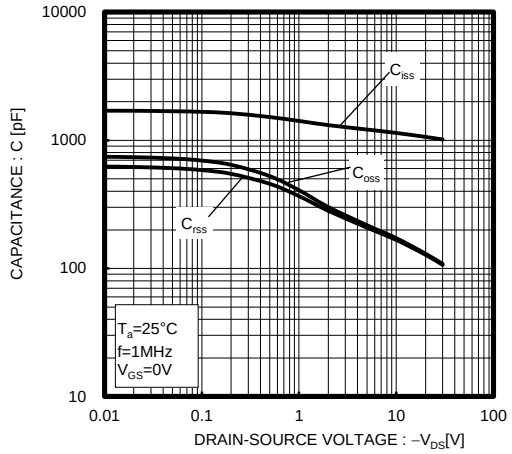


Fig.14 Maximum Safe Operating Aera

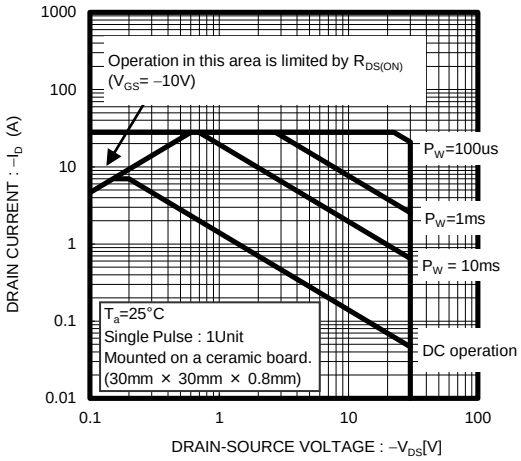
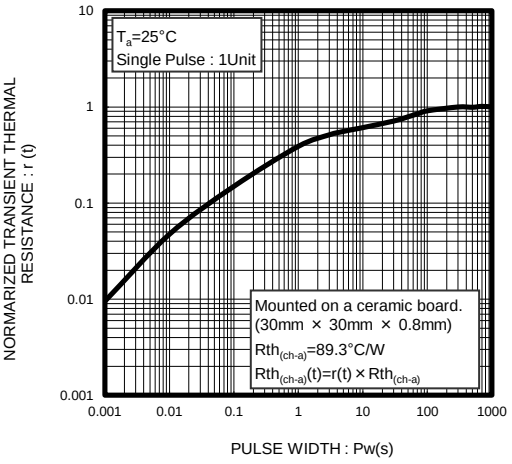


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width



● **Measurement circuits**

<Tr1(Nch)>

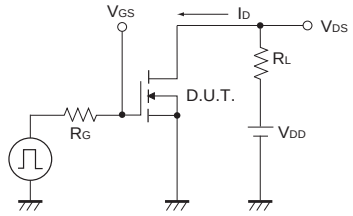


Fig.1-1 Switching Time Measurement Circuit

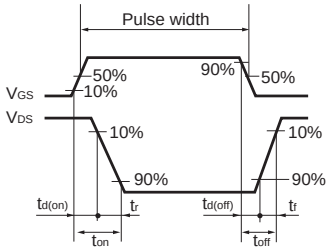


Fig.1-2 Switching Waveforms

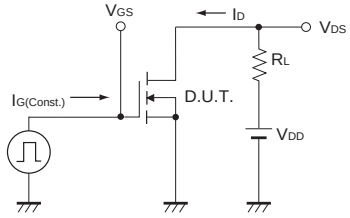


Fig.2-1 Gate Charge Measurement Circuit

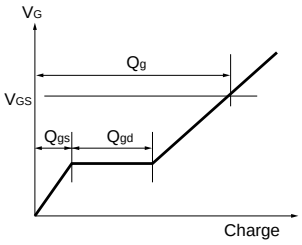


Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

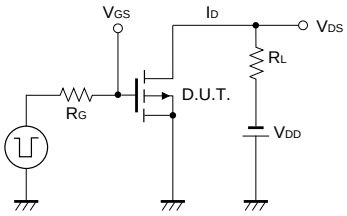


Fig.3-1 Switching Time Measurement Circuit

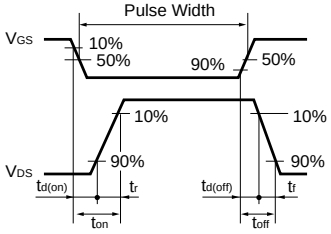


Fig.3-2 Switching Waveforms

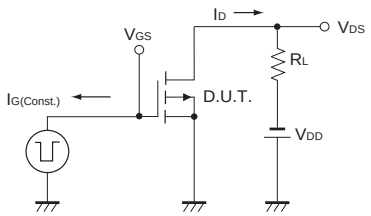


Fig.4-1 Gate Charge Measurement Circuit

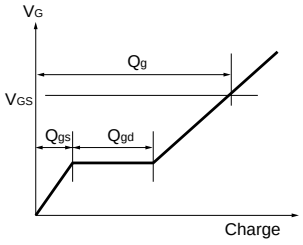


Fig.4-2 Gate Charge Waveform

● **Notice**

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Notes

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Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

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