

4V Drive Nch + Pch MOSFET

SH8M12

● Structure

Silicon N-channel MOSFET/
 Silicon P-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) High power package(SOP8).
- 3) Low voltage drive(4V drive).

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SH8M12		○

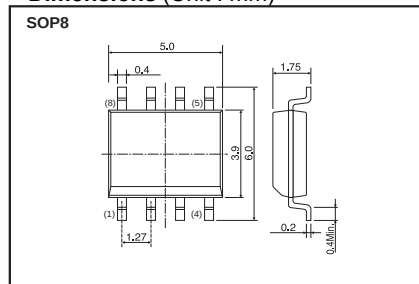
● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	V_{DSS}	30	-30	V
Gate-source voltage	V_{GSS}	±20	±20	V
Drain current	Continuous	I_D	±5	A
	Pulsed	I_{DP} *1	±20	A
Source current (Body Diode)	Continuous	I_S	1.6	A
	Pulsed	I_{sp} *1	20	A
Power dissipation	P_D *2	2.0		W / TOTAL
		1.4		W / ELEMENT
Channel temperature	T_{ch}	150		°C
Range of storage temperature	T_{stg}	-55 to +150		°C

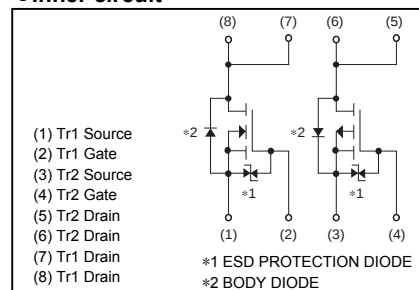
*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$I_D = 1mA$, $V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS} = 30V$, $V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	-	2.5	V	$V_{DS} = 10V$, $I_D = 1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	30	42	$m\Omega$	$I_D = 5A$, $V_{GS} = 10V$
		-	40	56		$I_D = 5A$, $V_{GS} = 4.5V$
		-	45	63		$I_D = 5A$, $V_{GS} = 4V$
Forward transfer admittance	$ Y_{fs} ^*$	2.5	-	-	S	$V_{DS} = 10V$, $I_D = 5A$
Input capacitance	C_{iss}	-	250	-	pF	$V_{DS} = 10V$
Output capacitance	C_{oss}	-	90	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	-	45	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	6	-	ns	$I_D = 2.5A$, $V_{DD} = 15V$
Rise time	t_r^*	-	27	-	ns	$V_{GS} = 10V$
Turn-off delay time	$t_{d(off)}^*$	-	26	-	ns	$R_L = 6\Omega$
Fall time	t_f^*	-	5	-	ns	$R_G = 10\Omega$
Total gate charge	Q_g^*	-	4.0	-	nC	$I_D = 5A$, $V_{DD} = 15V$
Gate-source charge	Q_{gs}^*	-	1.2	-	nC	$V_{GS} = 5V$
Gate-drain charge	Q_{gd}^*	-	1.2	-	nC	

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	1.2	V	$I_S = 5A$, $V_{GS} = 0V$

*Pulsed

● **Electrical characteristics** (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-30	-	-	V	$I_D = -1mA$, $V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}		-	-1	μA	$V_{DS} = -30V$, $V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-	-2.5	V	$V_{DS} = -10V$, $I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	40	56	m Ω	$I_D = -4.5A$, $V_{GS} = -10V$
		-	55	77		$I_D = -2.5A$, $V_{GS} = -4.5V$
		-	60	84		$I_D = -2.5A$, $V_{GS} = -4.0V$
Forward transfer admittance	$ Y_{fs} ^*$	3.5	-	-	S	$V_{DS} = -10V$, $I_D = -4.5A$
Input capacitance	C_{iss}	-	800	-	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	-	120	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	-	110	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	7	-	ns	$I_D = -2.5A$, $V_{DD} = -15V$
Rise time	t_r^*	-	15	-	ns	$V_{GS} = -10V$
Turn-off delay time	$t_{d(off)}^*$	-	70	-	ns	$R_L = 6\Omega$
Fall time	t_f^*	-	50	-	ns	$R_G = 10\Omega$
Total gate charge	Q_g^*	-	8.0	-	nC	$I_D = -4.5A$, $V_{DD} = -15V$
Gate-source charge	Q_{gs}^*	-	2.5	-	nC	$V_{GS} = -5V$
Gate-drain charge	Q_{gd}^*	-	3.0	-	nC	

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	-1.2	V	$I_s = -4.5A$, $V_{GS} = 0V$

*Pulsed

●Electrical characteristic curves (Ta=25°C)

〈Tr.1(Nch)〉

Fig.1 Typical Output Characteristics(I)

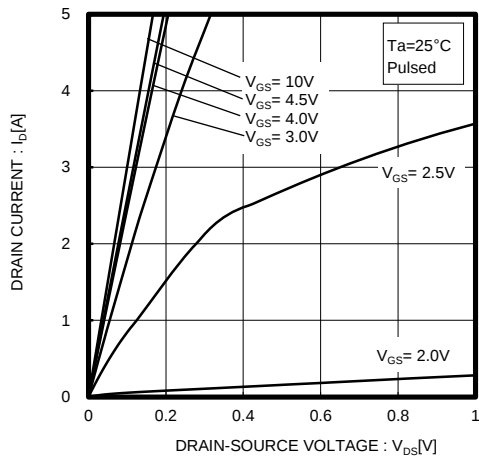


Fig.2 Typical Output Characteristics(II)

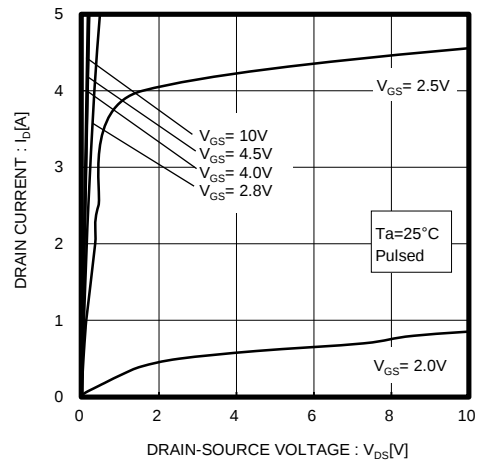


Fig.3 Typical Transfer Characteristics

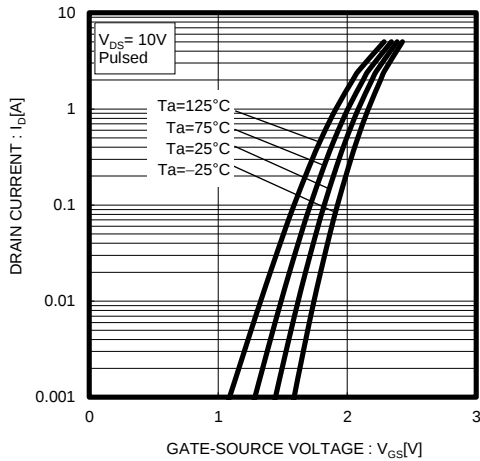


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

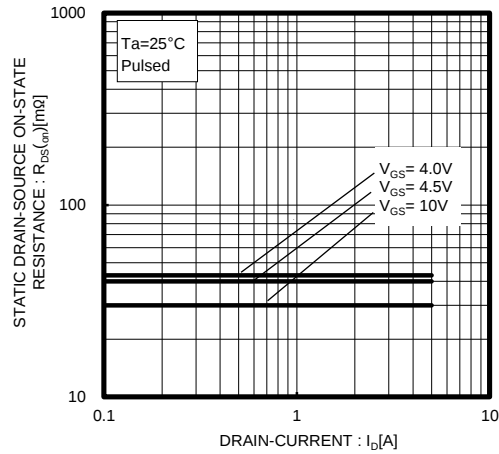


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

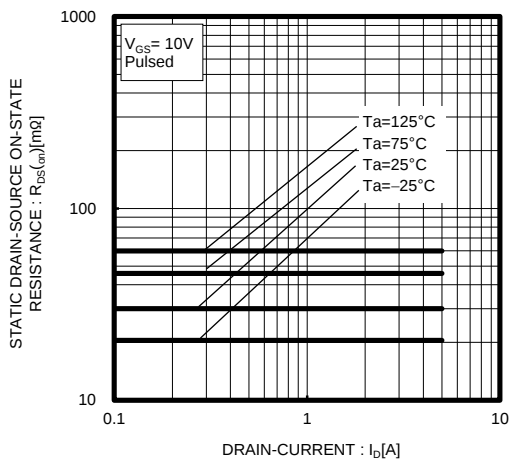


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

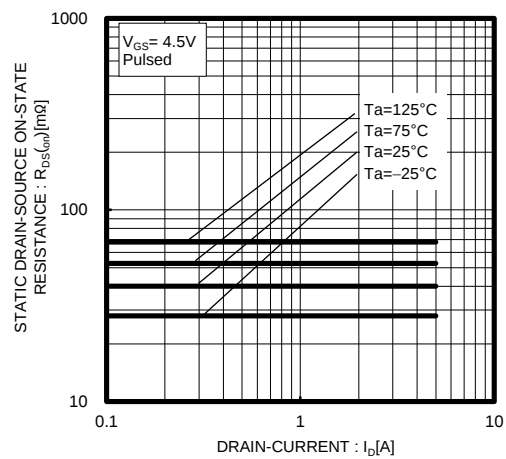


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

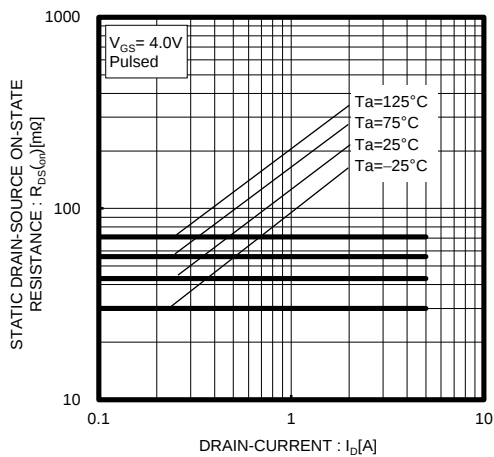


Fig.8 Forward Transfer Admittance vs. Drain Current

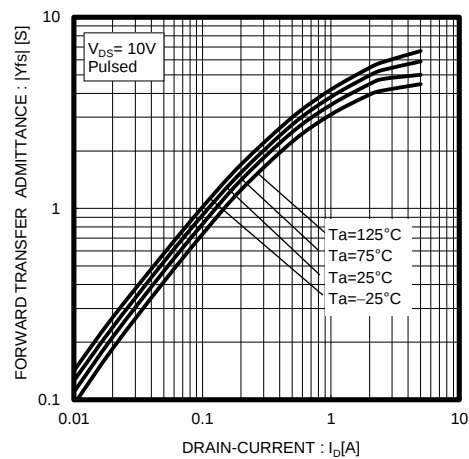


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

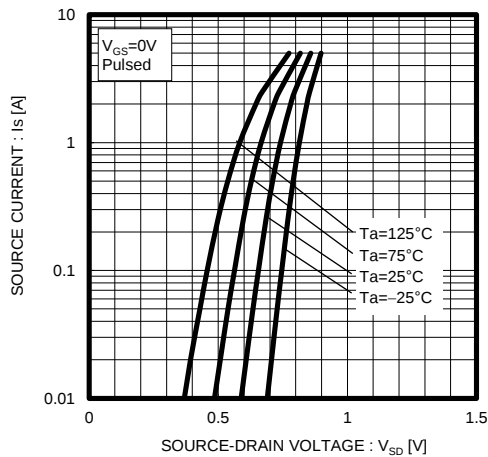


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

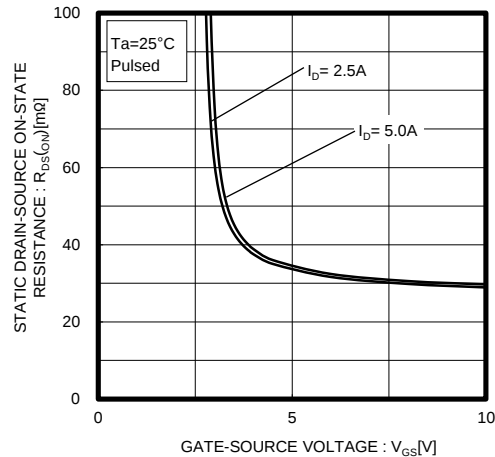


Fig.11 Switching Characteristics

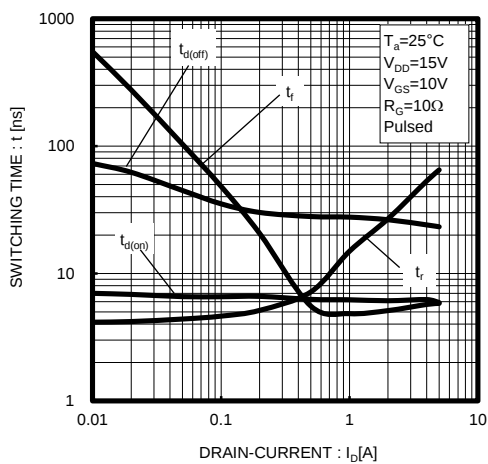


Fig.12 Dynamic Input Characteristics

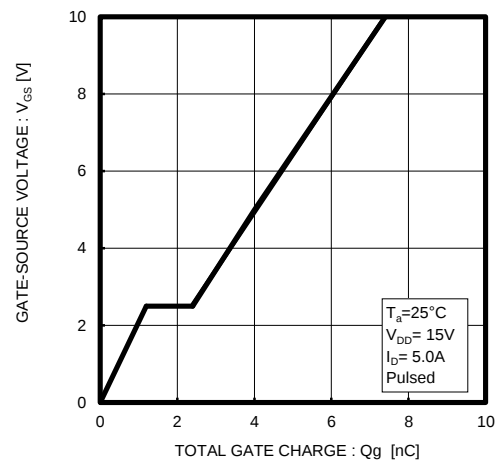


Fig.13 Typical Capacitance vs. Drain-Source Voltage

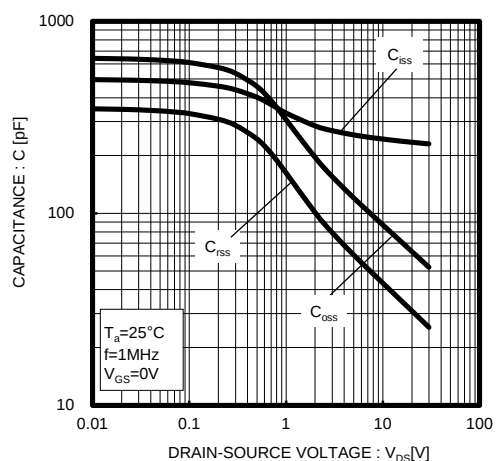


Fig.14 Maximum Safe Operating Area

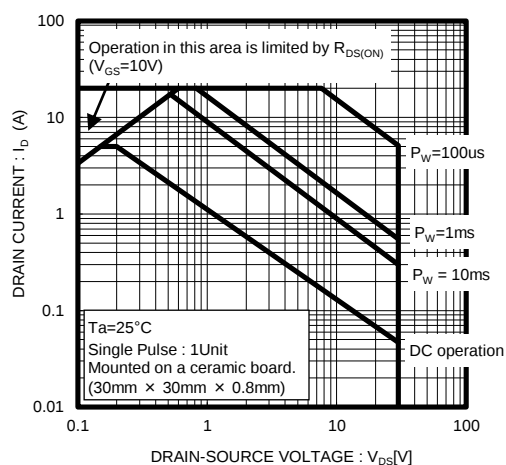
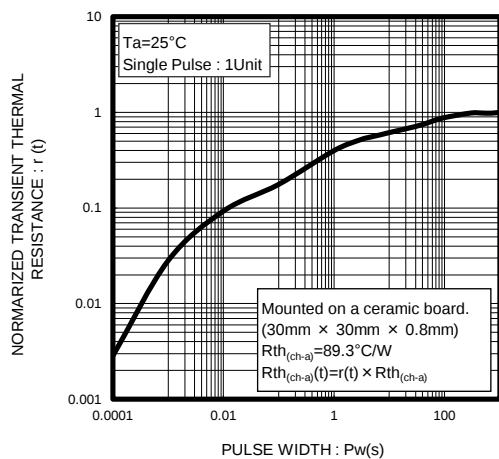


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width



〈Tr.2(Pch)〉

Fig.1 Typical Output Characteristics(I)

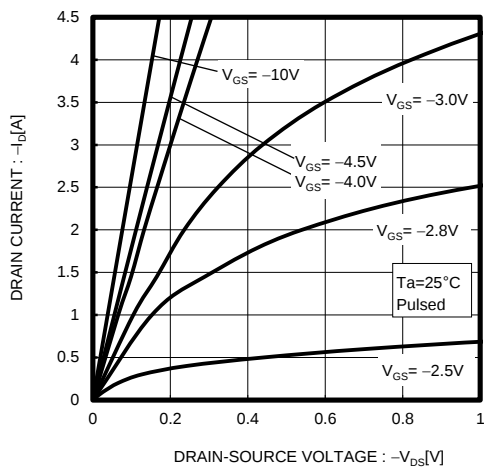


Fig.2 Typical Output Characteristics(II)

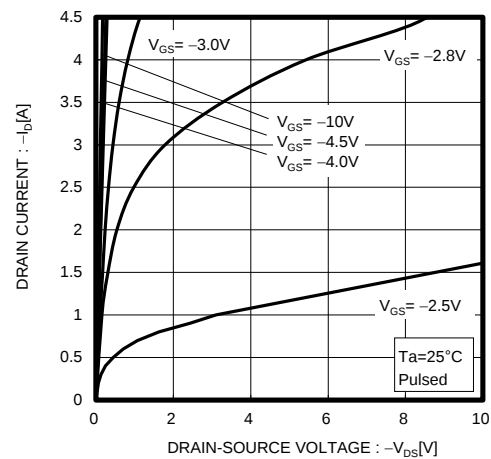


Fig.3 Typical Transfer Characteristics

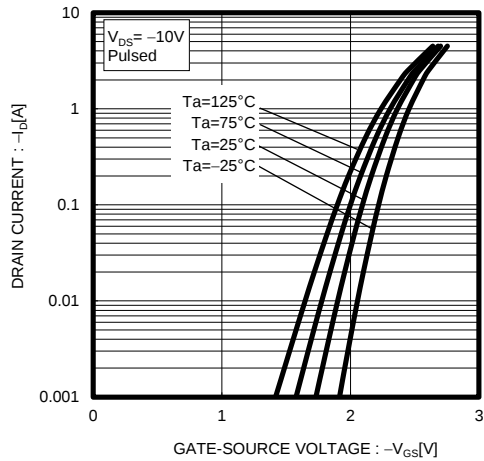


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

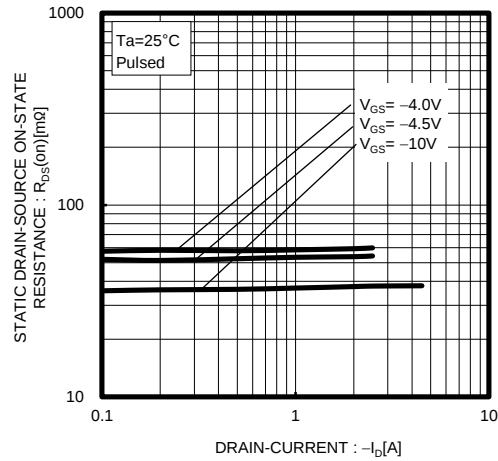


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

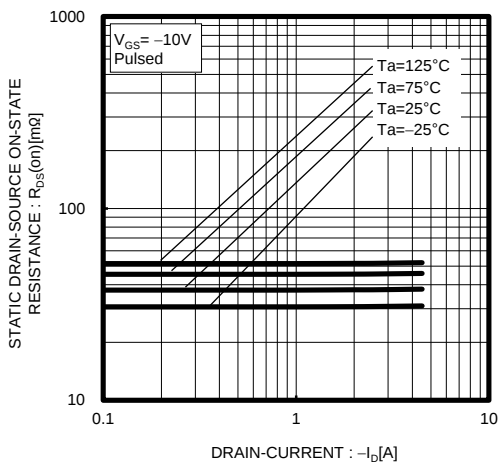


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

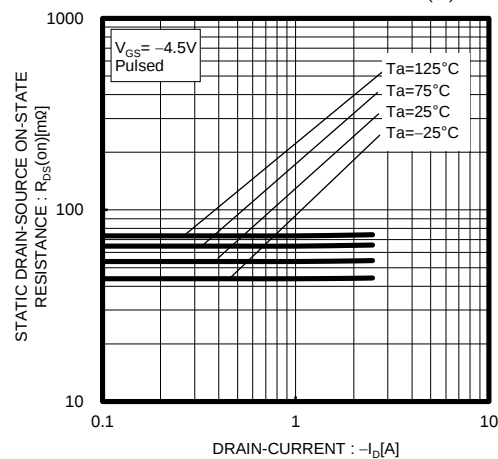


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

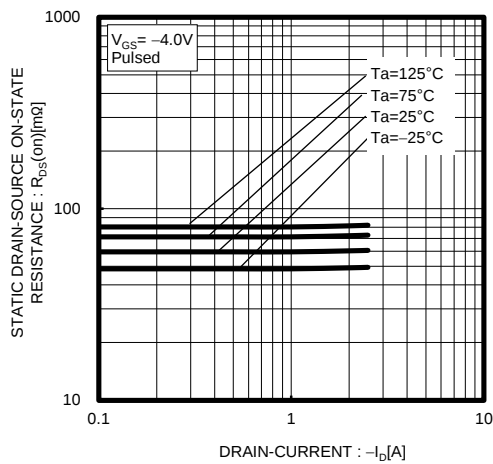


Fig.8 Forward Transfer Admittance vs. Drain Current

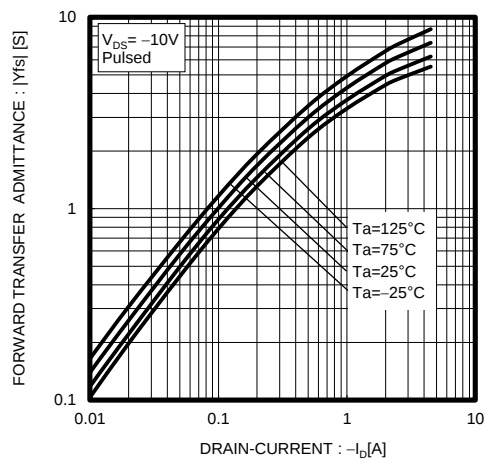


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

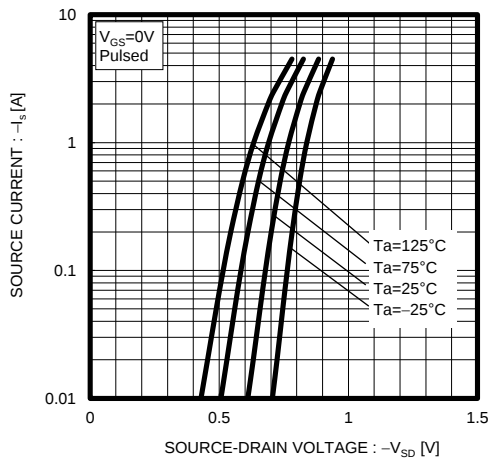


Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage

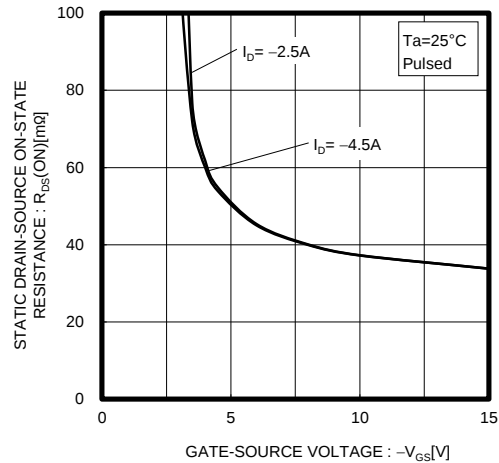


Fig.11 Switching Characteristics

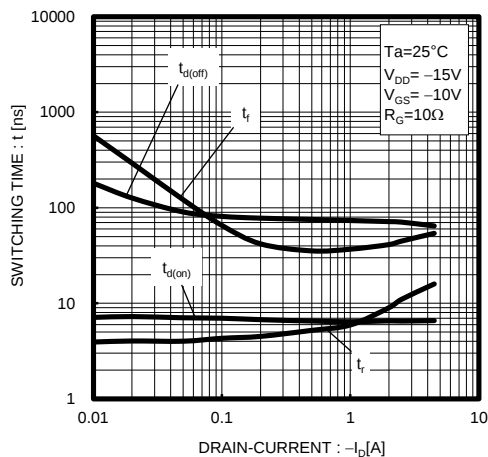


Fig.12 Dynamic Input Characteristics

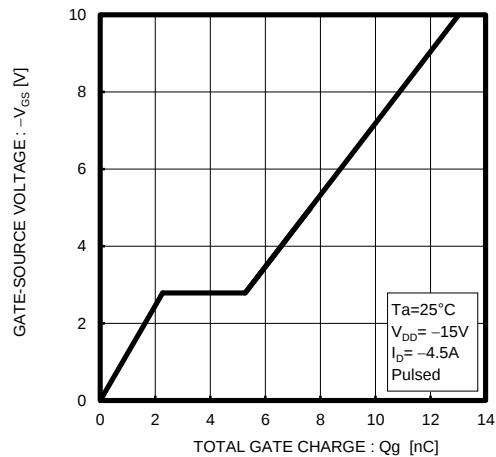


Fig.13 Typical Capacitance vs. Drain-Source Voltage

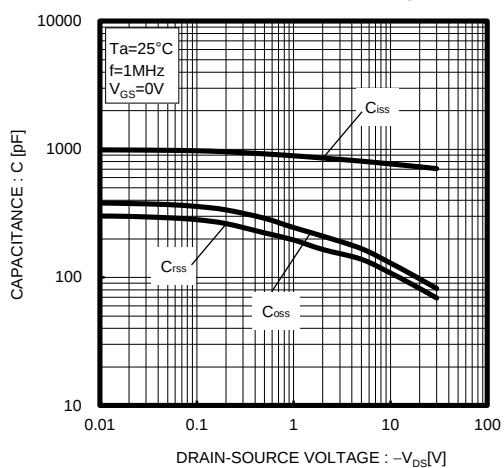


Fig.14 Maximum Safe Operating Area

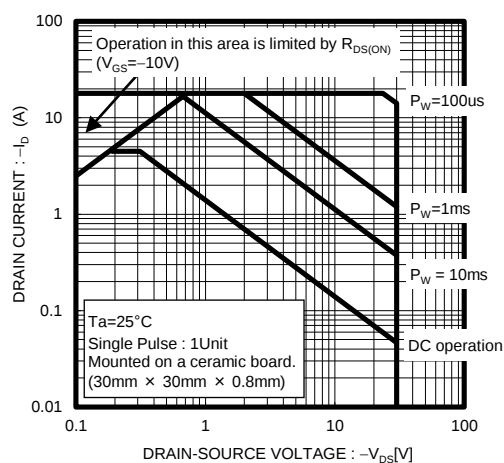
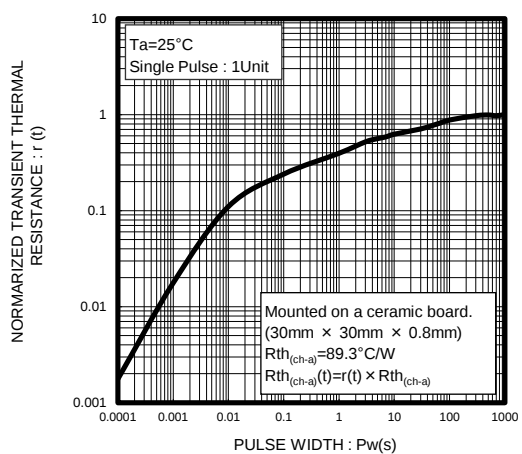


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width



● Measurement circuits

<Tr1(Nch)>

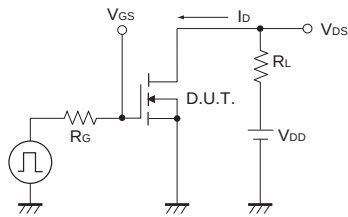


Fig.1-1 Switching Time Measurement Circuit

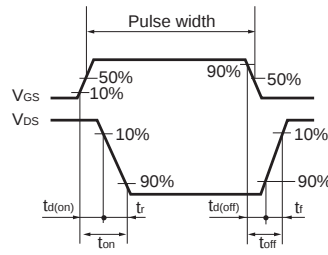


Fig.1-2 Switching Waveforms

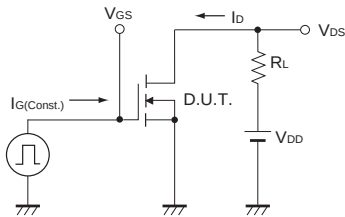


Fig.2-1 Gate Charge Measurement Circuit

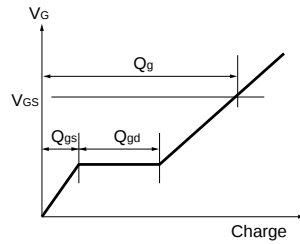


Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

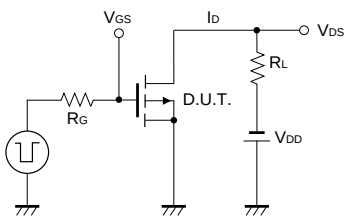


Fig.3-1 Switching Time Measurement Circuit

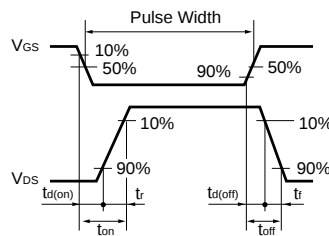


Fig.3-2 Switching Waveforms

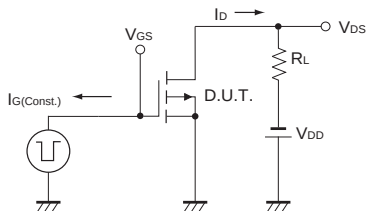


Fig.4-1 Gate Charge Measurement Circuit

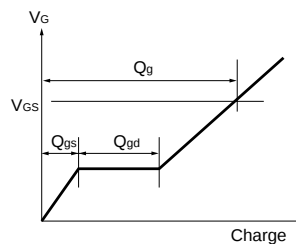


Fig.4-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Notes

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