

1.5V Drive Pch MOSFET

RW1A013ZP

●Structure

Silicon P-channel MOSFET

●Features

- 1) Low on-resistance.
- 2) High power package.
- 3) Low voltage drive. (1.5V)

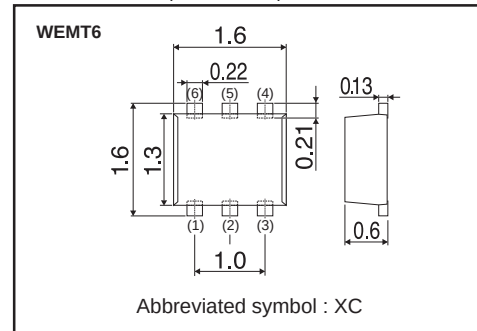
●Application

Switching

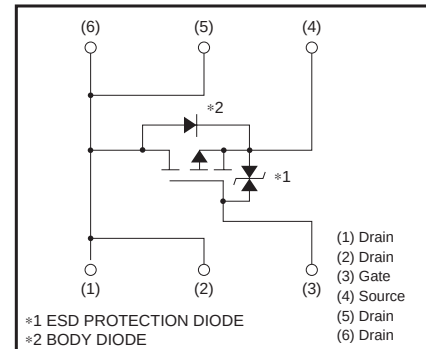
●Packaging specifications

Type	Package	Taping
	Code	T2R
	Basic ordering unit (pieces)	8000
RW1A013ZP		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DS}	-12	V
Gate-source voltage	V_{GS}	±10	V
Drain current	Continuous	I_D	±1.3
	Pulsed	I_{DP} *1	±2.6
Source current (Body diode)	Continuous	I_S	-0.5
	Pulsed	I_{SP} *1	-2.6
Total power dissipation	P_D *2	0.7	W
Channel temperature	T_{ch}	150	°C
Range of Storage temperature	T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 When mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	179	°C / W

* When mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	± 10	μA	$V_{GS}=\pm 10V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	-12	—	—	V	$I_D = -1mA$, $V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -12V$, $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-0.3	—	-1.0	V	$V_{DS} = -6V$, $I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	190	260	m Ω	$I_D = -1.3A$, $V_{GS} = -4.5V$
		—	280	390	m Ω	$I_D = -0.6A$, $V_{GS} = -2.5V$
		—	400	600	m Ω	$I_D = -0.6A$, $V_{GS} = -1.8V$
		—	530	1060	m Ω	$I_D = -0.2A$, $V_{GS} = -1.5V$
Forward transfer admittance	$ Y_{fs} $ *	1.4	—	—	S	$V_{DS} = -6V$, $I_D = -1.3A$
Input capacitance	C_{iss}	—	290	—	pF	$V_{DS} = -6V$
Output capacitance	C_{oss}	—	28	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	21	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	8	—	ns	$V_{DD} \doteq -6V$
Rise time	t_r *	—	10	—	ns	$I_D = -0.6A$
Turn-off delay time	$t_{d(off)}$ *	—	30	—	ns	$V_{GS} = -4.5V$
Fall time	t_f *	—	9	—	ns	$R_L \doteq 10\Omega$
Total gate charge	Q_g *	—	2.4	—	nC	$V_{DD} \doteq -6V$ $R_L \doteq 4.6\Omega$
Gate-source charge	Q_{gs} *	—	0.6	—	nC	$I_D = -1.3A$ $R_G=10\Omega$
Gate-drain charge	Q_{gd} *	—	0.4	—	nC	$V_{GS} = -4.5V$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	—	—	-1.2	V	$I_S = -1.3A$, $V_{GS}=0V$

*Pulsed

●Electrical characteristics

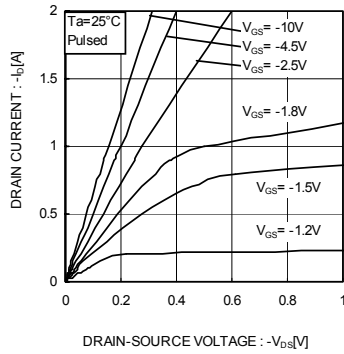


Fig.1 Typical Output Characteristics(I)

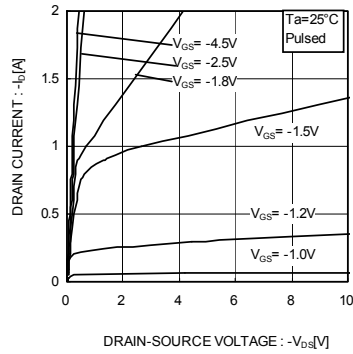


Fig.2 Typical Output Characteristics(II)

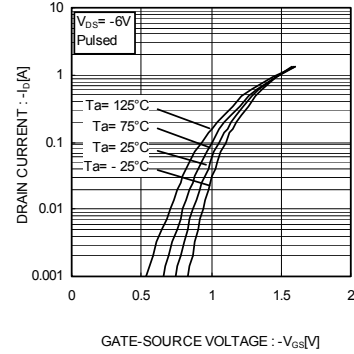
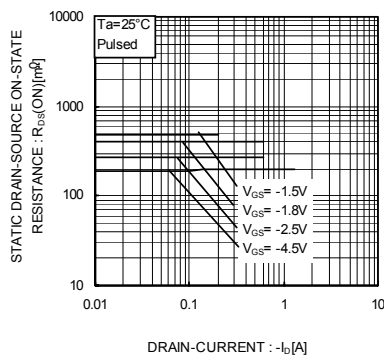
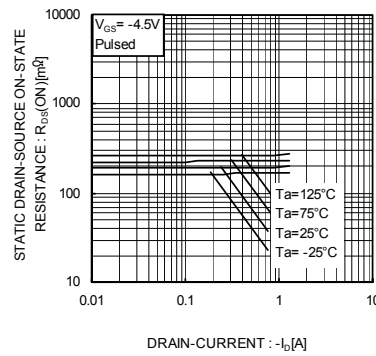
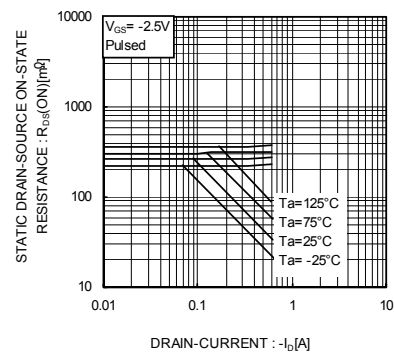
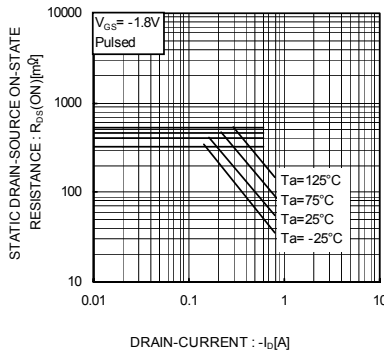
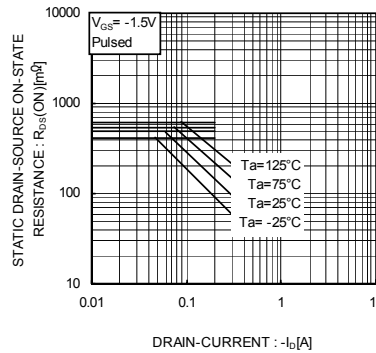
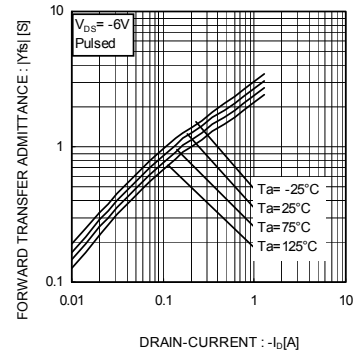
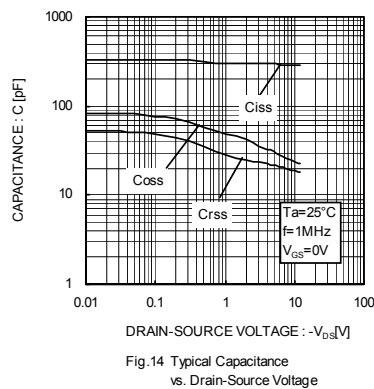
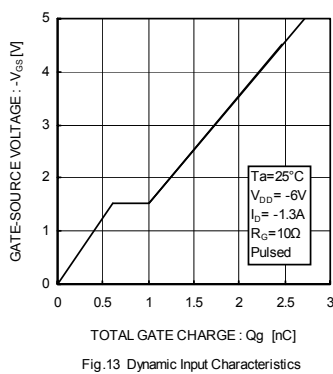
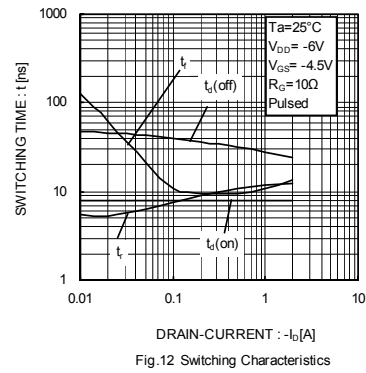
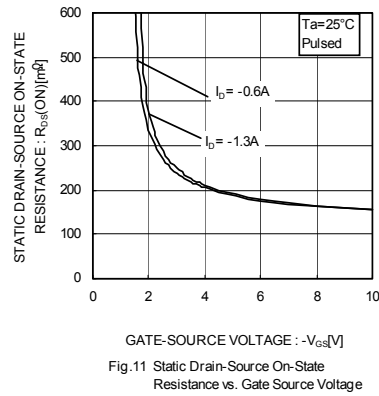
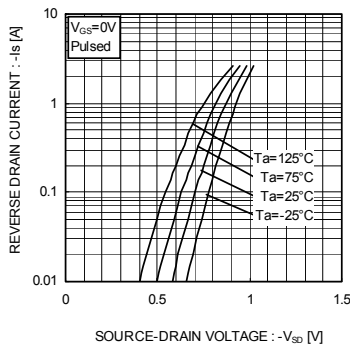
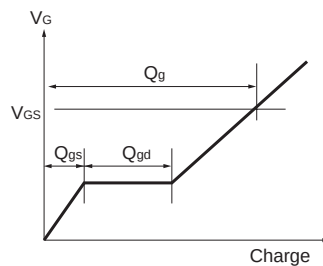
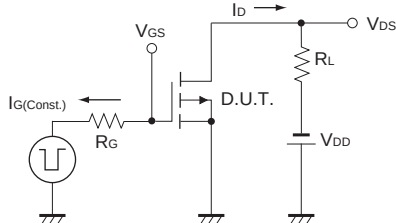
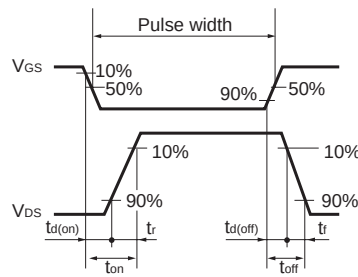
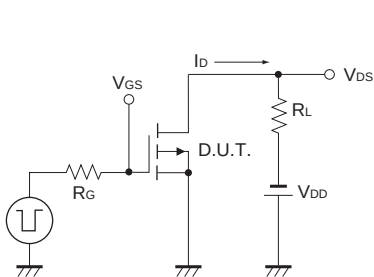


Fig.3 Typical Transfer Characteristics

Fig.4 Static Drain-Source On-State
Resistance vs. Drain Current(I)Fig.5 Static Drain-Source On-State
Resistance vs. Drain Current(II)Fig.6 Static Drain-Source On-State
Resistance vs. Drain Current(III)Fig.7 Static Drain-Source On-State
Resistance vs. Drain Current(IV)Fig.8 Static Drain-Source On-State
Resistance vs. Drain Current(V)Fig.9 Forward Transfer Admittance
vs. Drain Current



●Measurement circuits



●Notice

This product might cause chip aging and breakdown under the large electrified environment . Please consider to design ESD protection circuit.

Notes

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