

1.5V Drive Nch MOSFET

RUF020N02

●Structure

Silicon N-channel MOSFET

●Features

- 1) Low On-resistance.
- 2) Space saving, small surface mount Package (TUMT3).
- 3) Low voltage drive (1.5V drive).

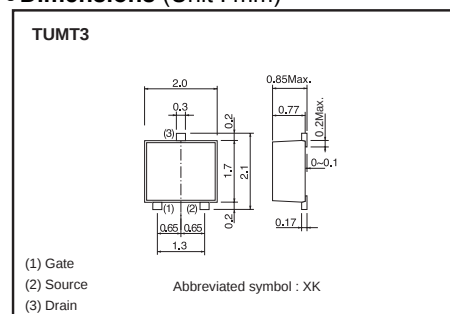
●Applications

Switching

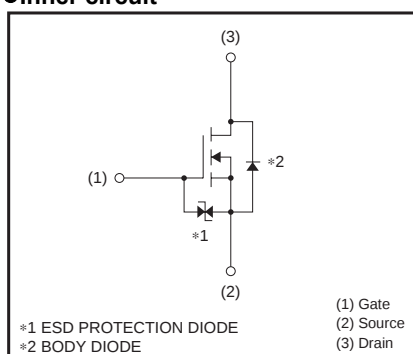
●Packaging specifications

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	3000
RUF020N02		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GS}	± 10	V
Drain current	Continuous	I_D	± 2	A
	Pulsed	I_{DP} *1	± 6	A
Source current (Body diode)	Continuous	I_S	0.6	A
	Pulsed	I_{SP} *1	6	A
Total power dissipation		P_D *2	0.8	W
Channel temperature		T_{ch}	150	°C
Range of storage temperature		T_{stg}	-55 to +150	°C

*1 $P_w \leq 10 \mu s$, Duty cycles $\leq 1\%$

*2 When mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	156	°C/W

* When mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	± 10	μA	$V_{GS}=\pm 10V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	20	–	–	V	$I_D=1mA$, $V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	$V_{DS}=20V$, $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.3	–	1.0	V	$V_{DS}=10V$, $I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	–	75	105	m Ω	$I_D=2A$, $V_{GS}=4.5V$
		–	95	135	m Ω	$I_D=2A$, $V_{GS}=2.5V$
		–	130	185	m Ω	$I_D=1A$, $V_{GS}=1.8V$
		–	170	240	m Ω	$I_D=0.4A$, $V_{GS}=1.5V$
Forward transfer admittance	$ Y_{fs} ^*$	1.8	–	–	S	$V_{DS}=10V$, $I_D=2A$
Input capacitance	C_{iss}	–	180	–	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	–	45	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	–	25	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	–	6	–	ns	$V_{DD}\doteq 10V$
Rise time	t_r^*	–	17	–	ns	$I_D=1A$ $V_{GS}=4.5V$
Turn-off delay time	$t_{d(off)}^*$	–	30	–	ns	$R_L\doteq 10\Omega$
Fall time	t_f^*	–	30	–	ns	$R_G=10\Omega$
Total gate charge	Q_g^*	–	2.0	–	nC	$V_{DD}\doteq 10V$, $I_D=2A$
Gate-source charge	Q_{gs}^*	–	0.6	–	nC	$V_{GS}=4.5V$
Gate-drain charge	Q_{gd}^*	–	0.4	–	nC	$R_L\doteq 5\Omega$, $R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}^*	–	–	1.2	V	$I_S=2A$, $V_{GS}=0V$

*Pulsed

●Electrical characteristics curves

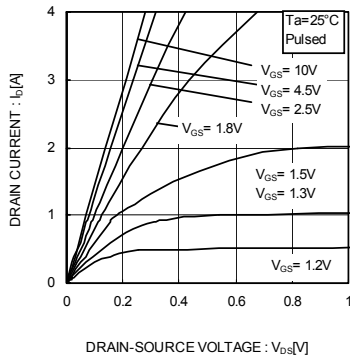


Fig.1 Typical Output Characteristics(I)

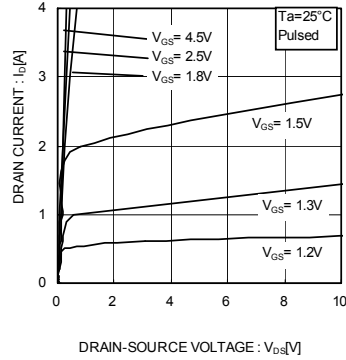


Fig.2 Typical Output Characteristics(II)

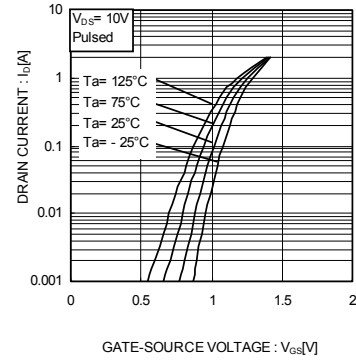


Fig.3 Typical Transfer Characteristics

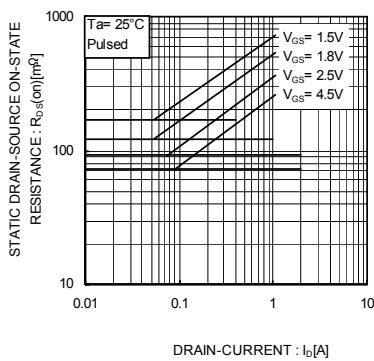


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

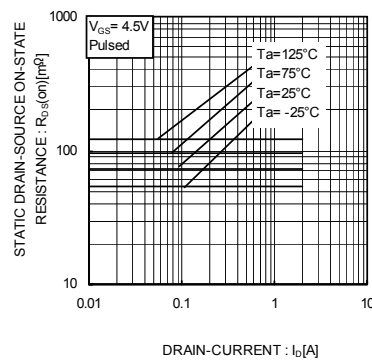


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

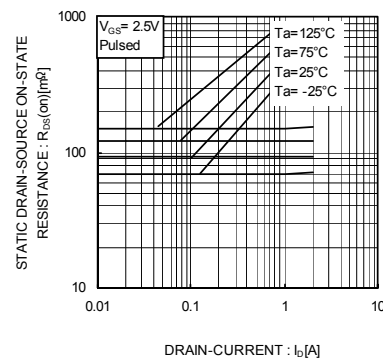


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

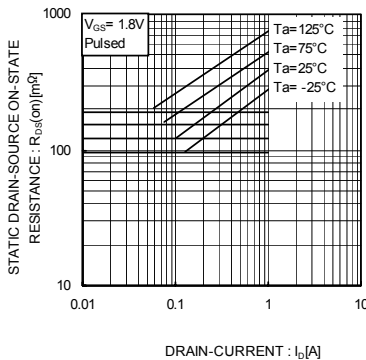


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

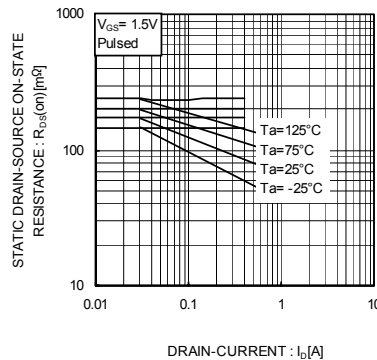


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

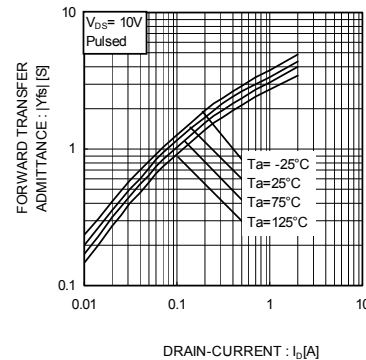
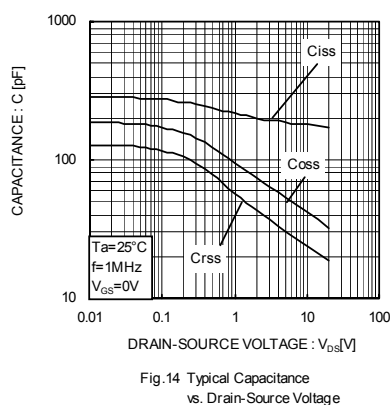
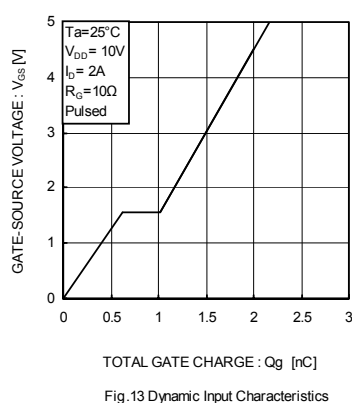
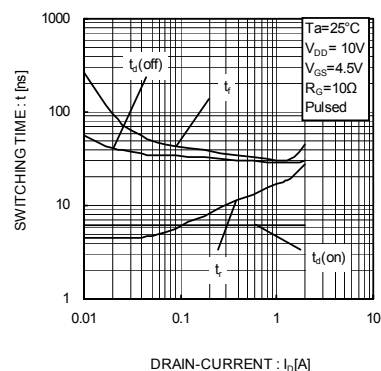
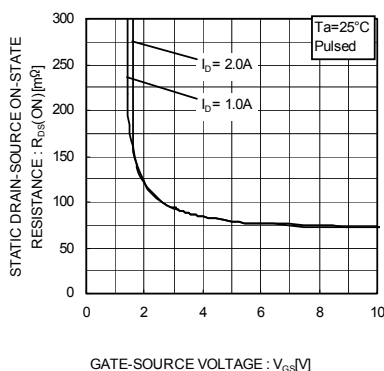
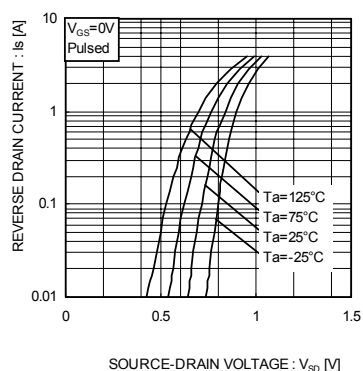
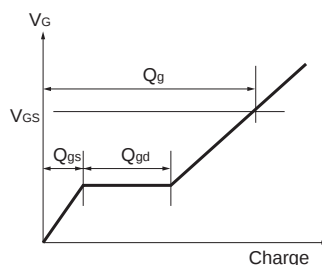
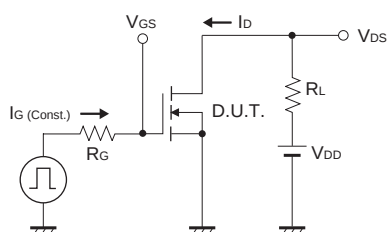
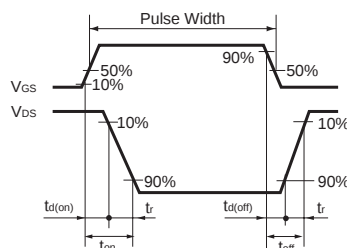
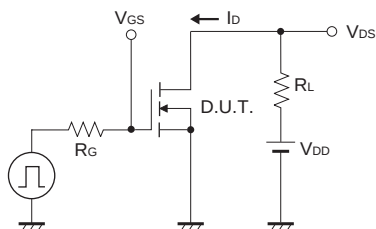


Fig.9 Forward Transfer Admittance vs. Drain Current



●Measurement circuit



●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Notes

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