

RSR025N03

Silicon N-channel
MOS FET

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (TSMT3) .

Power switching, DC / DC converter.

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	3000
RSR025N03		○

Parameter		Symbol	Limits	Unit
Drain-source voltage		V _{DSS}	30	V
Gate-source voltage		V _{GSS}	20	V
Drain current	Continuous	I _D	±2.5	A
	Pulsed	I _{DP} *1	±10	A
Source current (Body diode)	Continuous	I _S	0.8	A
	Pulsed	I _{SP} *1	3.2	A
Total power dissipation		P _D *2	1	W
Channel temperature		T _{ch}	150	°C
Storage temperature		T _{stg}	–55 to 150	°C

*1 $P_w \leq 100\mu s$, Duty cycle $\leq 2\%$
*2 Mounted on a ceramic board.

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth (ch-a)*	125	°C / W

*2 Mounted on a ceramic board.

The drawing shows the mechanical specifications for a TSMT3 package. The top view (left) indicates a rectangular body with a width of 2.9 and a length of 1.9. The distance between the centers of the two leads is 1.6. The lead width is 0.4, and the lead pitch is 0.7. The distance from the body edge to the lead center is 0.95. The side view (right) shows a maximum height of 1.0, a lead thickness of 0.85, a lead height of 0.7, and a standoff height of 0.16. The leads are spaced 0.3 apart.

TSMT3

2.9
0.4
(3)
1.6
2.8
(1) (2)
0.95 0.95
1.9
1.0MAX
0.85
0.7
0-0.1
0.16
0.3

(1) Gate
(2) Source
(3) Drain

Each lead has same dimensions

Abbreviated symbol : QY

The schematic diagram on the left shows a MOSFET with an ESD protection diode (*1) connected between the gate (1) and source (*2). Another ESD protection diode (*2) is connected between the drain (3) and source (*2). The footprint diagram on the right shows a rectangular package with three pins: pin (1) on the left, pin (2) on the right, and pin (3) on the top.

(1) Gate
(2) Source
(3) Drain

*1 ESD PROTECTION DIODE
*2 BODY DIODE

*A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	10	μA	$V_{GS}=20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	30	—	—	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS}=30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	—	2.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	50	70	m Ω	$I_D=2.5A, V_{GS}=10V$
		—	74	105		$I_D=2.5A, V_{GS}=4.5V$
		—	83	118		$I_D=2.5A, V_{GS}=4V$
Forward transfer admittance	$ Y_{fs} $ *	1.5	—	—	S	$I_D=2.5A, V_{DS}=10V$
Input capacitance	C_{iss}	—	165	—	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	—	55	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	35	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	6	—	ns	$I_D=1.25A, V_{DD} \approx 15V$
Rise time	t_r *	—	10	—	ns	$V_{GS}=10V$
Turn-off delay time	$t_{d(off)}$ *	—	20	—	ns	$R_L=12.0\Omega$
Fall time	t_f *	—	5	—	ns	$R_G=10\Omega$
Total gate charge	Q_g *	—	2.9	4.1	nC	$V_{DD} \approx 15V$
Gate-source charge	Q_{gs} *	—	0.8	—	nC	$V_{GS}=5V$
Gate-drain charge	Q_{gd} *	—	0.9	—	nC	$I_D=2.5A$

*Pulsed

●Body diode characteristics (Source-Drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	—	—	1.2	V	$I_S=3.2A, V_{GS}=0V$

*Pulsed

Transistors

●Electrical characteristic curves

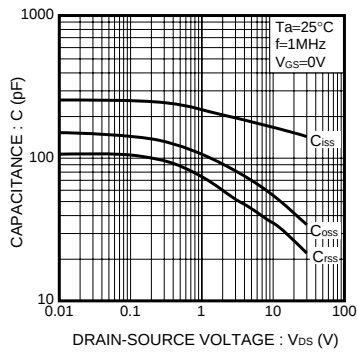


Fig.1 Typical Capacitance vs. Drain-Source Voltage

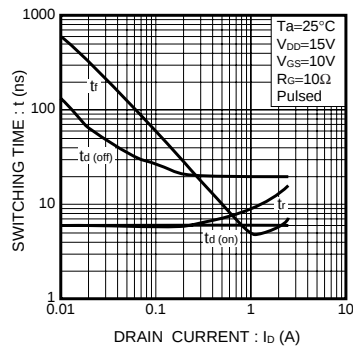


Fig.2 Switching Characteristics

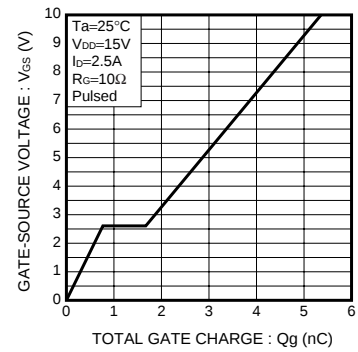


Fig.3 Dynamic Input Characteristics

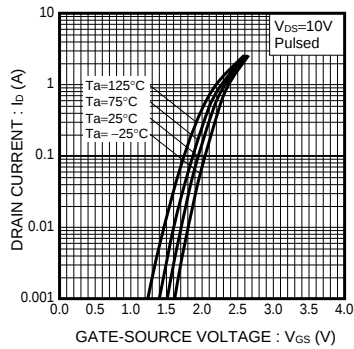


Fig.4 Typical Transfer Characteristics

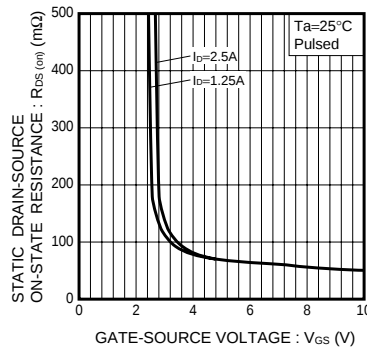


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

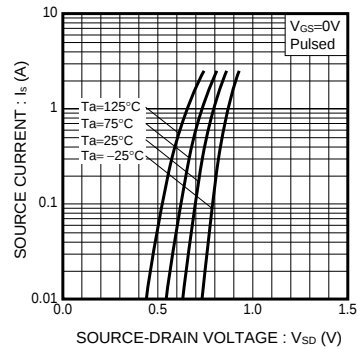


Fig.6 Source Current vs. Source-Drain Voltage

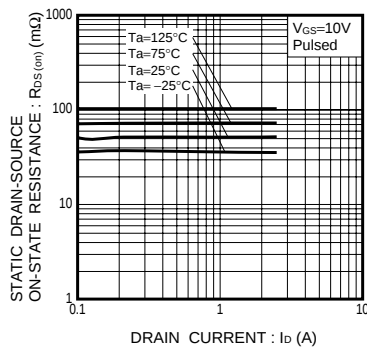


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

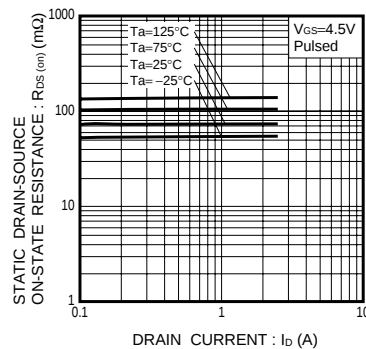


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

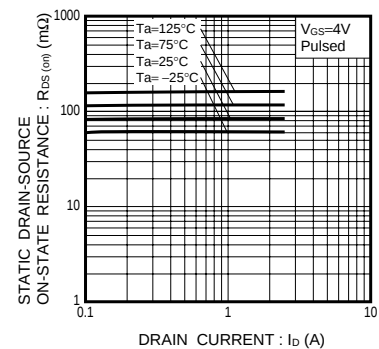


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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