

1.5V Drive Pch MOSFET

RAF040P01

● Structure

Silicon P-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) Low voltage drive(1.5V drive).
- 3) Small surface mount package(TUMT3).

● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TCL
	Basic ordering unit (pieces)	3000
RAF040P01		○

● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	-12	V
Gate-source voltage		V_{GSS}	0 to -8	V
Drain current	Continuous	I_D	±4	A
	Pulsed	I_{DP} *1	±16	A
Source current (Body Diode)	Continuous	I_S	-0.6	A
	Pulsed	I_{SP} *1	-16	A
Power dissipation		P_D *2	0.8	W
Channel temperature		T_{ch}	150	°C
Range of storage temperature		T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

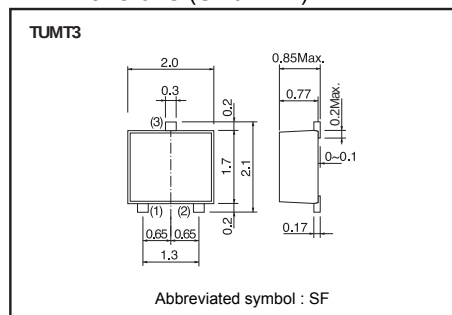
*2 Mounted on a ceramic board.

● Thermal resistance

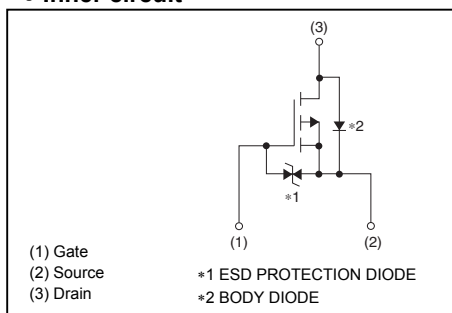
Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)^*$	156	°C / W

*Mounted on a ceramic board.

● Dimensions (Unit : mm)



● Inner circuit



● Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	-10	μA	$V_{GS} = -8V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-12	-	-	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	-	-	-10	μA	$V_{DS} = -12V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-0.3	-	-1.0	V	$V_{DS} = -6V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	-	22	30	$m\Omega$	$I_D = -4A, V_{GS} = -4.5V$
		-	27	38		$I_D = -2A, V_{GS} = -2.5V$
		-	35	53		$I_D = -2A, V_{GS} = -1.8V$
		-	40	68		$I_D = -0.8A, V_{GS} = -1.5V$
Forward transfer admittance	$ Y_{fs} $ *	5.5	-	-	S	$V_{DS} = -6V, I_D = -4A$
Input capacitance	C_{iss}	-	4000	-	pF	$V_{DS} = -6V$
Output capacitance	C_{oss}	-	410	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	-	400	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	-	15	-	ns	$V_{DD} = -6V, I_D = -2A$
Rise time	t_r *	-	43	-	ns	$V_{GS} = -4.5V$
Turn-off delay time	$t_{d(off)}$ *	-	240	-	ns	$R_L = 3\Omega$
Fall time	t_f *	-	120	-	ns	$R_G = 10\Omega$
Total gate charge	Q_g *	-	37	-	nC	$V_{DD} = -6V, I_D = -4A$
Gate-source charge	Q_{gs} *	-	6.0	-	nC	$V_{GS} = -4.5V$
Gate-drain charge	Q_{gd} *	-	5.5	-	nC	

*Pulsed

● Body diode characteristics (Source-Drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD} *	-	-	-1.2	V	$I_S = -4A, V_{GS} = 0V$

*Pulsed

●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical Output Characteristics (I)

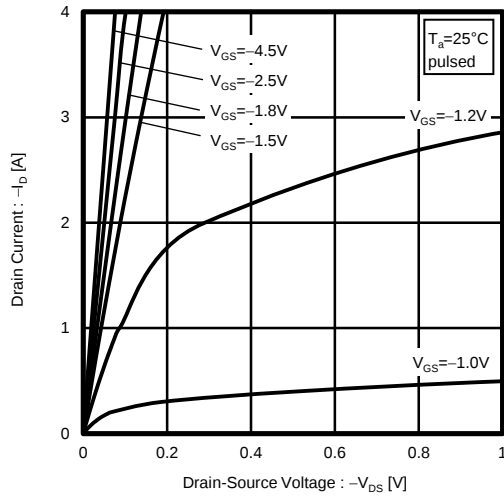


Fig.2 Typical Output Characteristics (II)

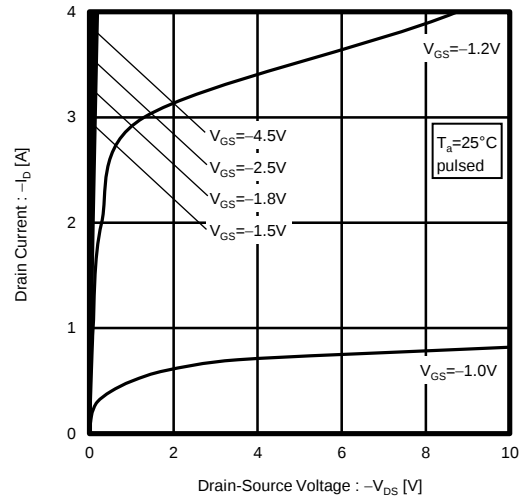


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

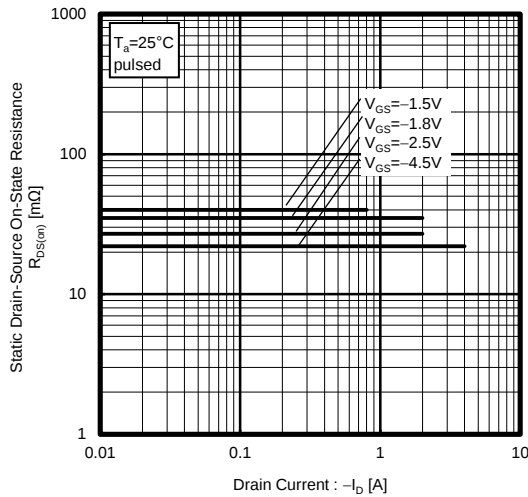


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

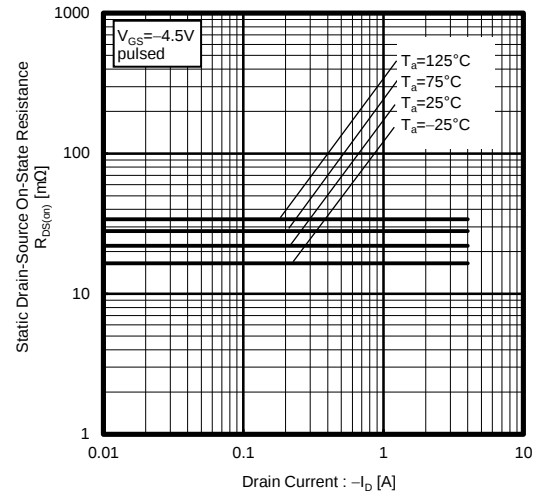


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

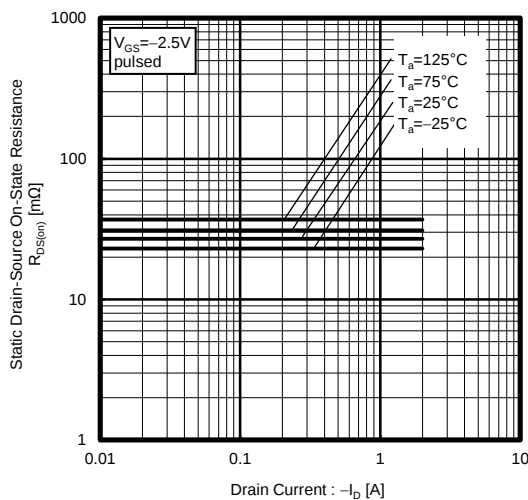


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

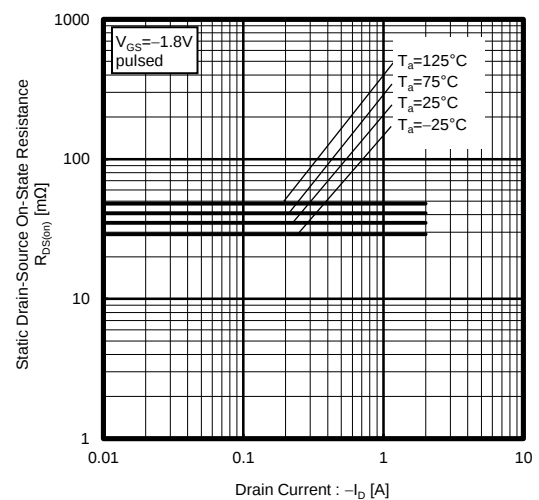


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current

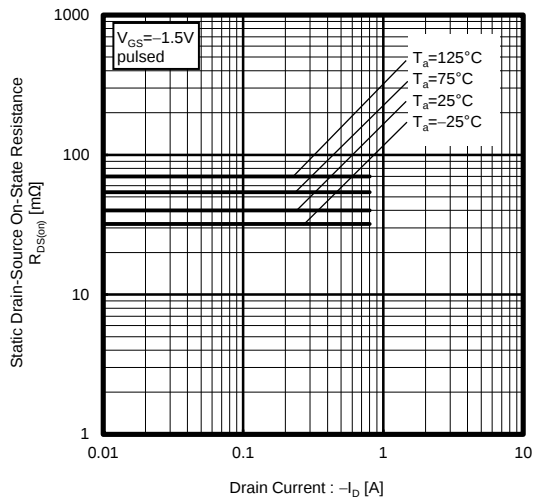


Fig.8 Forward Transfer Admittance vs. Drain Current

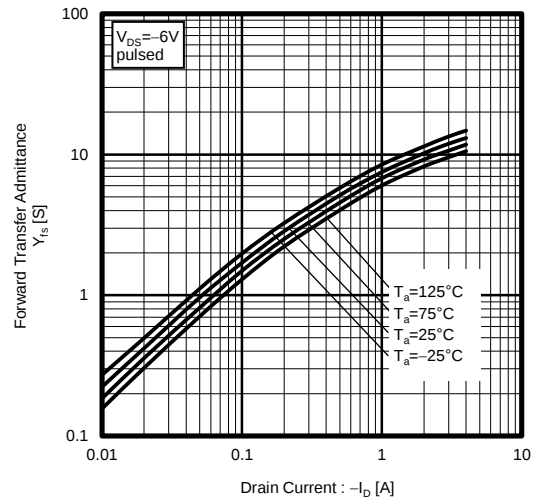


Fig.9 Typical Transfer Characteristics

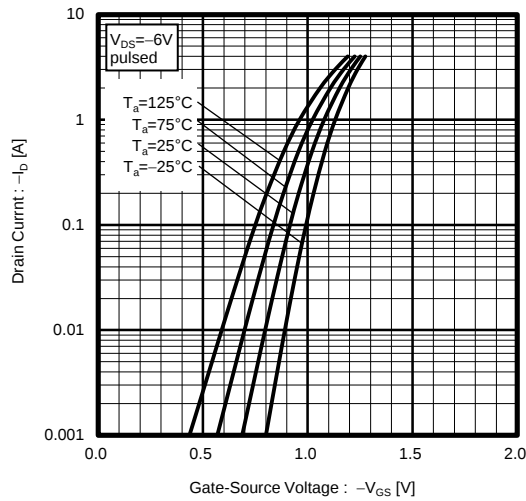


Fig.10 Source Current vs. Source-Drain Voltage

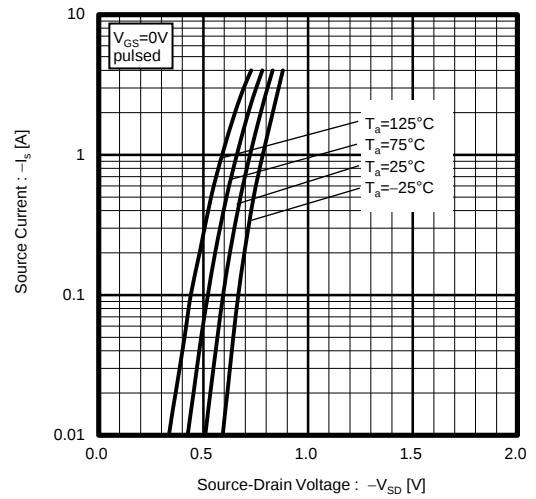


Fig.11 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

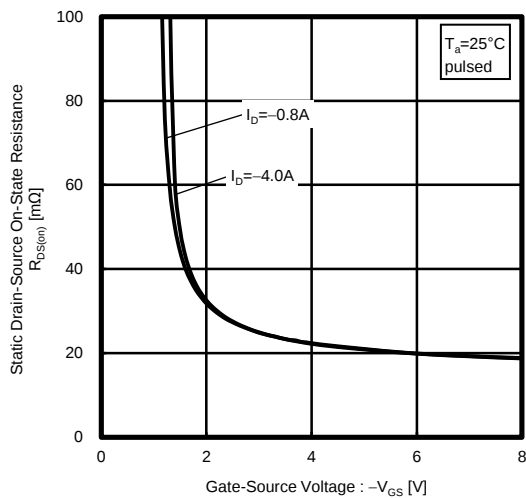


Fig.12 Switching Characteristics

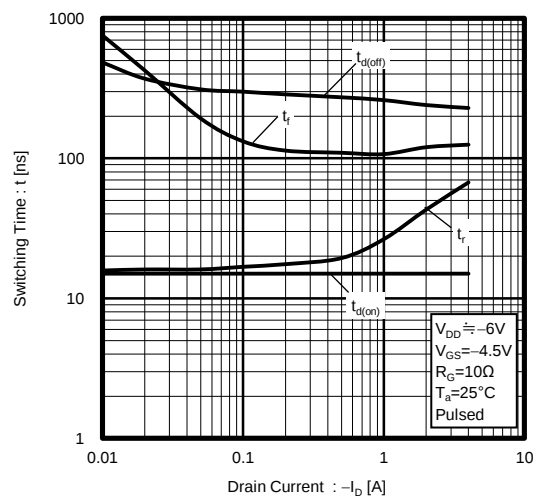


Fig.13 Dynamic Input Characteristics

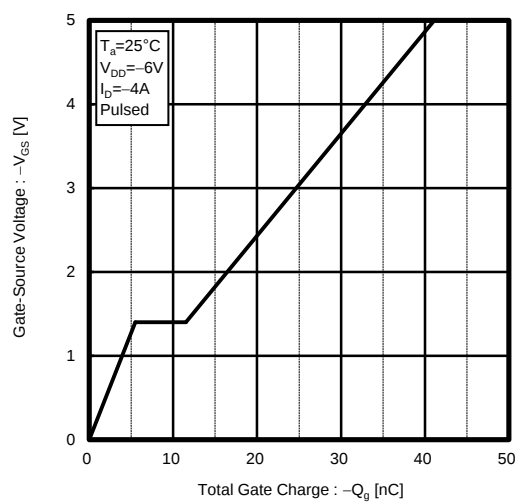
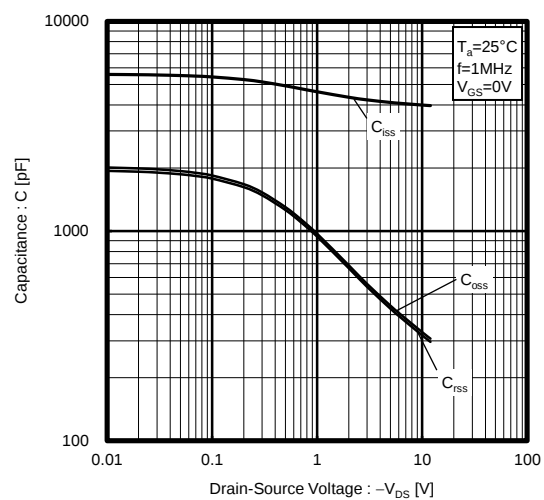


Fig.14 Typical Capacitance vs. Drain-Source Voltage



● Measurement circuits

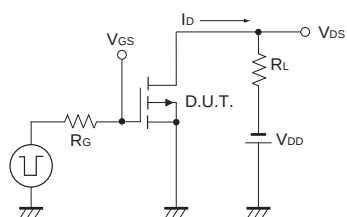


Fig.1-1 Switching Time Measurement Circuit

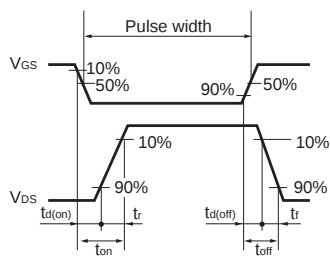


Fig.1-2 Switching Waveforms

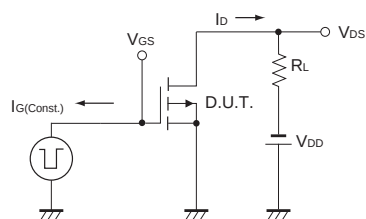


Fig.2-1 Gate Charge Measurement Circuit

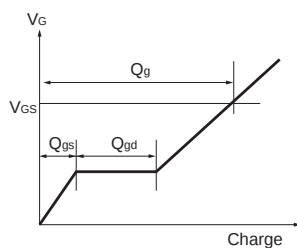


Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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