

QS5U27

Silicon P-channel MOS FET
Schottky Barrier DIODE

- 1) The QS5U27 combines Pch MOS FET with a Schottky barrier diode in a TSMT5 package.
- 2) Low on-state resistance with fast switching.
- 3) Low voltage drive (2.5V).
- 4) Built-in schottky barrier diode has low forward voltage.

load switch, DC/DC conversion

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
OS5U27		○

The drawing shows the TSM7 package with the following dimensions:

- Top View:**
 - Overall width: 2.9
 - Distance between lead centers: 1.9
 - Lead width: 0.95
 - Lead pitch: 0.95
 - Lead height: 1.6
 - Lead spacing: 2.8
 - Lead width: 0.4
- Side View:**
 - Maximum height: 1.0 MAX
 - Lead height: 0.85
 - Lead width: 0.7
 - Lead thickness: 0-0.1
 - Lead height: 0.3-0.6
 - Lead width: 0.16

The diagram shows a MOSFET with its source terminal connected to ground (pin 3). The gate terminal (pin 1) is connected to a positive voltage source (pin 5). The drain terminal (pin 4) is connected to a load resistor and a positive voltage source (pin 2). An ESD protection diode (labeled *1) is connected between the gate and source. A body diode (labeled *2) is connected between the drain and source. The legend indicates: (1) Gate, (2) Source, (3) Anode, (4) Cathode, (5) Drain.

* A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

Transistor

●Absolute maximum ratings (Ta=25°C)

<MOSFET>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V _{DSS}	−20	V
Gate-source voltage		V _{GSS}	±12	V
Drain current	Continuous	I _D	±1.5	A
	Pulsed	I _{DP} *1	±6.0	A
Source current (Body diode)	Continuous	I _S	−0.75	A
	Pulsed	I _{SP} *1	−3.0	A
Channel temperature		T _{ch}	150	°C
Power dissipation		P _D *3	0.9	W / ELEMENT

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Repetitive peak reverse voltage	V _{RM}	25	V
Reverse voltage	V _R	20	V
Forward current	I _F	1.0	A
Forward current surge peak	I _{FSM} *2	3.0	A
Junction temperature	T _j	150	°C
Power dissipation	P _D *3	0.7	W / ELEMENT

<MOSFET AND Di>

Total power dissipation	P _D *3	1.25	W / TOTAL
Range of Storage temperature	T _{stg}	−55 to +150	°C

*1 Pw≤10μs, Duty cycles≤1% *2 60Hz·1cyc. *3 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	−	−	±10	μA	V _{GS} =±12V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	−20	−	−	V	I _D =−1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	−	−	−1	μA	V _{DS} =−20V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	−0.7	−	−2.0	V	V _{DS} =−10V, I _D =−1mA
Static drain-source on-state resistance	R _{DS(on)} *	−	160	200	mΩ	I _D =−1.5A, V _{GS} =−4.5V
		−	180	240	mΩ	I _D =−1.5A, V _{GS} =−4V
		−	260	340	mΩ	I _D =−0.75A, V _{GS} =−2.5V
Forward transfer admittance	Y _{fs} *	1.0	−	−	S	V _{DS} =−10V, I _D =−0.75A
Input capacitance	C _{iss}	−	325	−	pF	V _{DS} =−10V
Output capacitance	C _{oss}	−	60	−	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	−	40	−	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	−	10	−	ns	I _D =−0.75A
Rise time	t _r *	−	10	−	ns	V _{DD} ≒−15V
Turn-off delay time	t _{d(off)} *	−	35	−	ns	V _{GS} =−4.5V
Fall time	t _f *	−	10	−	ns	R _L =20Ω
Total gate charge	Q _g	−	4.2	−	nC	R _G =10Ω
Gate-source charge	Q _{gs}	−	1.0	−	nC	V _{DD} ≒−15V
Gate-drain charge	Q _{gd}	−	1.1	−	nC	V _{GS} =−4.5V
					nC	I _D =−1.5A

* Pulsed

<Body diode (source–drain)>

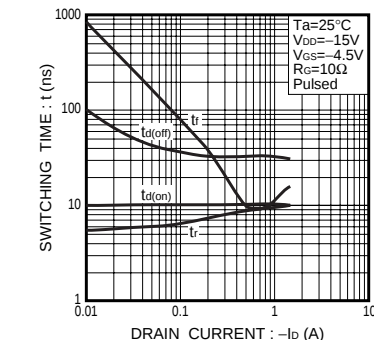
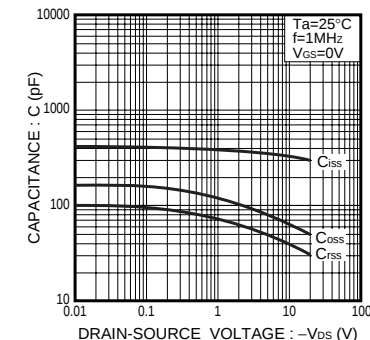
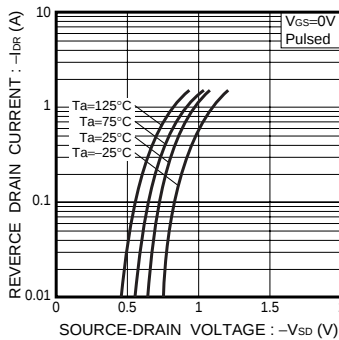
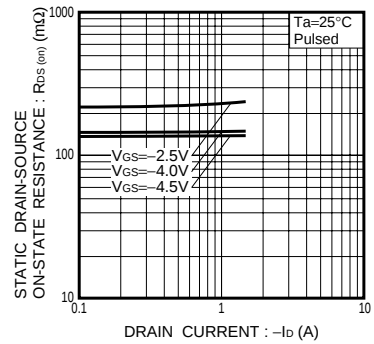
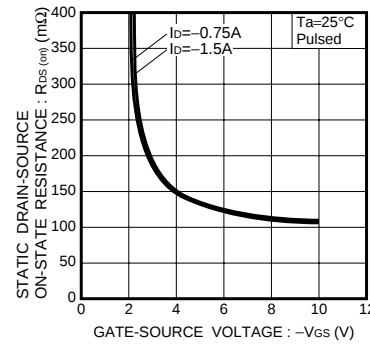
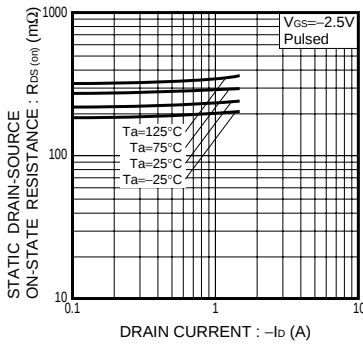
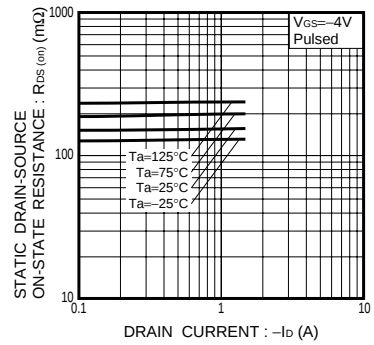
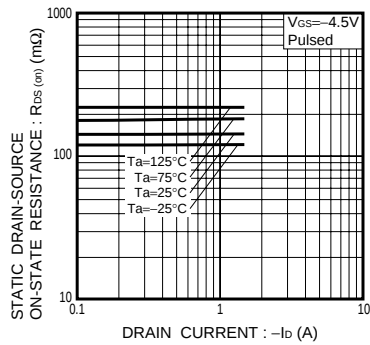
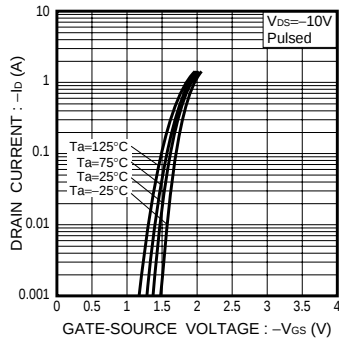
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD}	−	−	−1.2	V	I _S =−0.75A, V _{GS} =0V

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _F	−	−	0.45	V	I _F =1.0A
Reverse current	I _R	−	−	200	μA	V _R =20V

Transistor

●Electrical characteristic curves



Transistor

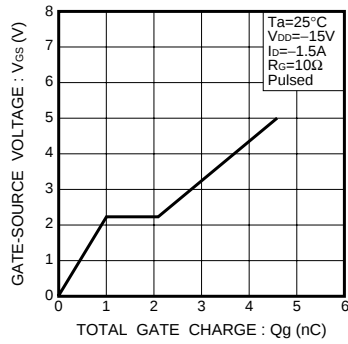


Fig.10 Dynamic Input Characteristics

●Measurement circuits

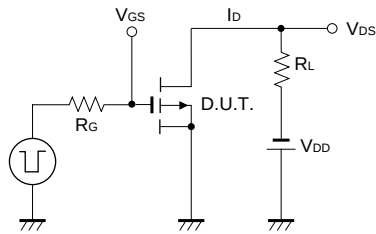


Fig.11 Switching Time Measurement Circuit

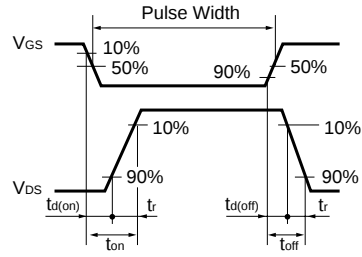


Fig.12 Switching Waveforms

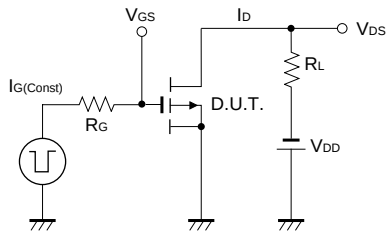


Fig.13 Gate Charge Measurement Circuit

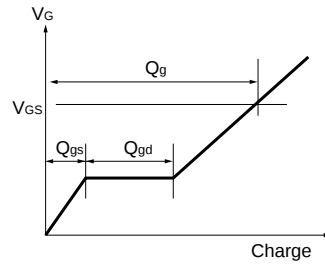


Fig.14 Gate Charge Waveforms

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